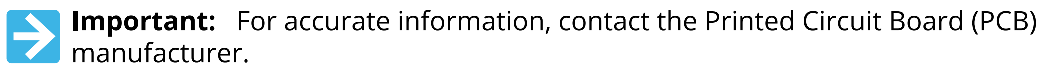
PolarFire FPGA Package Fanout Application Note

AN5672

PolarFire FPGA Package Fanout (Ask a Question)

Microchip offers Field Programmable Gate Array (FPGA) devices with the following three pitch sizes: 0.5 mm, 0.8 mm and 1 mm. The density, complexity, and type of routing differ across devices based on the application and size of the board. This application note provides information about the number of layers, cost implications, the size of pads and vias for different package sizes.


Important: For accurate information, contact the Printed Circuit Board (PCB) manufacturer.

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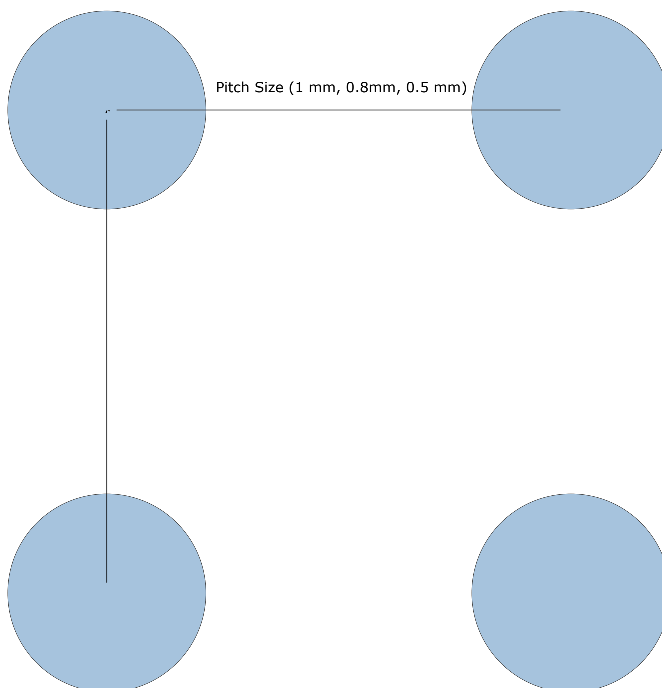
1. Pitch Size (Ask a Question)

The following figure illustrates the pitch size between the adjacent pads in a device package.

Figure 1-1. Pitch Size



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2. Pad Recommendation (Ask a Question)

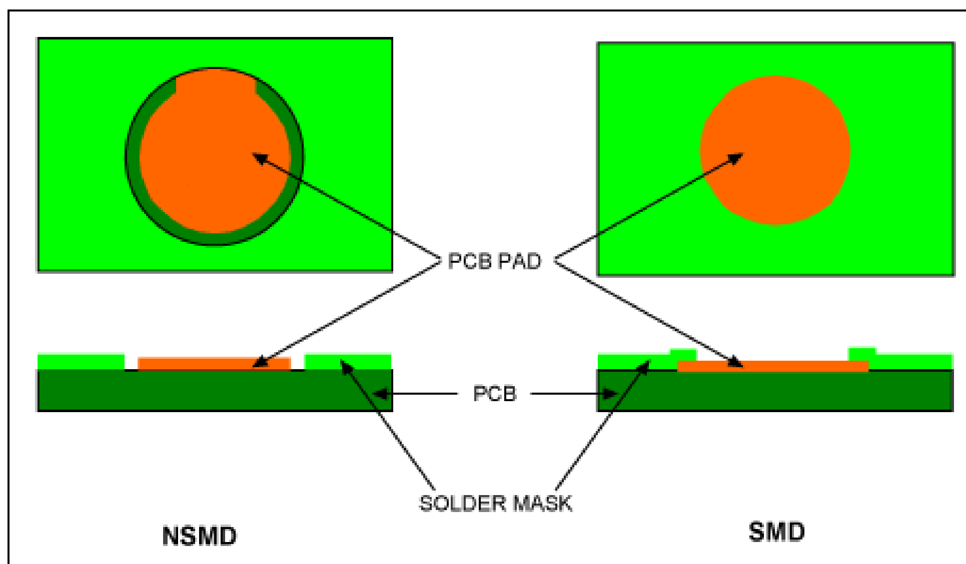
There are two types of Ball Grid Array (BGA) pads:

Non-Solder Mask Defined (NSMD)	NSMD type of pads help to achieve balanced stress on solder joints.
Solder Mask Defined (SMD).	The solder mask essentially defines the boundaries of the pad.

Important: Microchip recommends NSMD type of pads for all the devices.

The following figure illustrates the two BGA types.

Figure 2-1. BGA Pad Types



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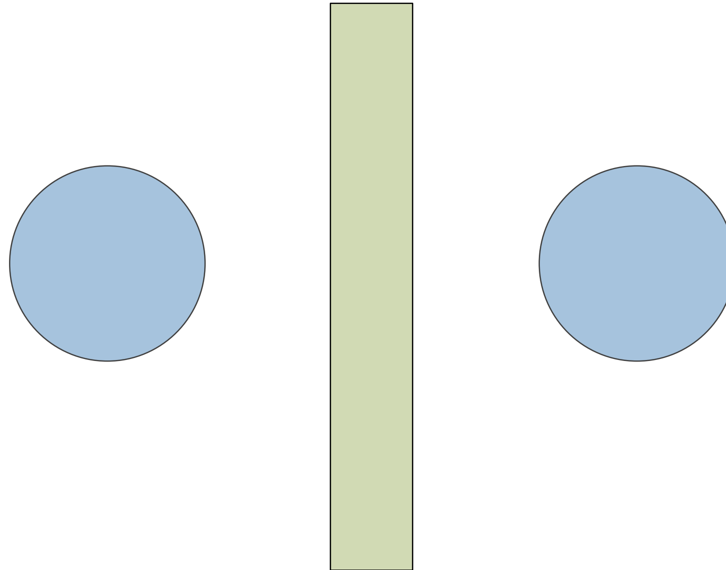
3. Types of Routing (Ask a Question)

The device has routing to all four directions for different signals. There are two types of signal fanouts: Single-Trace Breakout and Dual-Trace Breakout.

3.1 Single-Trace Breakout (Ask a Question)

In single-trace breakout, a single trace is fanned out between two pads on the outer layers and two fanout vias on the internal signal layers, as illustrated in the following figure.

Figure 3-1. Single-Trace Breakout



A single-trace breakout has high amount of copper-to-copper clearance. Therefore, it does not need an advanced technology for PCB fabrication. The per-layer cost for copper etching is less than that of dual-trace breakout.

3.2 Dual-Trace Breakout (Ask a Question)

Dual-trace breakout employs two signal traces between two BGA pads on the outer layers, and two traces between two fanout vias on the internal signal layers, as illustrated in the following figure.

Important: Dual-trace breakout is only possible with 1 mm pitch packages. For smaller packages, the space between two pads/vias might not be sufficient to route two traces, and PCB fabrication is costly.

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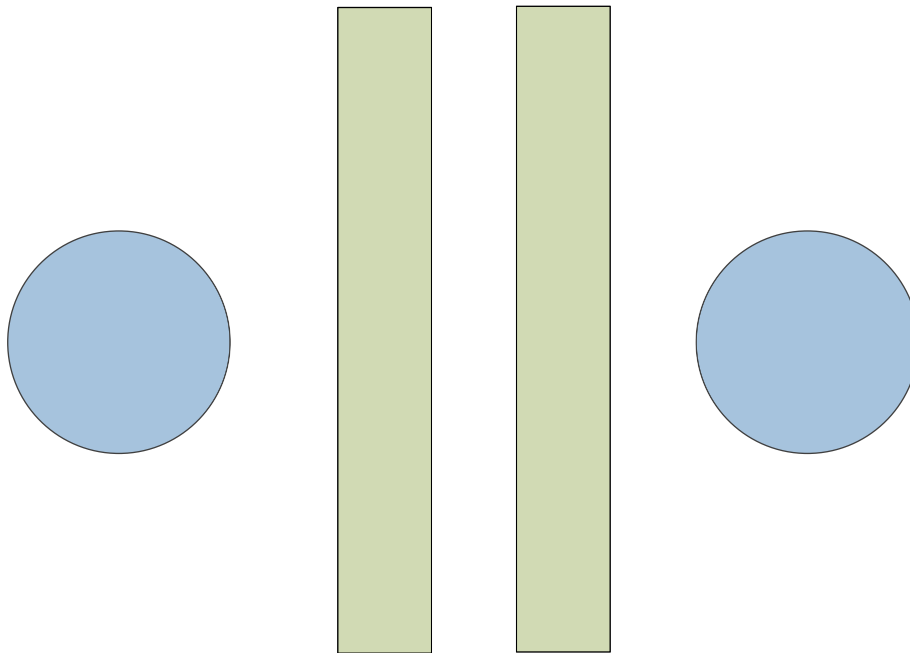
Figure 3-2. Dual-Trace Breakout



This kind of fanout needs very precise control for copper clearance and trace width, therefore, costing more than the single-trace breakout.

Important: No blind or buried via technology is employed for the fanout.

Table 3-1. Signal Layer Requirements

BGA Pins	Pitch Size (mm)	Number of Signal Layers Needed	
—	—	Dual Trace	Single Trace
484	0.8	3	4
484	1.0	2	4
536	0.5	—	3
784	1.0	3	5
1152	1.0	3	6

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4. Layout Consideration (Ask a Question)

The number of layers depend on the number of signals routed from the package.

In Microchip's FPGA devices, the signal pins constitute about 55–65% of the total pins in the package. The number of layers increases linearly with the number of signal pins to be routed. In applications with space constraints, the trace width can be narrowed down to route multiple traces between two pads/vias.

Important: Though this approach accommodates more traces in the BGA area, it causes impedance discontinuity in that region and increases crosstalk between the signals.

Tip: Microchip recommends contacting the signal integrity engineers if a narrowing down approach is followed.

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5. Stack-Up Design (Ask a Question)

A good stack-up design leads to better performance. The number of layers in the stack-up depends on the following factors:

- The board's form factor
- The number of signals to be routed
- Power requirements

Based on these factors, the designer chooses how many layers the board requires.

The upper-power layers must be used for high-priority supplies. High-switching current supplies should be placed vertically close to the devices to decrease the distance that the current needs to travel through the vias. Ground planes should be placed adjacent to the high-transient current power planes to reduce inductance and to provide decoupling of higher frequency noise.

It is good to have power and ground layers side-by-side so that the inter-plane capacitance provides better decoupling at high frequencies. The effect of vias on power pins is reduced by placing a power plane near the device. Signal integrity depends on how well the traces have controlled impedance, so it is always recommended to have controlled impedance.

Tip: Microchip recommends that all critical high-speed signals, such as DDR and transceiver PCIe signals, have a solid ground reference. These signals should be separated from each other by a good distance, ground, or power planes. This minimizes crosstalk and provides balanced and clean transmission lines with properly controlled characteristic impedance between devices and other board components. For the best performance, use dedicated ground plane layers that are continuous across the entire board area. Power planes can provide an adequate reference; however, the power planes should be related to the signals they serve to reference.

Important: Do not use unrelated power planes as a signal reference.

Slots should not interrupt the planes, or else they can force current to find an alternate return path. This undesired return path may cause a localized bounce on the power or ground plane that can be capacitively coupled to all signals adjacent to the planes

For example, the FC484 1.0 mm package features a single-trace breakout. The layers required for FC484 package are the following:

- Signal layers: 4
- Power plane: 2
- Ground layer: 4

Table 5-1. Sample Stack-Up Layers

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness
		Solderm...		Dielectric	3.3	0.5	
1	8	Signal	Top/Signal	Conductive			1.4
		Prepreg		Dielectric	4.3	3	
2		Plane	GND	Conductive			1.4
		Core		Dielectric	4.3	5	

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...........continued

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness
3		Signal	Signal Layer	Conductive			1.4
		Prepreg		Dielectric	4.3	5	
4		Signal	GND	Conductive			1.4
		Core		Dielectric	4.3	5	
5		Plane	VDD/Power Supply	Conductive			1.4
		Prepreg		Dielectric	4.3	18	
6		Plane	VDD/Power Supply	Conductive			1.4
		Core		Dielectric	4.3	5	
7		Signal	GND	Conductive			1.4
		Prepreg		Dielectric	4.3	5	
8		Signal	Signal Layer	Conductive			1.4
		Core		Dielectric	4.3	5	
9		Plane	Ground	Conductive			1.4
		Prepreg		Dielectric	4.3	3	
10		Signal	Bottom/Signal	Conductive			1.4
		Solderm...		Dielectric	3.3	0.5	

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6. Pinout (Ask a Question)

Some pins in these devices are assigned with specific functionality, such as JTAG and clock inputs. For these pins, the routing constraints are fixed, and swapping is not allowed.

For the DDR interface, the software defines the pin functionality, and limited swapping support is available.

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7. Fabrication Technology (Ask a Question)

Refers to the process and materials used to manufacture semiconductor devices. For fabrication, the following aspects must to be considered:

- Aspect Ratio
- Micro Via and Back-Drilled Via
- Via on Pad

7.1 Aspect Ratio (Ask a Question)

Aspect ratio is the ratio of thickness of the board, and maximum drill diameter of the Plated Through Holes (PTH) that are used on the board. By traditional PCB fabrication methods, the aspect ratio must not be more than 1/10. This means the PTH diameter on the board must be 1/10 of the board thickness or more. When a smaller via hole is required, blind and buried via on PCB must be used. The drill hole is usually 3 mils wider than the required diameter, as the via plating process reduces the drill diameter by 3 mils.

Important: For accurate aspect ratio, contact the fabrication vendor.

7.2 Micro Via and Back-Drilled Via (Ask a Question)

The use of blind and buried vias for signals increases the cost of PCB compared to PTH via, as the micro via needs more precise tolerance control on the PCB for drilling and copper clearance.

In some applications, the PTH via needs to be drilled from one end of the board to get rid of extra via stub on high frequency signals. The back drilling increases the cost of PCB because of the increase in fabrication complexity.

7.3 Via on Pad (Ask a Question)

The use of via on pad increases the cost of PCB because of the extra fabrication cycle of PCB, as it requires copper plating to cover the via on the pad. The pad is used to mount the components. The addition of micro vias, via-in-pad, and layers increase the PCB cost.

Important: For information about the PCB fabrication costs, contact the PCB fabrication vendor.

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8. Routing Guidelines for 1 mm Pitch Packages (Ask a Question)

The following figures illustrate the routing guidelines for fabricating 1 mm pitch packages, such as FC1152 and FCG484.

Figure 8-1. Single-Trace Breakout Between Two Balls (mils)

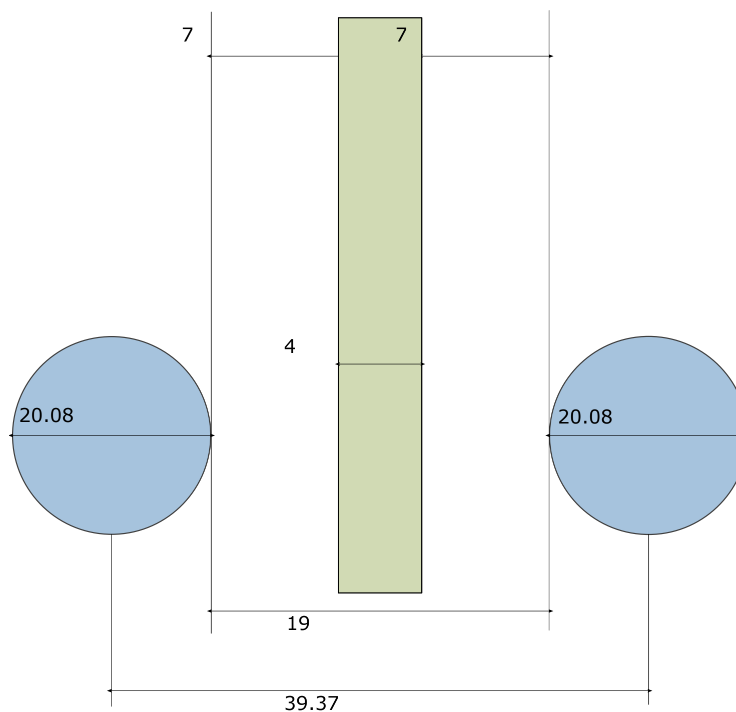

Figure 8-2. Dual-Trace Breakout Between Two Balls (mils)

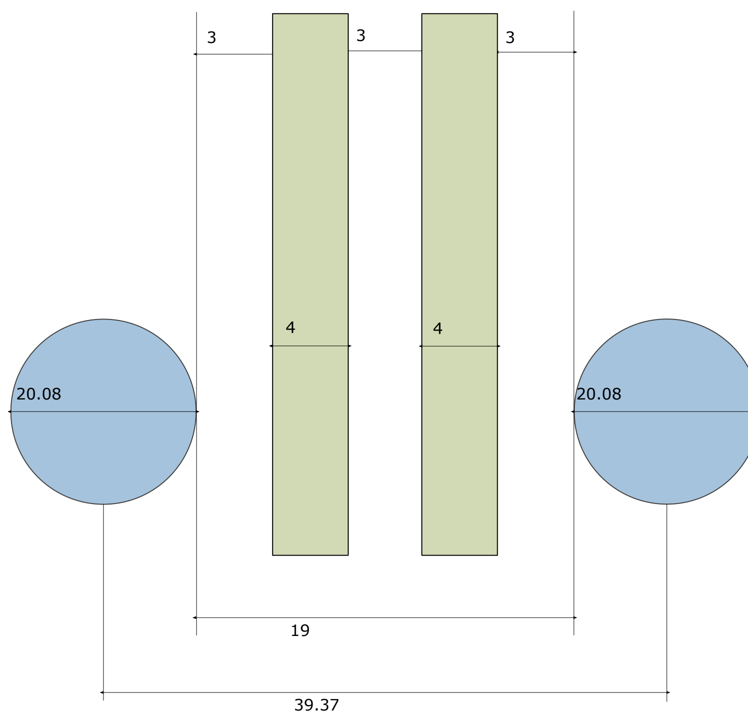

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Figure 8-3. Single-Trace Route Between Two Vias (mils)

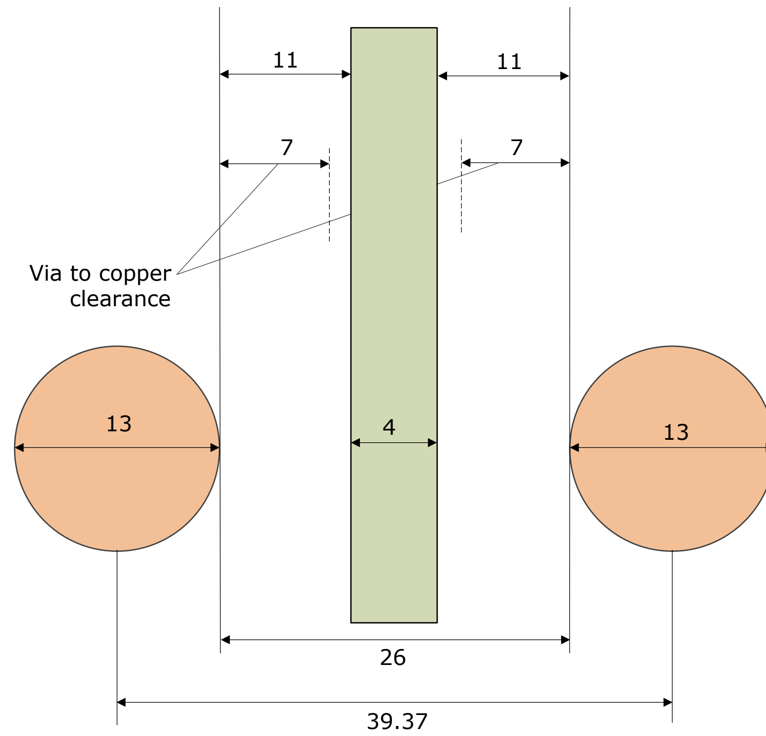
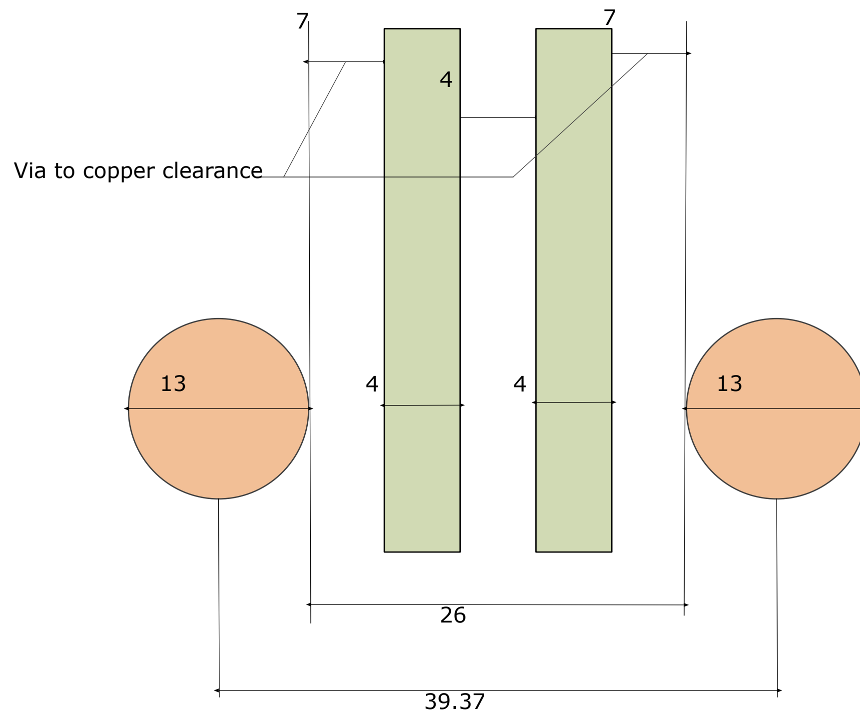


Figure 8-4. Double-Trace Route Between Two Vias (mils)



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8.1 Single-Trace Breakout for FC1152 (Ask a Question)

The following figures illustrate the single-trace breakout for FC1152.

Figure 8-5. Layer-1, Single-Trace Breakout (1 mm Pitch)

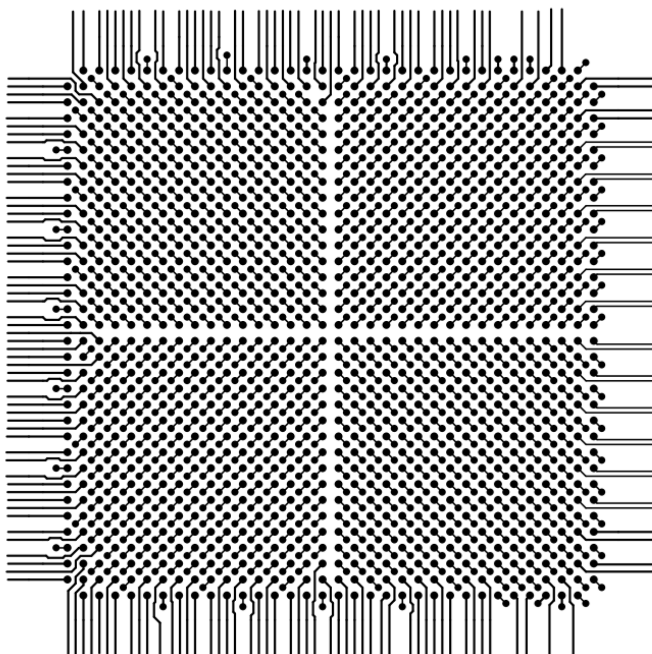

Figure 8-6. Layer-2, Single-Trace Breakout (1 mm Pitch)

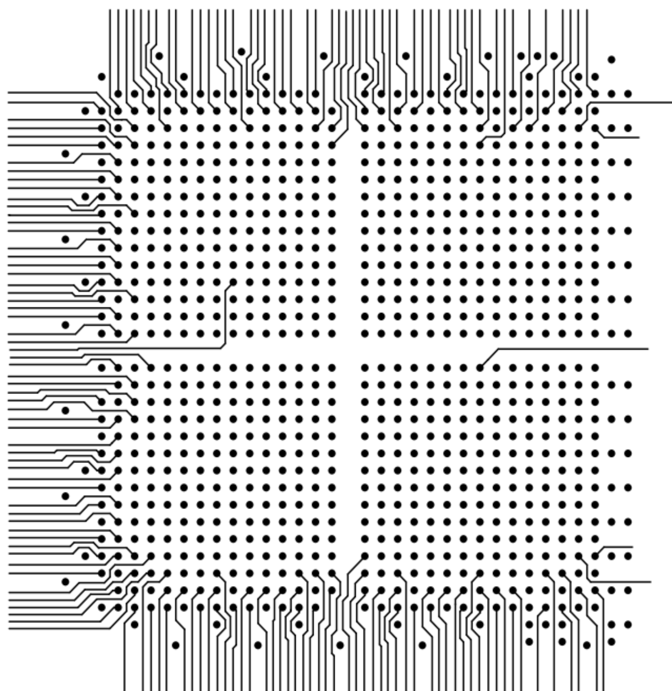

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Figure 8-7. Layer-3, Single-Trace Breakout (1 mm Pitch)

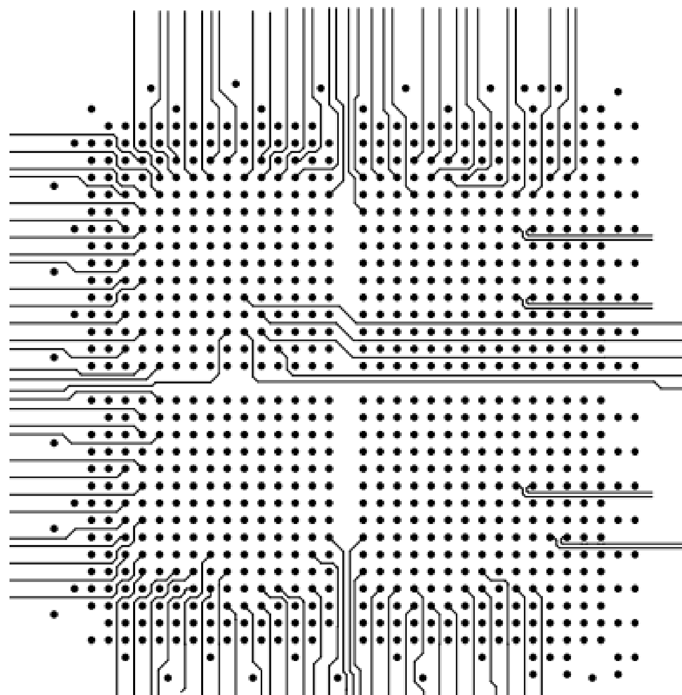

Figure 8-8. Layer-4, Single-Trace Breakout (1 mm Pitch)

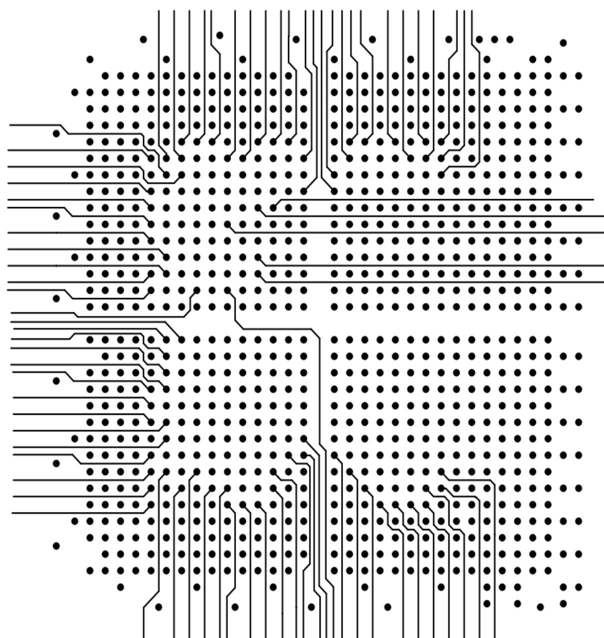

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Figure 8-9. Layer-5, Single-Trace Breakout (1 mm Pitch)

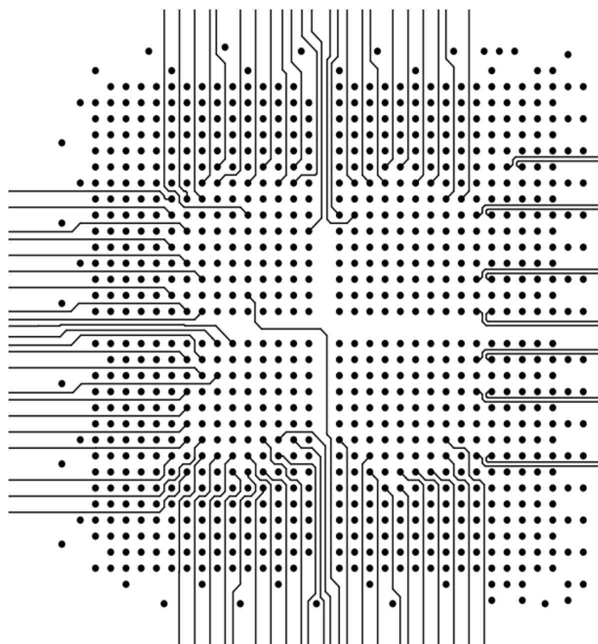
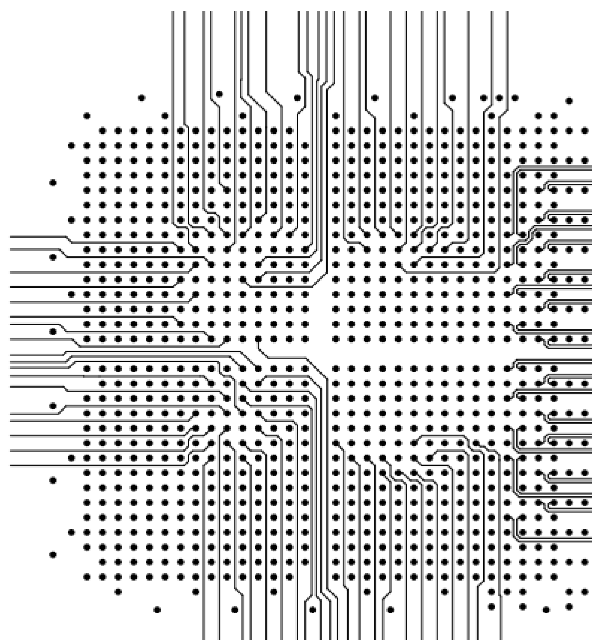


Figure 8-10. Layer-6, Single-Trace Breakout (1 mm Pitch)



8.2 Dual-Trace Breakout for FC1152 (Ask a Question)

The following figures illustrate the dual-trace breakout for FC1152.

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Figure 8-11. Layer-1, Dual-Trace Breakout (1 mm Pitch)

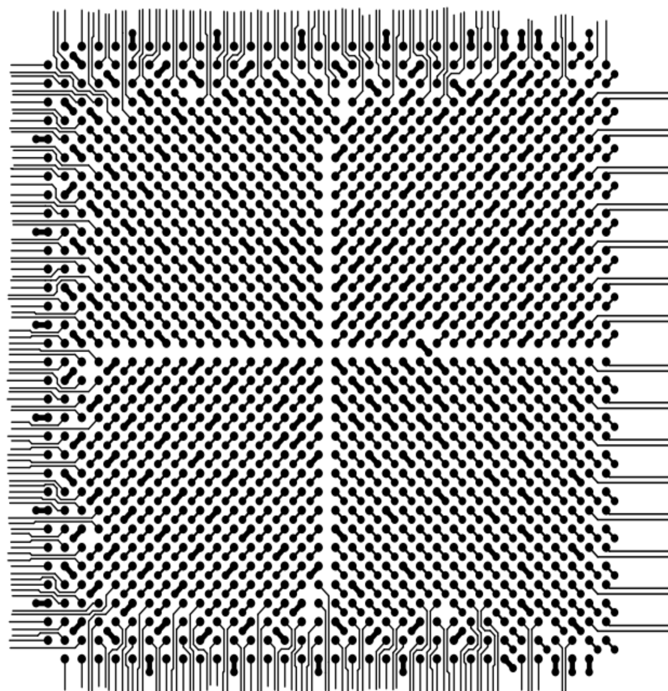

Figure 8-12. Layer-2, Dual-Trace Breakout (1 mm Pitch)

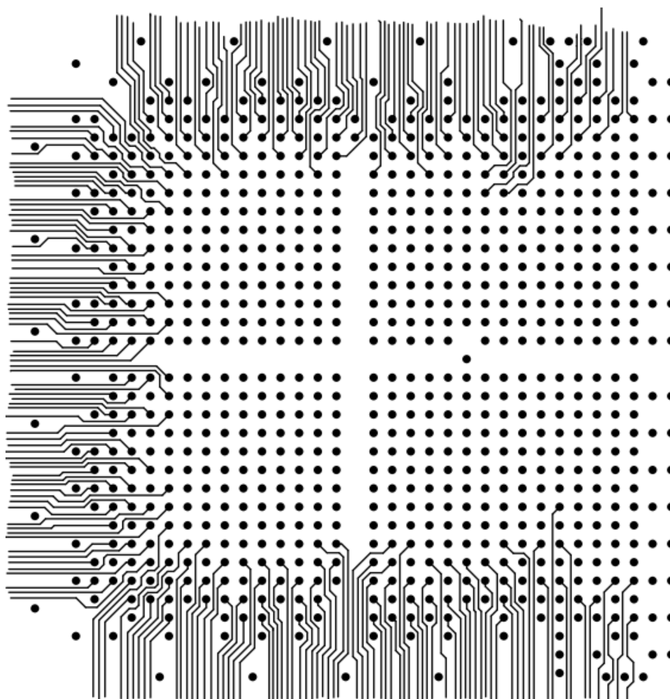

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Figure 8-13. Layer-3, Dual-Trace Breakout (1 mm Pitch)

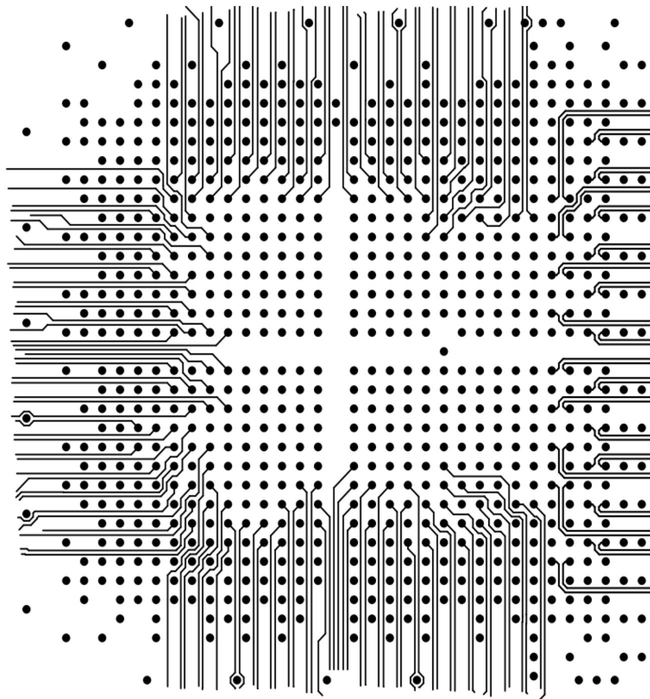
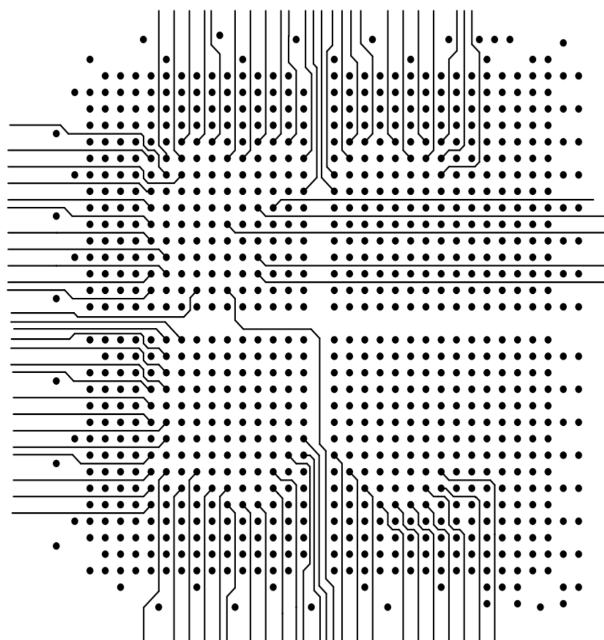


Figure 8-14. Layer-4, Dual-Trace Breakout (1 mm Pitch)



8.3 Single-Trace Breakout for FCG784 (Ask a Question)

The following figures illustrate the single-trace breakout for FCG784.

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Figure 8-15. Layer-1, Single-Trace Breakout (1 mm Pitch)

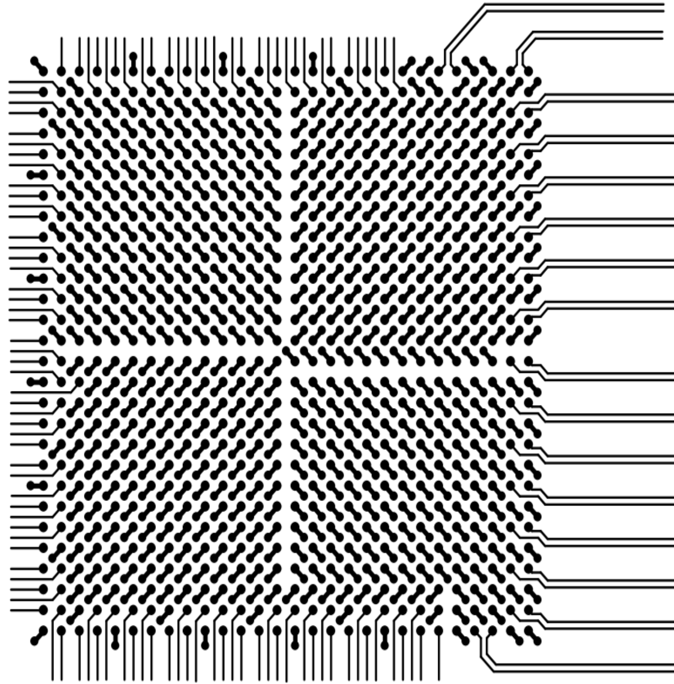

Figure 8-16. Layer-2, Single-Trace Breakout (1 mm Pitch)

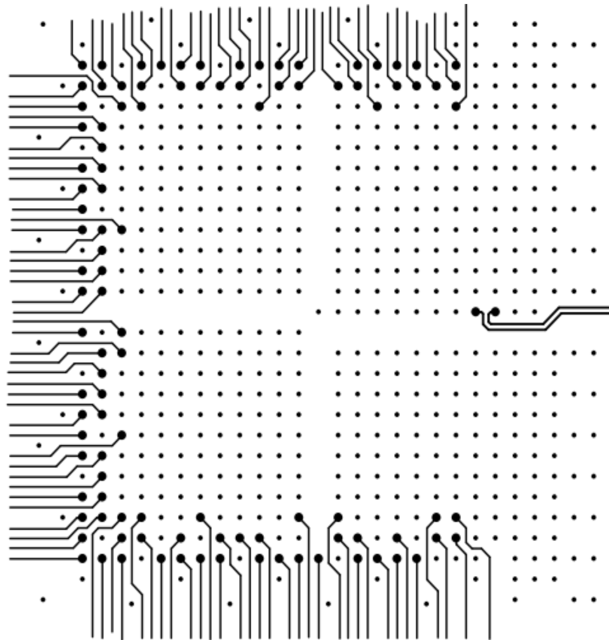

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Figure 8-17. Layer-3, Single-Trace Breakout (1 mm Pitch)

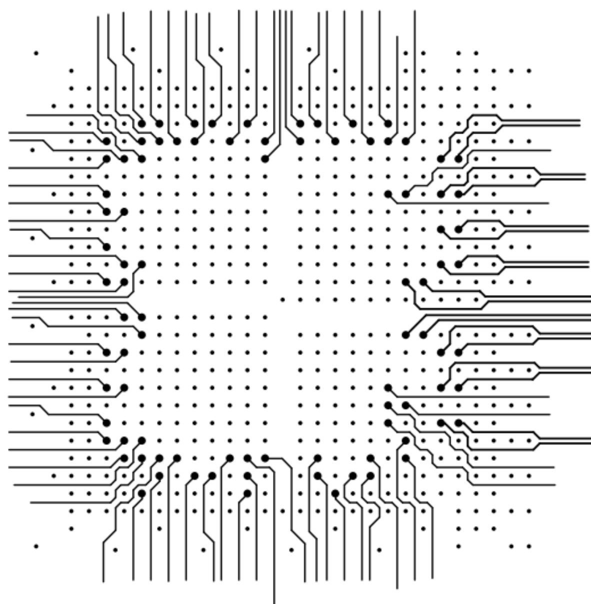

Figure 8-18. Layer-4, Single-Trace Breakout (1 mm Pitch)

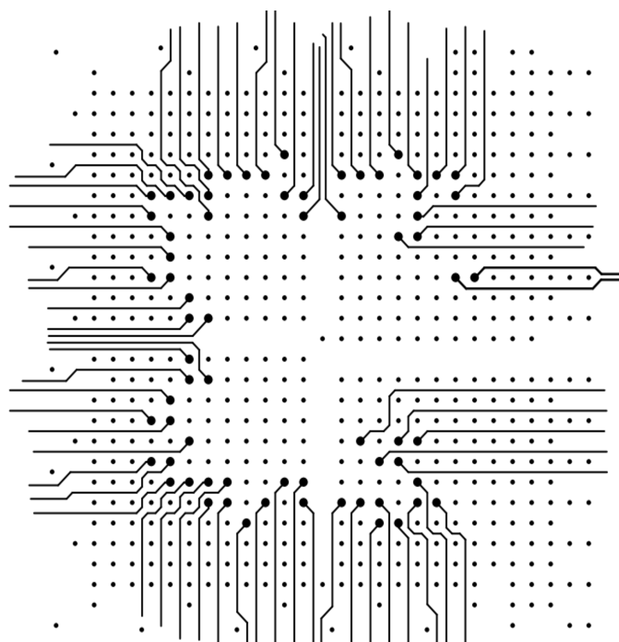

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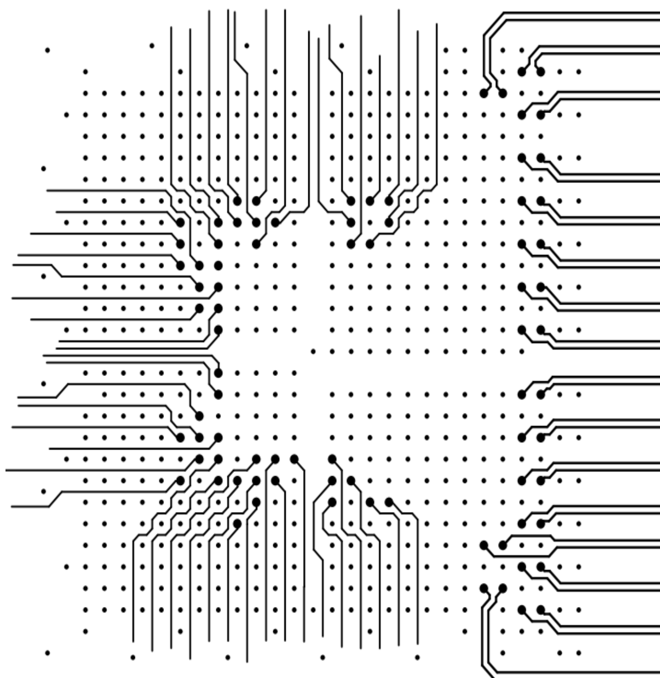
Figure 8-19. Layer-5, Single-Trace Breakout (1 mm Pitch)



8.4 Dual-Trace Breakout for FCG784 (Ask a Question)

The following figures illustrate the dual-trace breakout for FCG784.

Figure 8-20. Layer-1, Dual-Trace Breakout (1 mm Pitch)

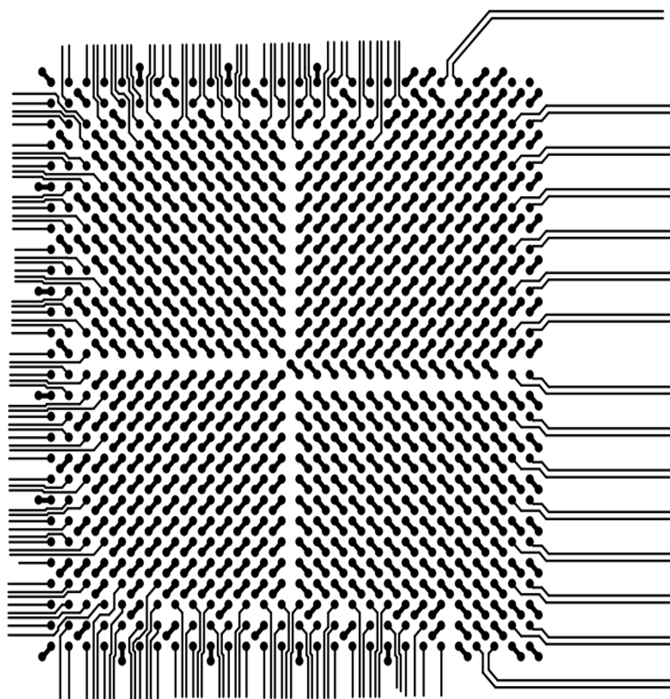


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Figure 8-21. Layer-2, Dual-Trace Breakout (1 mm Pitch)

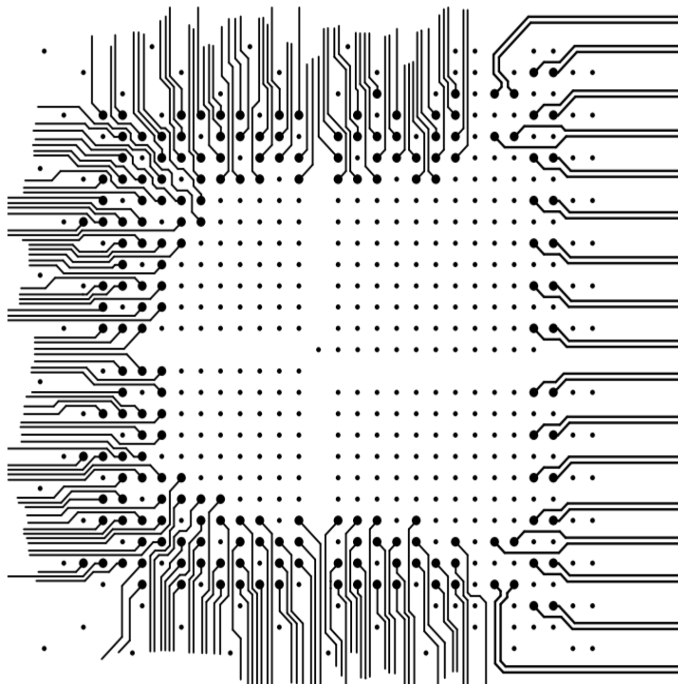
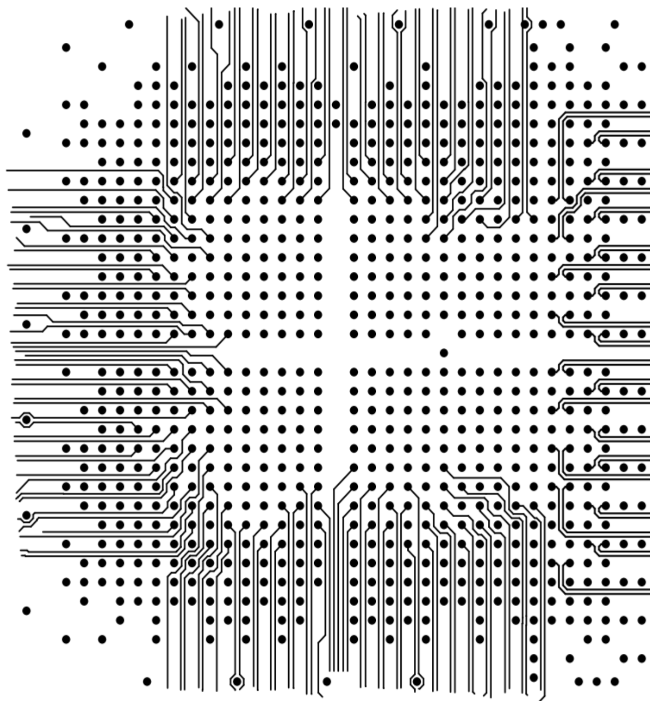


Figure 8-22. Layer-3, Dual-Trace Breakout (1 mm Pitch)



8.5 Single-Trace Breakout for FCG484 (Ask a Question)

The following figures illustrate the single-trace breakout for FCG484.

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Figure 8-23. Layer-1, Single-Trace Breakout (1 mm Pitch)

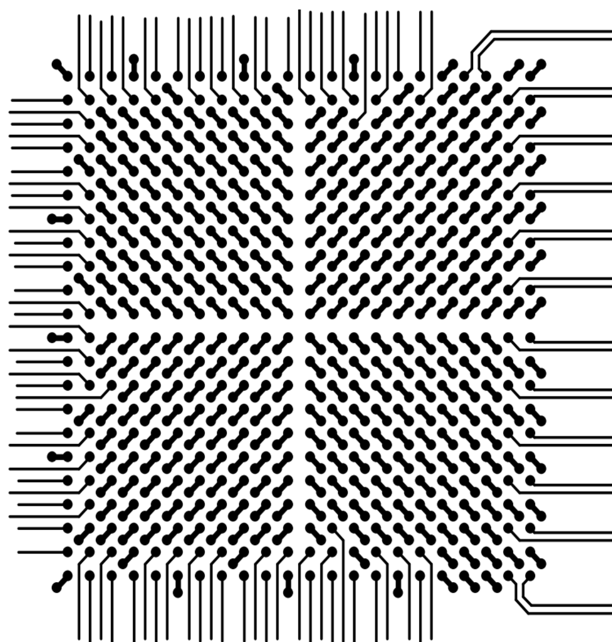

Figure 8-24. Layer-2, Single-Trace Breakout (1 mm Pitch)

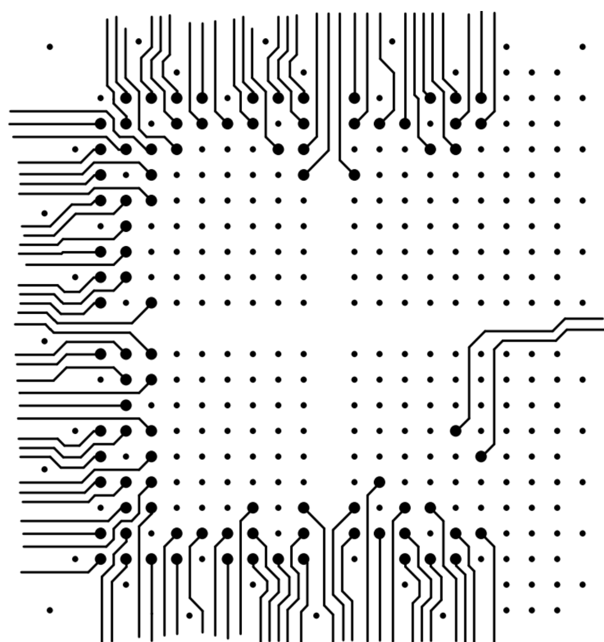

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Figure 8-25. Layer-3, Single-Trace Breakout (1 mm Pitch)

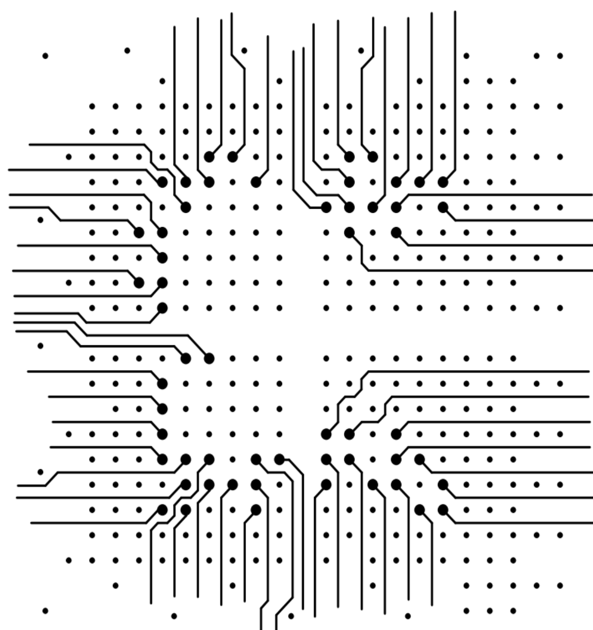
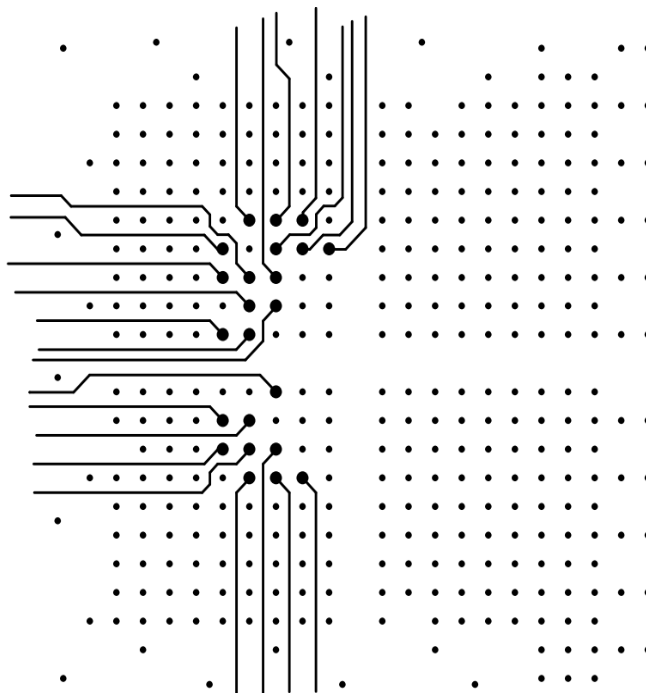


Figure 8-26. Layer-4, Single-Trace Breakout (1 mm Pitch)



8.6 Dual-Trace Breakout for FCG484 (Ask a Question)

The following figures illustrate the dual-trace breakout for FCG484.

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Figure 8-27. Layer-1, Dual-Trace Breakout (1 mm Pitch)

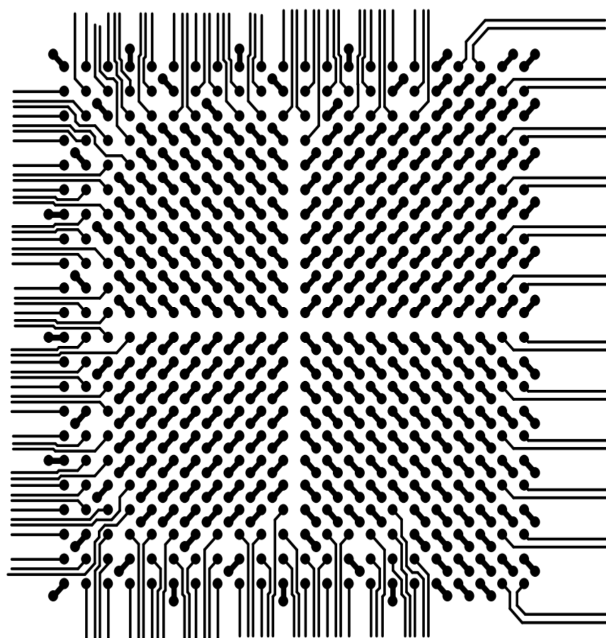
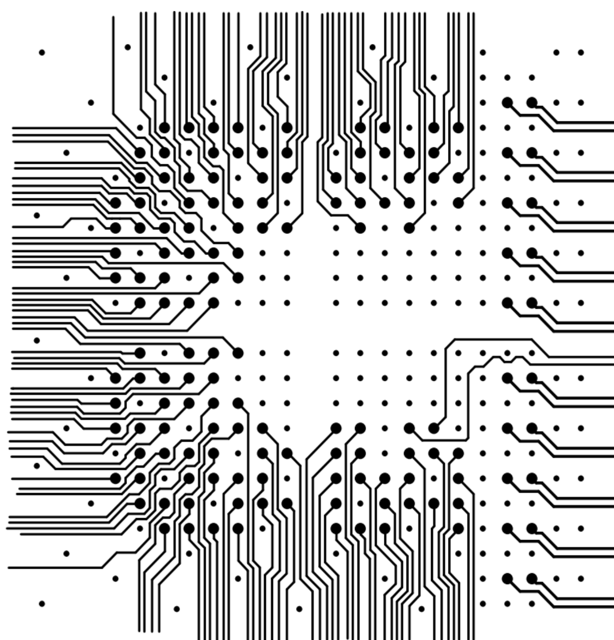


Figure 8-28. Layer-2, Dual-Trace Breakout (1 mm Pitch)



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9. Routing Guidelines for 0.8 mm Package (Ask a Question)

The following figures illustrate the routing guidelines for fabricating 0.8 mm pitch packages, such as FCV484.

Figure 9-1. Single-Trace Breakout Dimensions (mils)

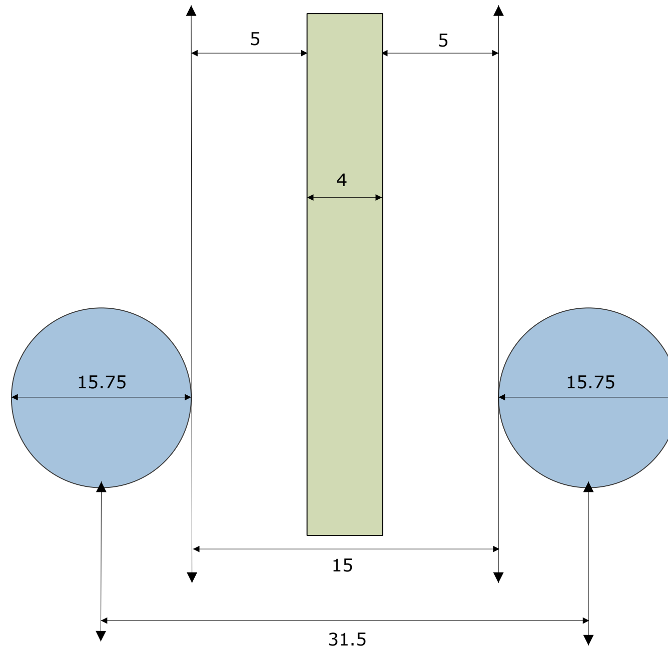

Figure 9-2. Dual-Trace Breakout Dimensions (mils)

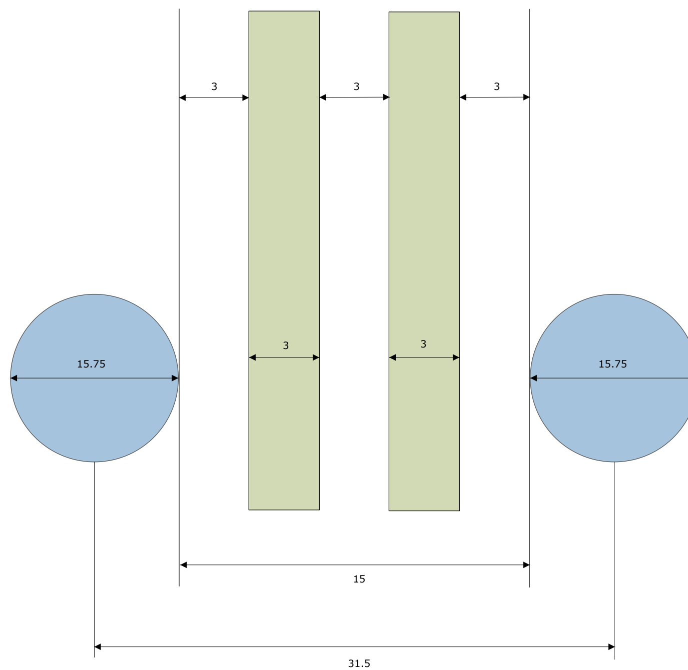

Figure 9-3. Single-Trace Breakout Between Two Vias (mils)

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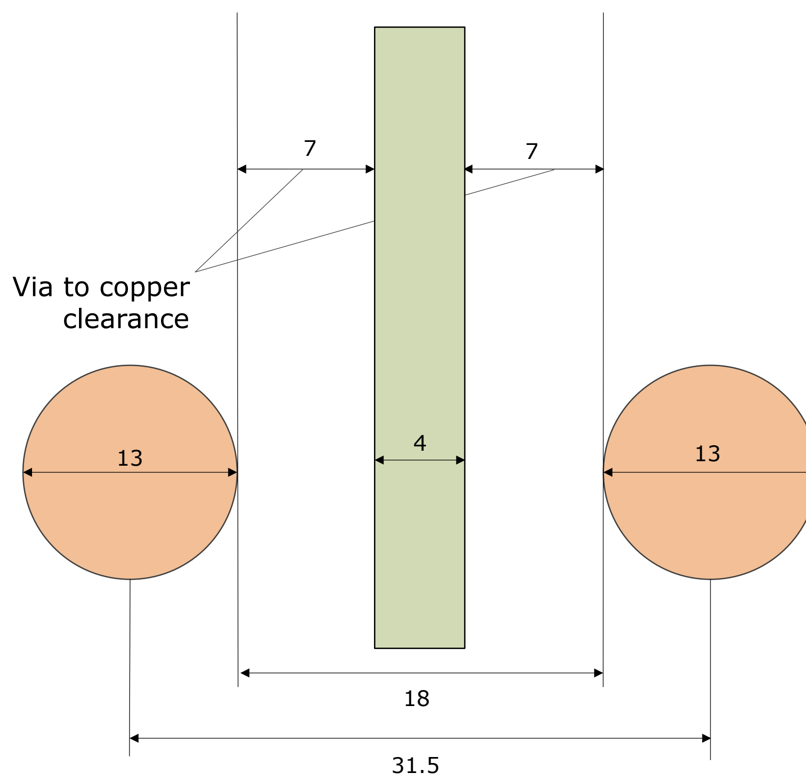

9.1 Single-Trace Breakout for FCV484 (Ask a Question)

The following figures illustrate the single-trace breakout for FCV484.

Figure 9-4. Layer-1, Single-Trace Breakout (0.8 mm Pitch)

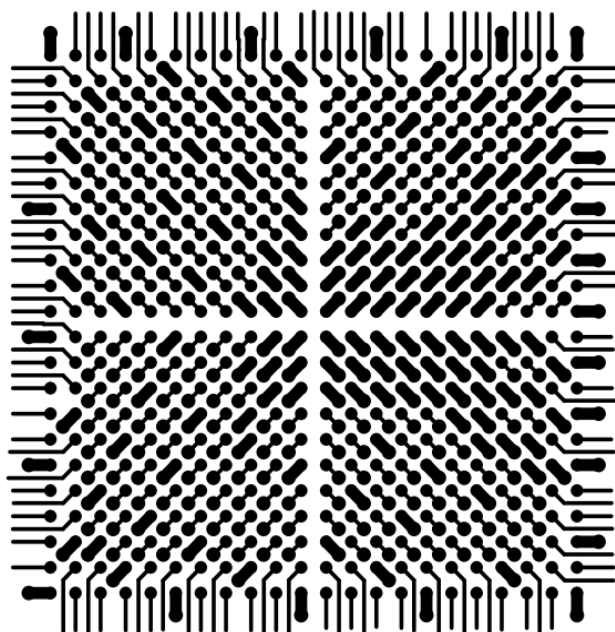

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Figure 9-5. Layer-2, Single-Trace Breakout (0.8 mm Pitch)

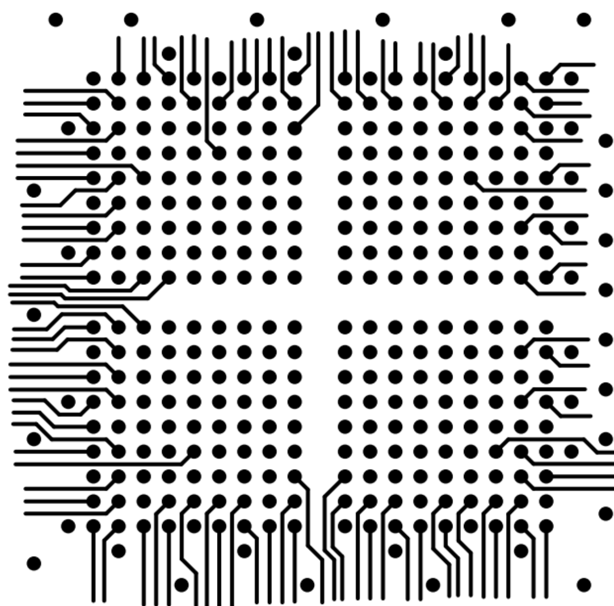

Figure 9-6. Layer-3, Single-Trace Breakout (0.8 mm Pitch)

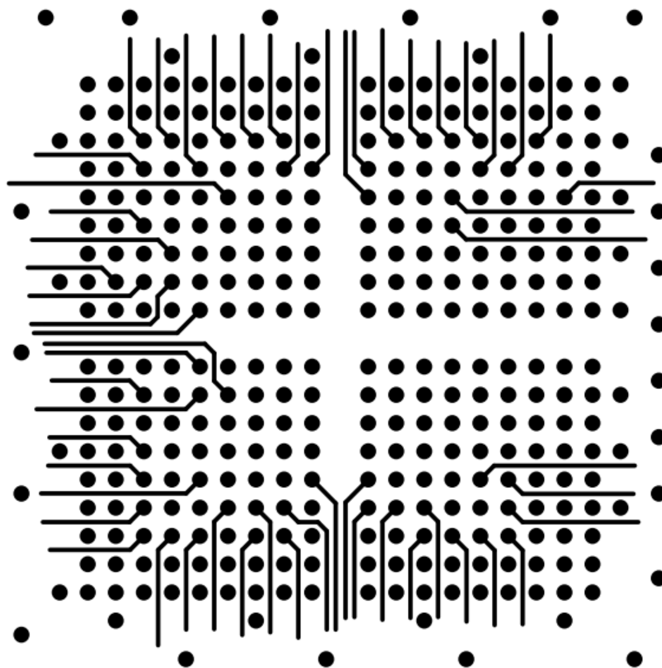

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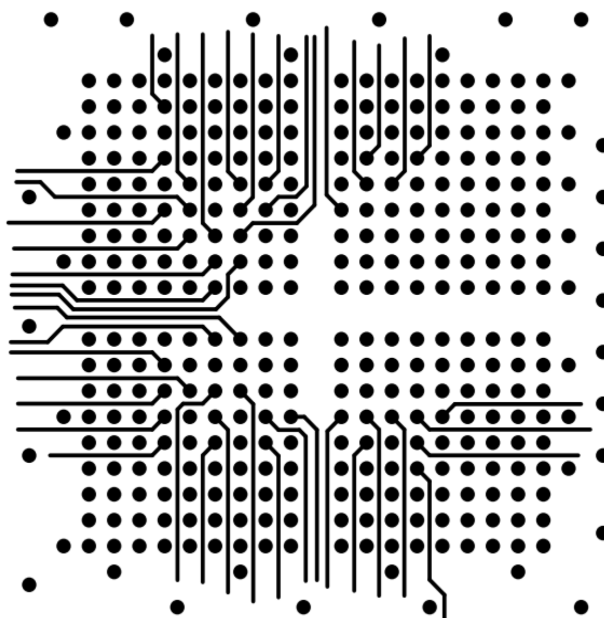
Figure 9-7. Layer-4, Single-Trace Breakout (0.8 mm Pitch)



9.2 Dual-Trace Breakout for FCV484 (Ask a Question)

The following figures illustrate the dual-trace breakout for FCV484.

Figure 9-8. Layer-1, Dual-Trace Breakout (0.8 mm Pitch)

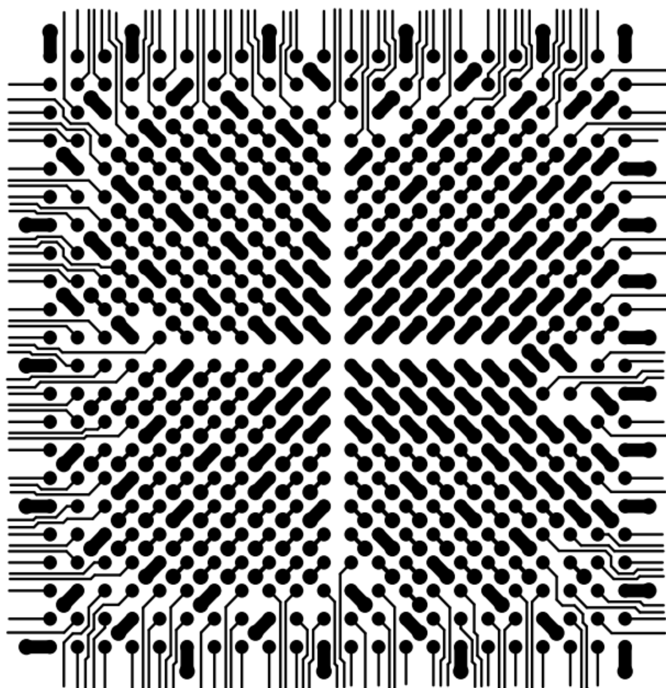


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Figure 9-9. Layer-2, Dual-Trace Breakout (0.8 mm Pitch)

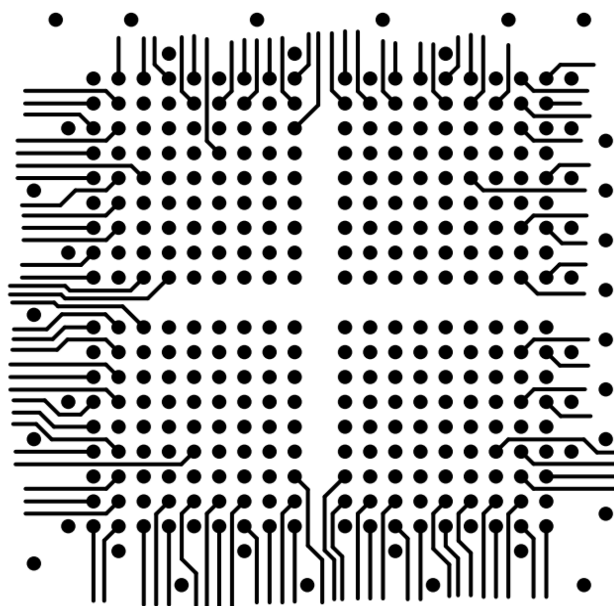
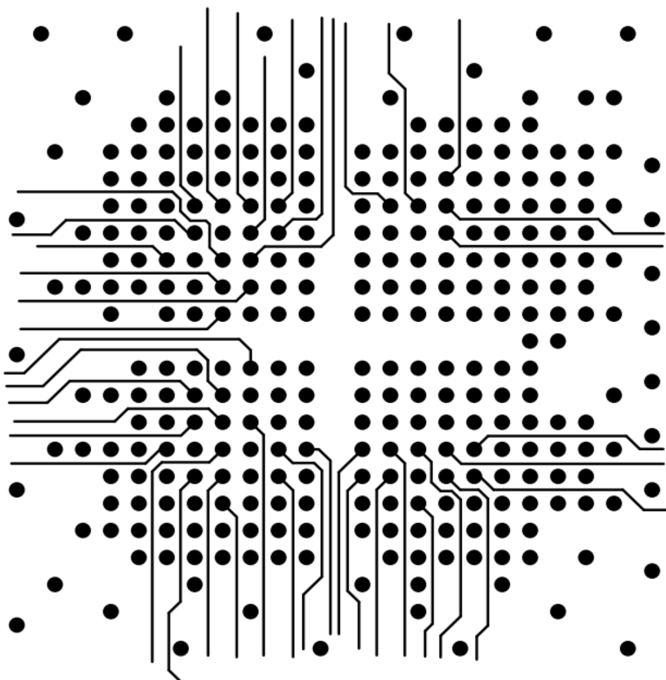


Figure 9-10. Layer-3, Dual-Trace Breakout (0.8 mm Pitch)



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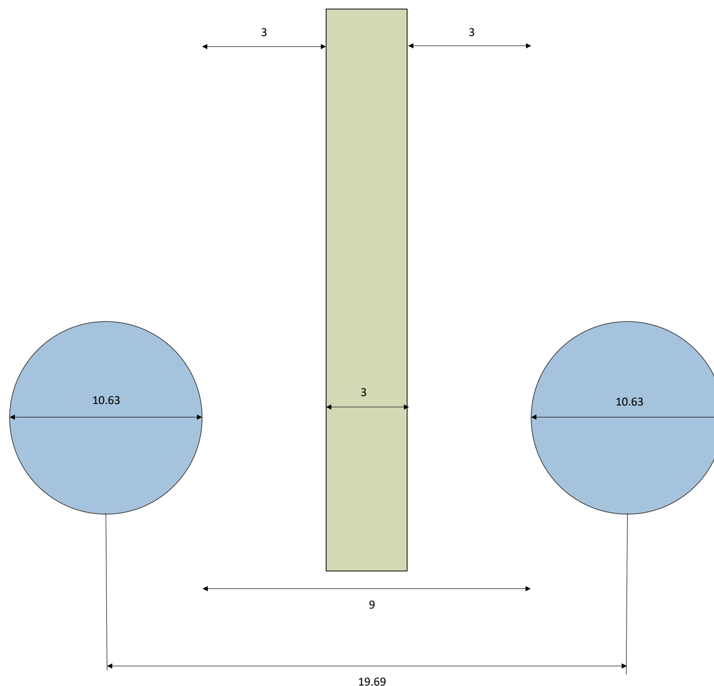
10. Routing Guidelines for 0.5 mm Package (Ask a Question)

The following figures illustrate the routing guidelines for fabricating 0.5 mm pitch packages, such as FCS536.

Figure 10-1. Single-Trace Breakout Dimensions (mils)



10.1 Single-Trace Breakout for FCS536 (Ask a Question)

The following figures illustrate the single-trace breakout for FCS536.

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Figure 10-2. Layer-1, Single-Trace Breakout (0.5 mm Pitch)

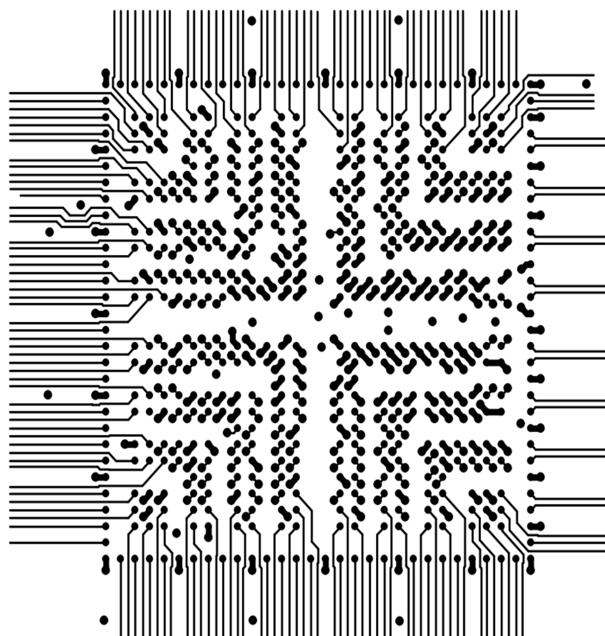

Figure 10-3. Layer-2, Single-Trace Breakout (0.5 mm Pitch)

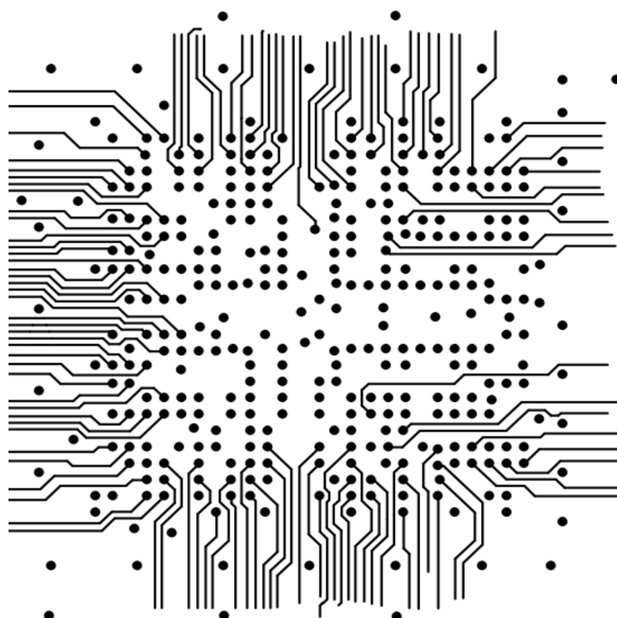

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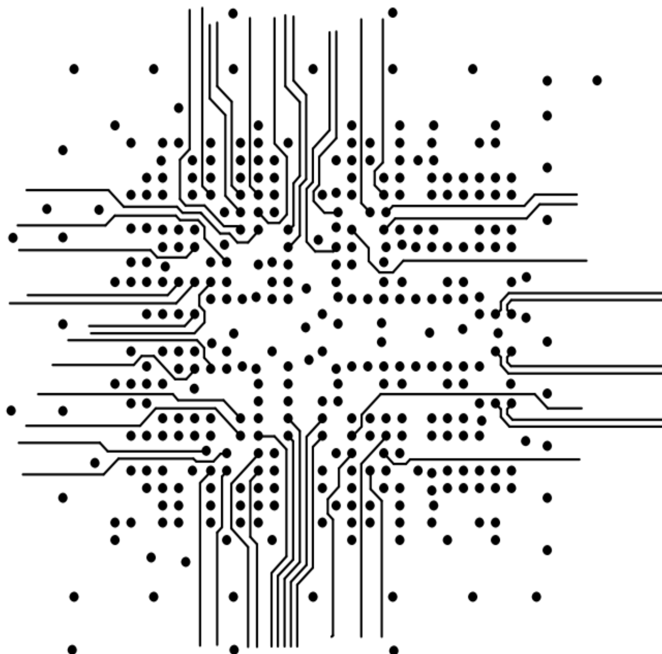
Figure 10-4. Layer-3, Single-Trace Breakout (0.5 mm Pitch)



11. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 11-1. Revision History

Revision	Date	Description
A	11/2024	The following are the changes in the revision A of the document: • The document was migrated to the Microchip template. • The document ID was updated from AC462 to AN5672.
1.0	—	Initial Revision

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