AN5150

Simultaneous Sampling and Conversion using the MCP346X(R) and MCP356X(R) Delta-Sigma ADCs

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INTRODUCTION

Simultaneous sampling and conversion is required for many applications that monitor the instantaneous phase relationship between multiple signals. Such an example is a power metering application that requires instantaneous current and voltage values and the phase relationship between them to calculate parameters such as the power factor or the instantaneous active power.

The simplest solution for this kind of application is to use an Analog-to-Digital Converter (ADC), which offers the ability to synchronously sample and convert multiple signals simultaneously. For example, most devices in the MCP391X family of ADCs provide multiple Delta-Sigma modulators that perform concurrent sampling and conversion of multiple input channels. However, MCP391X ADCs have their own limitations, because they are unable to support a full-scale measurement range greater than 1.2V. For more details, see the data sheets for the MCP391X family of ADCs.

If an application requires simultaneous sampling in addition to a greater full-scale input range, the MCP3461/2/4/5(R) and MCP3561/2/4/5(R) devices are a valid alternative. However, these devices have their own limitations, because their differential input channels are supported using only a single Delta-Sigma modulator and a single front-end multiplexer to switch between conversion channels.

The scope of this Application Note is to explain how multiple MCP3461/2/4/5(R) or MCP3561/2/4/5(R) devices can be operated in parallel to achieve simultaneous sampling and conversion. Additionally, this document outlines other factors that can affect the sampling point of an ADC and how to compensate for them in order to achieve a more precise simultaneous sampling point for each conversion.

Throughout this document, MCP3X6X(R) is used to refer to both MCP3461/2/4/5(R) and MCP3561/2/4/5(R).

HARDWARE CONSIDERATIONS

To achieve simultaneous sampling and conversion across multiple MCP3X6X(R) devices, there are several component, printed circuit board (PCB) and firmware-level attributes that must be considered to ensure synchronization across all ADCs.

Component Considerations

There are several component-level attributes to consider when selecting the devices used in a simultaneous sampling and conversion system. A few examples of component-level considerations include device output impedance, clock jitter and clock source distribution.

CONTROLLABLE CLOCK SOURCE

When using ADCs from the MCP3X6X(R) family in a simultaneous sampling and conversion system, it is required to have a single controllable clock source that is distributable across multiple devices. Two Microchip devices that meet this functional criteria are: PL133-27 1:2 Inverting Fanout Buffer Integrated Circuit (IC) and DSC1121 Low-Jitter Precision MEMS Oscillator.

DSC1121 is a 2.3 MHz to 170 MHz high performance oscillator that utilizes a proven microelectromechanical systems (MEMS) technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. While it can output frequencies up to 170 MHz, the maximum master clock (MCLK) frequency supported by MCP3X6X(R) is 20 MHz. Therefore, the DSC1121 part number used in the proof-of-concept design of this Application Note is the 20 MHz DSC1121CM2-020.0000.

CLOCK SOURCE JITTER

Clock jitter is the deviation of a periodic signal from its ideal reference signal. It is an important specification for timing components as it adversely impacts system performance. Total jitter is comprised of two main types of jitter: random jitter and deterministic jitter.

Random jitter is unpredictable from cycle to cycle and consists mainly of thermal noise, shot noise and flicker noise (also referred to as $1/f$ noise). Random jitter is unbounded as its Gaussian distribution virtually extends indefinitely on both sides of the mean value.

Deterministic jitter is more predictable as it is a repeatable error with well-defined minimum and maximum limits and is typically caused by systematic problems in high-speed digital design. Two components of deterministic jitter are: Duty Cycle Distortion (DCD) and Inter-Symbol Interference (ISI).

While DCD results from differences in the propagation delay between low-to-high and high-to-low signal transitions, ISI occurs when one or more pulses in a digital baseband transmission interfere with subsequent signals. Ultimately, ISI is either caused by improper impedance termination or by bandwidth limitations in the transmitter-receiver or physical media.

Clock jitter is specified using three main metrics:

- **Time Interval Error (TIE) jitter**
  TIE jitter is the absolute difference in the position of an observed clock's edge from its ideal position.
- **Periodic jitter (long-term jitter)**
  Periodic jitter is the difference between any single clock period and the ideal (average) clock period. It is usually specified as a peak-to-peak value. Periodic jitter is important in synchronous systems where the performance is determined by the average clock period.
- **Cycle-to-cycle jitter (short-term jitter)**
  Cycle-to-cycle jitter is the maximum difference between adjacent clock periods and it is also measured as a peak-to-peak value.

Figure 1 shows the different metrics used in defining clock source jitter.

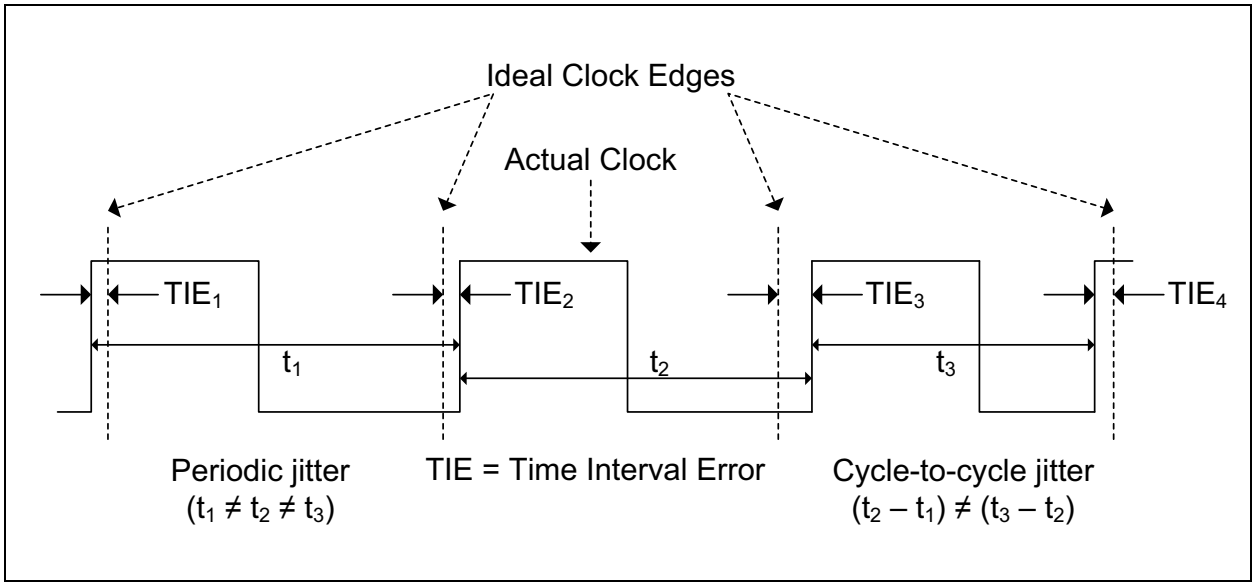

FIGURE 1: *Clock Source Jitter Metrics.*

Jitter is a significant and unwanted source of error that occurs in the design of most communication systems. In time-sensitive applications, such as precision simultaneous sampling and conversion, clock jitter has a significant adverse effect on the signal-to-noise ratio (SNR) and on the effective number of bits (ENOB) of an ADC, as shown in Figure 2.

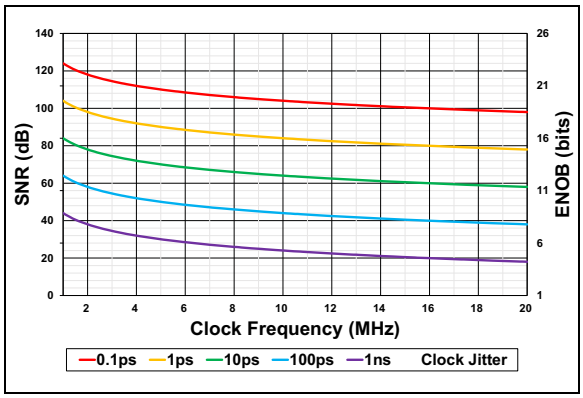

FIGURE 2: *SNR/ENOB vs. Clock Frequency vs. Clock Jitter.*

Clock jitter performance is affected by multiple factors, including, but are not limited to, manufacturing process, temperature, frequency, clock-slew rate, voltage and power supply noise. When reviewing the data sheet of the clock source, exercise due diligence and careful consideration to account not only for the minimum and maximum specifications, but also for the conditions under which these specifications were tested.

The DSC1121 MEMS Oscillator offers less than 2 ps (maximum) and 1 ps (typical) Root Mean Square (RMS) Phase Jitter over a wide range of operating voltages and temperatures, as shown in Figure 3.

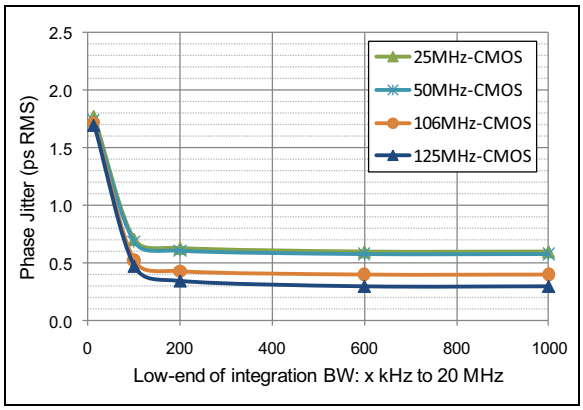

FIGURE 3: *DSC1121 Phase Jitter (Integrated Phase Noise).*

CLOCK SOURCE OUTPUT IMPEDANCE

Clock source output impedance is another component characteristic requiring consideration when designing time-sensitive applications. Generally, a clock source has a low-impedance output to reduce losses at the output stage of the device. If such low-impedance outputs are used to drive loads with higher impedances, an impedance mismatch occurs. As a result of this impedance mismatch, part of the transmitted signal can be reflected backwards through the line trace when the incident (transmitted) signal reaches the end of the line.

When signal reflection occurs, interference in the form of a standing wave happens with higher than normal amplitude. The excessive amplitude of the standing wave can adversely affect system performance and can cause component damage. To compensate for an impedance mismatch, termination of the signal trace is required. Proper termination is achieved by matching the output impedance of the transmitting device to the characteristic impedance of the signal trace. Once the impedance termination value is determined, matching is accomplished by inserting a **resistor** in-line (series) with the signal trace such that the sum of the output impedance of the device and the series termination resistor are approximately equal to the characteristic impedance of the trace.

More details on the termination of signal traces, including proper placement of the termination resistor for best performance, are found in **"Signal Reflections"**.

PCB CONSIDERATIONS

In time-sensitive applications, such as simultaneous sampling and conversion across multiple ADCs, the distribution of a clean clock source can be difficult. Proper design and layout techniques of signal traces become more critical as issues such as crosstalk, attenuation and transmission line effects become more problematic with each signal trace added to the PCB.

Transmission Lines

When the characteristic impedance of a signal trace is small and the trace length (l) is less than one-tenth of the wavelength of the transmitted signal ($l < \lambda/10$), the circuit can be treated as a lumped system. In a lumped system the characteristics of a circuit are considered concentrated into ideal resistive, inductive and capacitive components that are interconnected with perfectly conducting wires of zero impedance.

However, in instances where the physical dimensions of a signal trace are comparable to the wavelength of the transmitted signal, the trace can exhibit characteristics of a distributed transmission line system. In a distributed system, the characteristics of a circuit are viewed as being immeasurably small and distributed continuously along the circuit. In other words, in PCB design, a transmission line is a signal trace composed of a distributed combination of resistance (R), inductance (L) and capacitance (C).

When a device with low output impedance, such as a clock source, transmits a signal over a signal trace that exhibits characteristics of a transmission line, issues such as propagation delay, skew and signal reflection can occur.

PROPAGATION DELAY AND SKEW

Propagation delay is the time needed for a clock signal to traverse a trace. When a single clock source is distributed to multiple devices, but arrives at different time intervals, the paths the signal took to these devices demonstrate different propagation delays.

Skew is a phenomenon that occurs when two signals are expected to arrive at their respective destinations at precisely the same time, but instead have different propagation delays. In time-sensitive applications, like simultaneous sampling and conversion of multiple analog signals, skew is an undesired source of error.

Since no two signal traces are perfectly identical, there is always some amount of variation in the parasitic characteristics of even the most closely matched traces. Mitigating the effects these parasitic variations have on system performance is critical. The trace characteristics that contribute the most to propagation delay and skew are parasitic capacitance and trace length.

Capacitance is inversely proportional to the distance between two parallel conductors. Therefore, by increasing the spacing between adjacent (parallel) signal traces, the amount of parasitic capacitance formed between the signals traces can be mitigated. Increasing the distance between adjacent signal traces has the added benefit of limiting the susceptibility of the system to crosstalk (capacitive-coupling). For more details, see **"Crosstalk"**.

Variation in signal trace length can be just as critical when attempting to preserve the integrity of the transmitted signal(s). To ensure the smallest variation in propagation delay between two signal paths, trace lengths must be matched as closely as possible. Although it is important to keep signal traces as short as possible, it may not be the best solution when attempting to achieve specific design criteria, like avoiding skew. In some cases, to limit the signal skew between the two traces as much as possible, it may be necessary to extend the length of a trace to ensure it matches the length of a similar signal trace.

SIGNAL REFLECTIONS

A standing waveform with excessive amplitude occurs when an impedance mismatch exists between the output stage of a device, such as a clock source, and the characteristics impedance of a signal trace.

There are two worst-case scenarios for an impedance mismatch that can occur:

- An open-circuit resulting in an infinite impedance.
- A short-circuit resulting in zero impedance.

Both scenarios represent absolute discontinuity in the PCB trace and cause total signal reflection.

The relationship between the output impedance of a device and the characteristic impedance of a transmission line is expressed as a dimensionless quantity known as the reflection coefficient (Γ). The reflection coefficient is defined as the ratio of the reflected wave amplitude over the incident wave amplitude and it is calculated as shown in Equation 1.

EQUATION 1:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Where:

- Γ = Reflection Coefficient
- Z_L = Source Output Impedance (Ω)
- Z_0 = Transmission Line Characteristic Impedance (Ω)

When applying Equation 1 to the open-circuit and short-circuit worst-case scenarios, the reflection coefficient is respectively $\Gamma = +1$ and $\Gamma = -1$. A reflection coefficient of +1 or –1 indicates total reflection of the incident wave at the boundary where the impedance changes, causing the incident wave to travel back towards the source. A reflection coefficient of 0, however, indicates the impedance at the source has the same value as the characteristic impedance of the transmission line; therefore no signal reflection occurs.

Figure 4 illustrates what happens when a clock signal (incident waveform) is transmitted along a transmission line exhibiting impedance mismatching. If impedance mismatching exists between the output impedance of the clock source and the load impedance of the transmission line signal, then reflections occur and cause the incident waveform to be reflected back through the transmission line. As a result, the incident and reflected waveforms end up passing each other on the transmission line causing interference in the form of a standing waveform. The standing waveform is the sum of the incident and reflected waveforms that can result in line voltages exceeding (overshoot and undershoot) the voltage levels of the original transmitted signal.

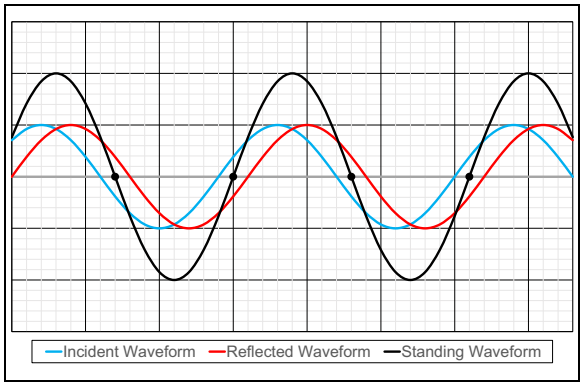

FIGURE 4: *Incident, Reflected and Standing Waveforms.*

Signal reflections affect signal integrity and can lead to system failure or even damage to the output or input stages of devices. For this reason, best performance is achieved when signal traces are as short as possible, except when trace lengths need to be matched to avoid issues such as clock skew.

CHARACTERISTIC IMPEDANCE, INDUCTANCE AND CAPACITANCE

When trace lengths are comparable to the wavelength of the signal being transmitted, a signal trace begins to exhibit characteristics similar to a transmission line with a distributed combination of resistance (R), inductance (L) and capacitance (C). The wavelength of the transmitted signal is determined using Equation 2.

EQUATION 2:

$$\lambda = \frac{v_p}{f}$$

Where:

λ = Signal Wavelength (m)
v_p = Signal Propagation Velocity (m/s)
f = Signal Frequency (Hz)

The wavelength of a signal sent along a transmission line is dependent on its propagation velocity (v_p). In turn, the propagation velocity is dependent on the architecture of the signal trace and the PCB design.

In PCB design, there are two primary layout techniques used in the construction of a signal trace: microstrip and stripline. The microstrip layout method has the trace conductor isolated from a single ground plane by a dielectric material, whereas the stripline method has the trace conductor embedded in a dielectric material wedged between two reference planes (usually ground planes). Figure 5 shows the two layout methods.

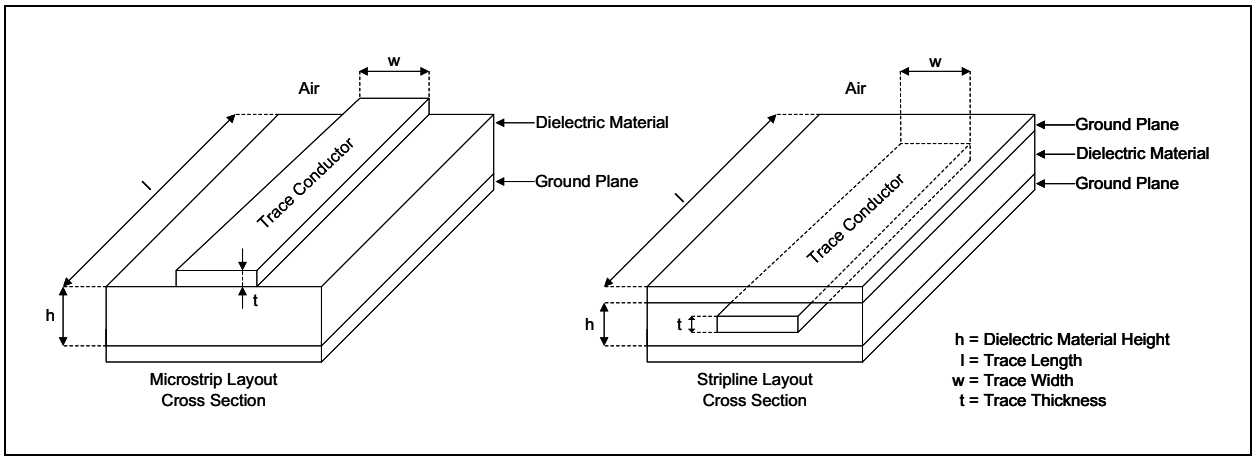

FIGURE 5: *Cross Section of Microstrip and Stripline Layout Techniques.*

The propagation velocity of a signal as it traverses a transmission line is a function of the permittivity and permeability of the dielectric material surrounding the trace conductor. For a stripline trace, the propagation velocity is calculated using Equation 3, where ε_r is the relative permittivity of the dielectric substrate in which the trace is fabricated.

EQUATION 3:

$$v_p = \frac{c}{\sqrt{\varepsilon_r}}$$

Where:

- v_p = Signal Propagation Velocity (m/s)
- c = Speed of Light in Vacuum (≈ 3×10^8 m/s)
- ε_r = Relative Permittivity

For a microstrip trace, the propagation velocity calculation is more complex as the trace is not surrounded by a single dielectric substrate. To determine an effective relative permittivity (ε_e), consider both the permittivity constant of the air above the trace and the permittivity constant of the dielectric material on which the trace is fabricated.

Substituting ε_e for ε_r in Equation 3 results in an equation for the propagation velocity of a signal transmitted across a microstrip trace, as shown in Equation 4.

The effective relative permittivity of the dielectric (ε_e) is calculated using Equation 5. In practice, the microstrip thickness (t) is considerably smaller than the width of the trace (w) or the height of the dielectric substrate (h) and, therefore, Equation 5 assumes that $t \cong 0$.

EQUATION 4:

$$v_p = \frac{c}{\sqrt{\varepsilon_e}}$$

Where:

- v_p = Signal Propagation Velocity (m/s)
- c = Speed of Light in Vacuum (m/s)
- ε_e = Effective Relative Permittivity

EQUATION 5:

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \cdot \left(1 + 10\frac{h}{w}\right)^{-a \cdot b}$$

Where:

- ε_e = Effective Relative Permittivity
- ε_r = Relative Permittivity (Dielectric Substrate)
- h = Dielectric Material Height (m)
- w = Trace Width (m)

and:

$$a\left(\frac{w}{h}\right) = 1 + \frac{1}{49} \cdot \ln\left[\frac{\left(\frac{w}{h}\right)^4 + \left(\frac{w}{52h}\right)^2}{\left(\frac{w}{h}\right)^4 + 0.432}\right] + \frac{1}{18.7} \cdot \ln\left[1 + \left(\frac{w}{18.1h}\right)^3\right]$$

$$b(\varepsilon_r) = 0564 \cdot \left(\frac{\varepsilon_r - 0.9}{\varepsilon_r + 3}\right)^{0.053}$$

A common dielectric material for PCBs is FR-4 due to its versatile high-pressure thermoset plastic laminate grade and good strength-to-weight ratios with near-zero water absorption. The relative permittivity of the FR-4 dielectric ranges from 3.8 to 4.8, depending on the glass weave style, thickness, resin content and copper foil roughness.

Once the effective relative permittivity (ε_e) is determined using Equation 5, the characteristic impedance (Z_0) of a microstrip trace of height h and width w is calculated using Equation 6, where the relative permittivity of free-space (air) is $\varepsilon_r = 1$. The characteristic impedance of air ($Z_0|_{air}$) is calculated using Equation 7.

If $0.01 \leq w/h \leq 100$ and $1 \leq \varepsilon_r \leq 128$, the precision of Equation 5 is better than 0.2%, whereas Equation 7 and consequently Equation 6 have a precision better than 0.1% when $w/h < 1000$. Note that Equation 7 results in a maximum characteristic impedance when the trace width (w) is minimized.

EQUATION 6:

$$Z_0 = \frac{Z_0|_{air}}{\sqrt{\varepsilon_e}}$$

Where:

Z_0 = Characteristic Impedance (Ω)

$Z_0|_{air}$ = Characteristic Impedance in Free-space (Ω)

ε_e = Effective Relative Permittivity

EQUATION 7:

$$Z_0|_{air} = Z_0|_{(\varepsilon_r = 1)} = 60 \cdot \ln\left[\frac{f_1 \cdot h}{w} + \sqrt{1 + \left(\frac{2h}{w}\right)^2}\right]$$

Where:

$Z_0|_{air}$ = Characteristic Impedance in Free-space (Ω)

ε_r = Relative Permittivity of Free-space (air)

h = Dielectric Material Height (m)

w = Trace Width (m)

and:

$$f_1 = 6 + (2\pi - 6) \cdot e^{-\left(\frac{30.666h}{w}\right)^{0.7528}}$$

DISTORTION AND TERMINATION

When the characteristic impedance (Z_0) of a transmission line is determined, proper termination is achieved by way of an in-line resistor to ensure the best possible waveform is available at the end of the trace.

Typically, a series termination resistor is sufficient if its resistance matches the characteristic impedance of the transmission line to within ±10% of the characteristic output impedance of the clock generator. For best signal quality at the receiver (end of the trace), the termination resistor is typically placed at the beginning of the trace, between the output of the clock generator and the start of the trace, as shown in Figure 6.

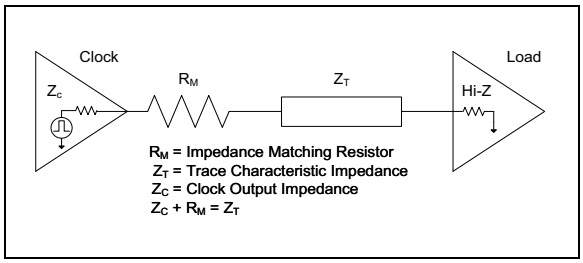

FIGURE 6: *Impedance Matching Termination Resistor.*

Consider the following example: a transmission line with a characteristic impedance (Z_0) of 50Ω and the output impedance (Z_L) of a CMOS buffer of 10Ω (as found on the DSC1121). To properly match the output impedance of the DSC1121 to the characteristic impedance of the transmission line, a series termination resistor of 40Ω is placed between the output of the clock generator and the start of the signal trace.

Figure 7 shows how a transmitted clock signal looks at various points along the trace. The main concern is how the signal looks at the end of the transmission line, at the receiver input. There are significant reflections at all points along the trace, except at the end where it is most critical. The scope capture at the trace end shows a transmission line that is adequately terminated by matching the output impedance (Z_L) of the clock source (CMOS output) to the characteristic impedance (Z_0) of the transmission line.

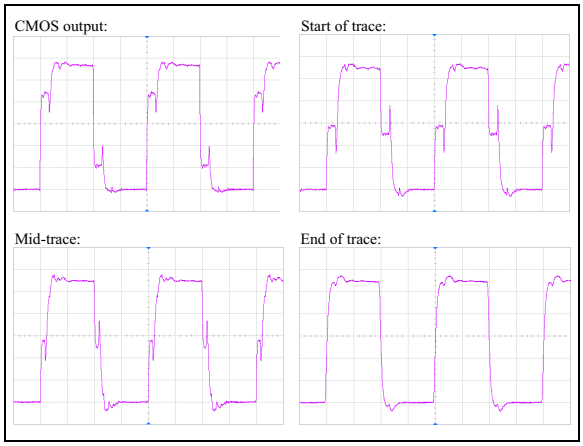

FIGURE 7: *Trace Location Captures.*

Crosstalk

Crosstalk occurs when a signal transmitted on one conductor causes an unwanted effect on a nearby or adjacent conductor by way of electrical interference. When the electromagnetic fields generated by two adjacent conductors overlap each other, the integrity of the signals transmitted on both conductors is affected. Two common forms of crosstalk are capacitive coupling and inductive coupling.

To suppress the effects of crosstalk on clock signal transmission lines, use the following layout techniques:

1. Use point-to-point connections. In other words, a single clock output connected to a single clock input.
2. Keep clock traces as straight as possible:
   - If trace bending is necessary, use 45° (or 135°) trace angles or curved angles. Do not use 90° trace angles. See Figure 8.

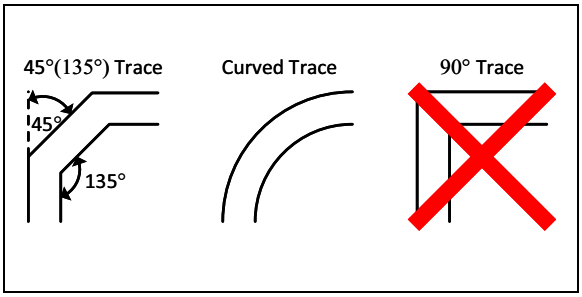

FIGURE 8: *Trace Layout Techniques.*

   - In some cases, it may be necessary to extend the trace lengths and/or use a zigzag layout to achieve a specific characteristic impedance for the transmission line.
3. Careful attention to the trace geometry: width, height and dielectric thickness (trace-to-ground distance), can minimize crosstalk by controlling the trace impedance, capacitance and inductance.
4. Do not use vias in the clock signal path as they increase parasitic impedance, inductance and capacitance. They also cause signal reflection.
5. Separate adjacent conductors by two to three times the trace width. This reduces the potential of mutual interference by up to 70%.
6. Insert a ground plane between adjacent signal layers to reduce the possibility of broadside coupling that occurs between traces running parallel to each other on separate, but adjacent, PCB layers.
7. Route traces on adjacent board layers in a crosshatch pattern: vertically on one layer, then horizontally on the adjacent layer.

Following is an example of how to calculate the parasitic capacitance and inductance of a microstrip transmission line. It is assumed the characteristic impedance (Z_0) and effective relative permittivity (ε_e) are already calculated using the equations found in **"Transmission Lines"**. The parasitic capacitance and inductance are expressed in terms of per-unit-length. Therefore, an equation for the time a signal (voltage change) takes to travel a unit-length, is required. Equation 8 defines the propagation velocity (v_p) of a signal through a transmission line of unit-length.

EQUATION 8:

$$v_p = \frac{1}{\sqrt{L \cdot C}}$$

Where:

v_p = Signal Propagation velocity (m/s)
L = Per-unit-length Inductance (H)
C = Per-unit-length Capacitance (F)

Since the dielectric properties of a medium have negligible impact on the parasitic inductance, it can be assumed the transmission line is surrounded by a medium of free-space (air). The propagation velocity of a signal through a microstrip transmission line is expressed by Equation 9.

EQUATION 9:

$$v_p\big|_{air} = c = \frac{1}{\sqrt{L \cdot C_{air}}}$$

Where:

- $v_p|_{air}$ = Propagation Velocity through Air (m/s)
- c = Speed of Light in Vacuum (≈ 3×10^8 m/s)
- L = Per-unit-length Inductance (H)
- C_{air} = Capacitance in Free-space (F)

Equation 9 can be solved for the per-unit-length inductance (L) in free-space (and dielectric medium) in terms of the per-unit-length capacitance (C) as shown in Equation 10.

EQUATION 10:

$$L = \frac{1}{C_{air} \cdot c^2} = \frac{1}{C \cdot c^2}$$

Where:

- L = Per-unit-length Inductance (H)
- C_{air} = Capacitance in Free-space (F)
- c = Speed of Light in Vacuum (≈ 3×10^8 m/s)
- C = Per-unit-length Capacitance (F)

Since the effective relative permittivity (ε_e) can be defined as the ratio of a capacitance with material dielectric (C) to a capacitance with free-space dielectric (C_{air}), the effective relative permittivity is expressed as shown in Equation 11.

EQUATION 11:

$$\varepsilon_e = \frac{C}{C_{air}}$$

Where:

- ε_e = Effective Relative Permittivity
- C = Per-unit-length Capacitance (F)
- C_{air} = Capacitance in Free-space Dielectric (F)

Equation 12 shows the reduced approximation for the characteristic impedance (Z_0) of a low-loss microstrip transmission line expressed in terms of per-unit-length inductance (L) and per-unit-length capacitance (C).

EQUATION 12:

$$Z_0 = \sqrt{\frac{L}{C}}$$

Where:

- Z_0 = Characteristic Impedance (Ω)
- L = Per-unit-length Inductance (H)
- C = Per-unit-length Capacitance (F)

Rearranging Equation 11 and substituting the capacitance in free-space (C_{air}) and the per-unit-length inductance (L) of Equation 10 into Equation 12, the per-unit-length capacitance (C) can be determined as shown in Equation 13.

EQUATION 13:

$$C = \frac{\sqrt{\varepsilon_e}}{Z_0 \cdot c}$$

Where:

- C = Per-unit-length Capacitance (F)
- ε_e = Effective Relative Permittivity
- Z_0 = Characteristic Impedance (Ω)
- c = Speed of Light in Vacuum (≈ 3×10^8 m/s)

Alternatively, since Equation 4 and Equation 8 both represent the propagation velocity (v_p) of a signal in a microstrip transmission line, they can be equated to derive the equation for the per-unit-length capacitance (C) in terms of the per-unit-length inductance (L) and the effective relative permittivity (ε_e), as shown in Equation 14.

EQUATION 14:

$$C = \frac{\varepsilon_e}{L \cdot c^2}$$

Where:

- C = Per-unit-length Capacitance (F)
- ε_e = Effective Relative Permittivity
- L = Per-unit-length Inductance (H)
- c = Speed of Light in Vacuum (≈ 3×10^8 m/s)

Finally, substituting Equation 14 into Equation 12, the per-unit-length inductance (L) can be determined as shown in Equation 15.

EQUATION 15:

$$L = \sqrt{\varepsilon_e} \cdot \frac{Z_0}{c}$$

Where:

- L = Per-unit-length Inductance (H)
- ε_e = Effective Relative Permittivity
- Z_0 = Characteristic Impedance (Ω)
- c = Speed of Light in Vacuum (≈ 3×10^8 m/s)

As previously stated, inductive coupling is a form of crosstalk that adversely affects the quality of signals being transmitted along a PCB. Therefore, minimizing the amount of parasitic inductance intrinsic to a PCB trace is an important factor in limiting its susceptibility to crosstalk.

Considering Equation 15 together with Equation 5, Equation 6 and Equation 7 shows the parasitic inductance of a PCB trace has an underlying dependence on its width-to-height (w/h) ratio. Assuming the height is a known specified design parameter, Figure 9 shows that for a specified characteristic impedance (Z_0), there is a specific width that results in a minimized per-unit-length trace inductance (L).

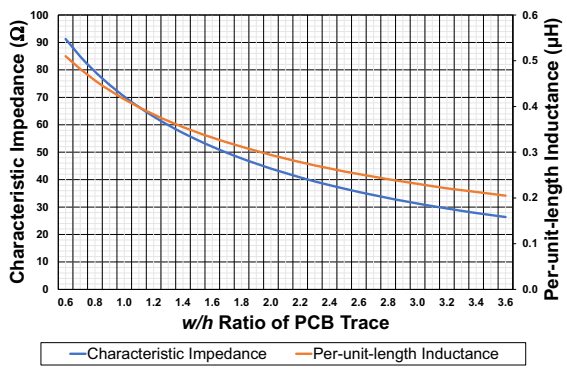

FIGURE 9: *Impedance vs w/h vs Inductance.*

Since the damping factor (ζ) of any ringing transient signal is inversely proportional to the inductance of the circuit (inter-connection), as shown in Equation 16, the importance of minimizing the per-unit-length inductance (L) of any PCB trace used in time-critical systems is clear.

EQUATION 16:

$$\zeta = \frac{\alpha}{\omega_0} = \frac{R}{2} \cdot \sqrt{\frac{C}{L}}$$

Where:

- ζ = Damping Factor
- α = Damping Attenuation (Np/s)
- ω_0 = Resonant Frequency of RLC Circuit (Hz)
- R = Resistance (Ω)
- C = Per-unit-length Capacitance (F)
- L = Per-unit-length Inductance (H)

FIRMWARE CONSIDERATIONS

The final consideration for simultaneous sampling and conversion systems are the requirements the hardware places on the architecture and code sequencing of the firmware.

Since only a single MCP3X6X(R) device can communicate on the SPI bus at a time, a means to synchronize the start-of-conversion across multiple devices is required. For the MCP3X6X(R) family of devices, synchronization is achieved through control of the conversion clock (MCLK) source.

To ensure proper synchronization, the conversion clock of all devices must be held idle while each device in the system is sequentially configured for the desired mode of operation.

Once all devices are configured and ready to begin conversion, a start-of-conversion command by way of the Conversion-Start/Restart Fast-CMD (or a direct write of the ADCMODE[1:0] bits) can be executed for each device. With the MCLK source held idle during the initiation of the conversion command, no conversion sequence can be executed; this is the key to synchronizing multiple devices for simultaneous sampling and conversion.

The MCLK conversion clock must be made active to begin the conversion process only once a conversion command is initiated for each device. Figure 10 shows the complete sequence of SPI bus activity required to achieve simultaneous sampling and conversion of two ADCs operating in parallel (simultaneously).

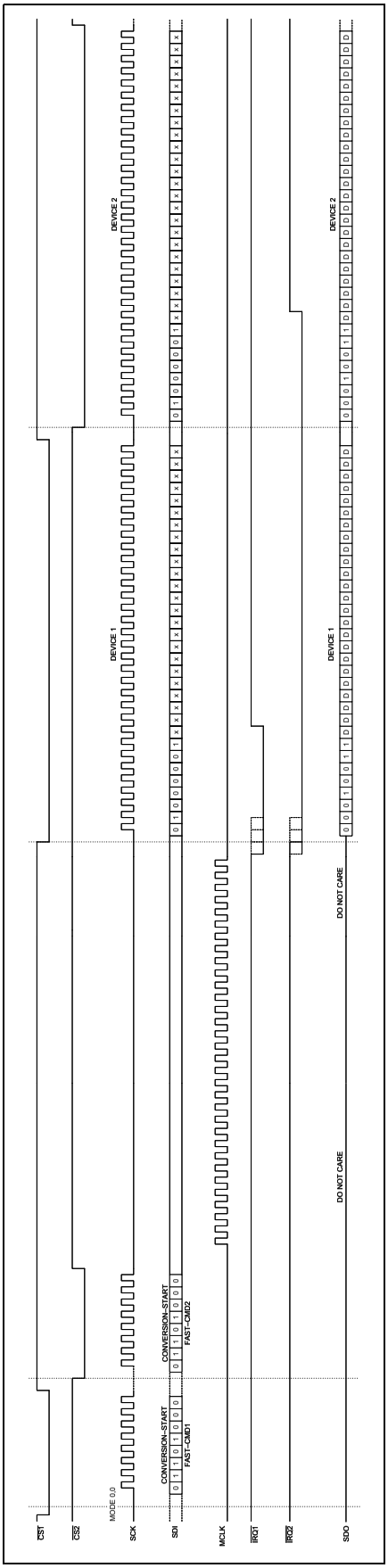

FIGURE 10: *SPI Command Sequence for Parallel ADC Devices.*

CONCLUSION

Simultaneous sampling and conversion is a requirement for many applications that need to monitor the instantaneous phase relationship between multiple signals. For ADCs such as the MCP391X family of dual channel Analog-Front-End (AFE), simultaneous sampling and conversion is easily achieved due to the multiple Delta-Sigma modulators present in the device. For devices such as the MCP3X6X(R) family of Delta-Sigma ADCs that offer only a single Delta-Sigma modulator, simultaneous sampling and conversion can be problematic. To achieve simultaneous sampling and conversion using the MCP3X6X(R) devices, alternative means must be implemented, such as operating multiple ADCs in parallel.

When attempting to design a simultaneous sampling and conversion system using multiple ADCs, there are several component, PCB and firmware-level attributes that need to be considered to ensure a precise simultaneous sampling point of all devices in the system. Attributes such as:

- Component output impedance and jitter.
- Parasitic PCB elements that include impedance, inductance and capacitance.
- Firmware control and sequencing of component operation.

Through careful consideration and control of these attributes, the best possible performance of the simultaneous sampling and conversion system can be achieved.

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NOTES:

APPENDIX A: REVISION HISTORY

Revision B (August 2024)

The following is a list of modifications:

- Updated Figure 8.

Revision A (October 2023)

- Initial release of this document.

NOTES:

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