MICROCHIP

# Section 9. Watchdog Timer (WDT) and Power-Saving Modes

## HIGHLIGHTS

This section of the manual contains the following major topics:


9.1 Introduction .......... 9-2
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| **Note:** | This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33F/PIC24H devices.<br>Please consult the note at the beginning of the **"Special Features"** and **"Power-Saving Features"** chapters in the current device data sheet to check whether this document supports the device you are using.<br>Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com |
|---|---|

# 9.1 INTRODUCTION

This section describes the Watchdog Timer (WDT) and power-saving modes implemented in the dsPIC33F/PIC24H devices. The dsPIC33F/PIC24H device family offers a number of built-in capabilities that permit user-assigned applications to select the best balance of performance and low-power consumption.

The WDT resets the device in the event of a software malfunction. It can also be used to wake the device from Sleep or Idle mode.

# 9.2 POWER-SAVING MODES

Power-saving features implemented in dsPIC33F/PIC24H devices include the following:

- System Clock Management
- Instruction-Based Power-Saving Modes
- Hardware-Based Doze Mode
- Peripheral Module Disable

## 9.2.1 System Clock Management

Reducing the system clock frequency results in power-saving that is roughly proportional to the frequency reduction. The dsPIC33F/PIC24H devices provide an on-the-fly clock switching feature that allows the user-assigned application to optimize power consumption by dynamically changing the system clock frequency. For more information, refer to **Section 7. "Oscillator"** (DS70186).

## 9.2.2 Instruction-Based Power-Saving Modes

The dsPIC33F/PIC24H devices have two instruction based power-saving modes. These modes can be entered by executing a special `PWRSAV` instruction. If an interrupt coincides with the execution of a `PWRSAV` instruction, the interrupt is delayed until the device fully enters Sleep or Idle mode. If the interrupt is a wake-up event, it will then wake-up the device and execute.

- **Sleep Mode:** In Sleep mode, the CPU, the system clock source, and the peripherals that operate on the system clock source are disabled. This is the lowest power mode for the device. The wake-up from Sleep Flag Status bit (SLEEP) in the Reset Control register (RCON<3>) is set when the device enters Sleep mode.
- **Idle Mode:** In Idle mode, the CPU is disabled, but the system clock source continues to operate. The peripherals continue to operate but can optionally be disabled. The wake-up from Idle Flag Status bit, IDLE (RCON<2>), is set when the device enters Idle mode.

The SLEEP status bit (RCON<3>) and the IDLE status bit (RCON<2>) are cleared on Power-on Reset (POR) and Brown-out Reset (BOR). These bits can also be cleared in the user application. For more information, refer to **Section 8. "Reset"** (DS70192).

The assembly syntax of the PWRSAV instruction is shown in Example 9-1.

**Example 9-1: PWRSAV Assembly Syntax**

```
PWRSAV #SLEEP_MODE   ; Put the device into SLEEP mode
PWRSAV #IDLE_MODE    ; Put the device into IDLE mode
```

> **Note 1:** SLEEP_MODE and IDLE_MODE are constants defined in the assembler include file for the selected device.
>
> **2:** Sleep mode does not change the state of the I/O pins.

#### 9.2.2.1 SLEEP MODE

Sleep mode is the lowest current consumption state. The characteristics of Sleep mode include the following:

- The Primary Oscillator (POSC) and Internal Fast RC (FRC) Oscillator are disabled
- The Secondary Oscillator (SOSC) continues to run, if the Secondary Oscillator Enable bit (LPOSCEN) in the Oscillator Control register (OSCCON<1>) is set. For more information, refer to **Section 7. "Oscillator"** (DS70186).
- The WDT and the clock source Internal Low-power RC (LPRC) oscillator continue to run, if the WDT is enabled. For more information, refer to **9.3 "Watchdog Timer (WDT)"**.
- If the Voltage Regulator Standby During Sleep bit (VREGS) is cleared in the Reset Control register (RCON<8>), the internal voltage regulator enters the stand-by state. The voltage regulator consumes less current when in the stand-by state.
- The peripherals operating with the system clock are disabled
- The Fail-safe Clock Monitor (FSCM) does not operate during Sleep mode, because the system clock is disabled

To minimize the current consumption in Sleep mode, perform the following:

- Ensure that I/O pins do not drive resistive loads
- Ensure that I/O pins configured as inputs are not floating
- Disable the SOSC
- Disable the WDT
- Enable the voltage regulator to enter standby state in Sleep mode

When the device exits Sleep mode, it restarts with the current clock source as indicated by the Current Oscillator Selection bits (COSC<2:0>) in the Oscillator Control register (OSCCON<14:12>).

##### 9.2.2.1.1 Delay on Wake-up from Sleep Mode

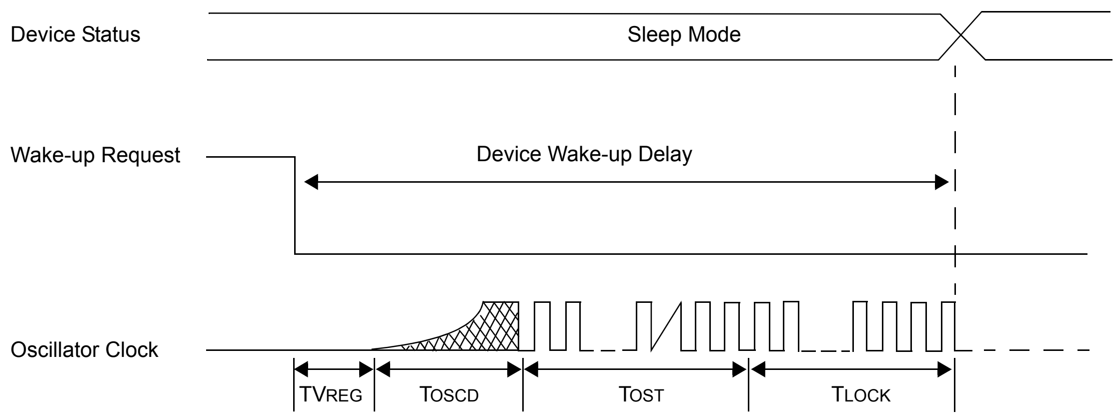
Figure 9-1 illustrates the wake-up delay from Sleep mode. This delay consists of the voltage regulator delay and the oscillator delay.

- Voltage Regulator Delay: The time delay for the voltage regulator to transit from the standby state to active state. This delay is required only if Standby mode is enabled for the voltage regulator.
- Oscillator Delay: The time delay for the clock to be ready for various clock sources, as provided in Table 9-1. For more information, refer to **Section 7. "Oscillator"** (DS70186).



**Figure 9-1: Wake-up Delay from Sleep Mode**




**Where:**

TVREG = Voltage regulator standby to Active mode transition time (130 ms nominal)
TOSCD = Oscillator start-up delay (FRC = 1.1 ms nominal; LPRC = 70 ms nominal)
TOST = Oscillator start-up timer delay (1024 oscillator clock period)
TLOCK = PLL lock time (1 ms nominal), if PLL is enabled

**Table 9-1: Oscillator Delay[1,2,3]**

| Oscillator Source | Oscillator Start-up Delay | Oscillator Start-up Timer | PLL Lock Time | Total Delay |
|---|---|---|---|---|
| FRC, FRCDIV16, FRCDIVN | TOSCD | — | — | TOSCD |
| FRCPLL | TOSCD | — | TLOCK | TOSCD + TLOCK |
| XT | TOSCD | TOST | — | TOSCD + TOST |
| HS | TOSCD | TOST | — | TOSCD + TOST |
| EC | — | — | — | — |
| XTPLL | TOSCD | TOST | TLOCK | TOSCD + TOST + TLOCK |
| HSPLL | TOSCD | TOST | TLOCK | TOSCD + TOST + TLOCK |
| ECPLL | — | — | TLOCK | TLOCK |
| SOSC | TOSCD | TOST | — | TOSCD + TOST |
| LPRC | TOSCD | — | — | TOSCD |

**Note 1:** TOSCD = Oscillator start-up delay (1.1 µs maximum for FRC; 70 µs maximum for LPRC). Crystal oscillator start-up time varies with crystal characteristics, load capacitance, and so on.

**2:** TOST = Oscillator start-up timer delay (1024 oscillator clock period). For example, TOST = 102.4 µs for 10 MHz crystal and TOST = 32 ms for 32 kHz crystal.

**3:** TLOCK = PLL lock time (1 ms nominal), if PLL is enabled.

#### 9.2.2.2 IDLE MODE

Idle mode has the following characteristics:

- CPU stops executing instructions
- System clock source remains active
- Peripheral modules, by default, continue to operate normally from the system clock source
- Peripherals can optionally be shut down using their Stop-in-Idle control bit (SIDL), which is located in bit position 13 of the control register for most peripheral modules. The generic bit-field name format is “xxxSIDL” (where, “xxx” is the mnemonic name of the peripheral device). For more information, refer to the respective peripheral sections in the *“dsPIC33F/PIC24H Family Reference Manual”*.

When the device exits Idle mode, the CPU starts executing instructions within eight system clock cycles.

#### 9.2.2.3 WAKE-UP FROM SLEEP MODE AND IDLE MODE

Sleep and Idle modes exit on the following events:

- Enabled interrupt event
- WDT time-out
- Reset from any source (POR, BOR and $\overline{\text{MCLR}}$)

##### 9.2.2.3.1 Wake-up on Interrupt

An enabled interrupt event wakes the device from Sleep or Idle mode, which results in the following actions:

- If the assigned priority for the interrupt is less than or equal to the current CPU priority, the device wakes up and continues code execution from the instruction following the `PWRSAV` instruction that initiated Sleep mode.
- If the assigned priority level for the interrupt source is greater than the current CPU priority, the device wakes up and the CPU exception process begins. Code execution continues from the first instruction of the ISR.

##### 9.2.2.3.2 Wake-up on WDT Time-out

If enabled, the WDT continues to run during Sleep or Idle mode. When the WDT time-out occurs, the device wakes up and code execution continues from where the `PWRSAV` instruction was executed.

The Watchdog Timer Time-out Flag bit, WDTO (RCON<4>) is set to indicate that the wake-up event is due to a WDT time-out.

##### 9.2.2.3.3 Wake-up on Reset

A Reset from any source (POR, BOR and $\overline{\text{MCLR}}$) causes the device to exit Sleep or Idle mode, and begin executing from the Reset vector.

| | |
|---|---|
| **Note:** | The Disable Interrupts (`DISI`) instruction cannot disable the interrupt in Sleep mode. For more information on the `DISI` instruction, refer to **Section 6. “Interrupts”** (DS70184). |

### 9.2.3 Hardware-Based Doze Mode

The preferred strategy for reducing power consumption is to change clock speed and invoke Idle mode or Sleep mode. However, in certain circumstances this strategy is not practical. The following effects must be considered:

- Manipulating the system clock speed alters the communication peripheral baud rate and can introduce communication errors
- Using an instruction based power-saving mode (Idle mode/Sleep mode) stops processor execution

Doze mode provides an alternate method to reduce power consumption. In Doze mode, the peripherals are clocked at the system clock frequency, whereas the CPU is clocked at a reduced speed.

Doze mode is enabled by setting the Doze Mode Enable bit (DOZEN) in the Clock Divisor register (CLKDIV<11>). The ratio between peripheral and CPU clock speed is determined by the Processor Clock Reduction Select bits, DOZE<2:0> (CLKDIV<14:12>). There are eight possible configurations, ranging from 1:1 to 1:128, with 1:1 being the default.

The CPU automatically returns to full-speed operation on any interrupt when the Recover On Interrupt bit, ROI (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

| **Note:** | A `NOP` instruction must be executed immediately before entering Doze mode and immediately after exiting Doze mode. Failure to do so may result in unpredictable behavior. |
|---|---|

### 9.2.4 Peripheral Module Disable

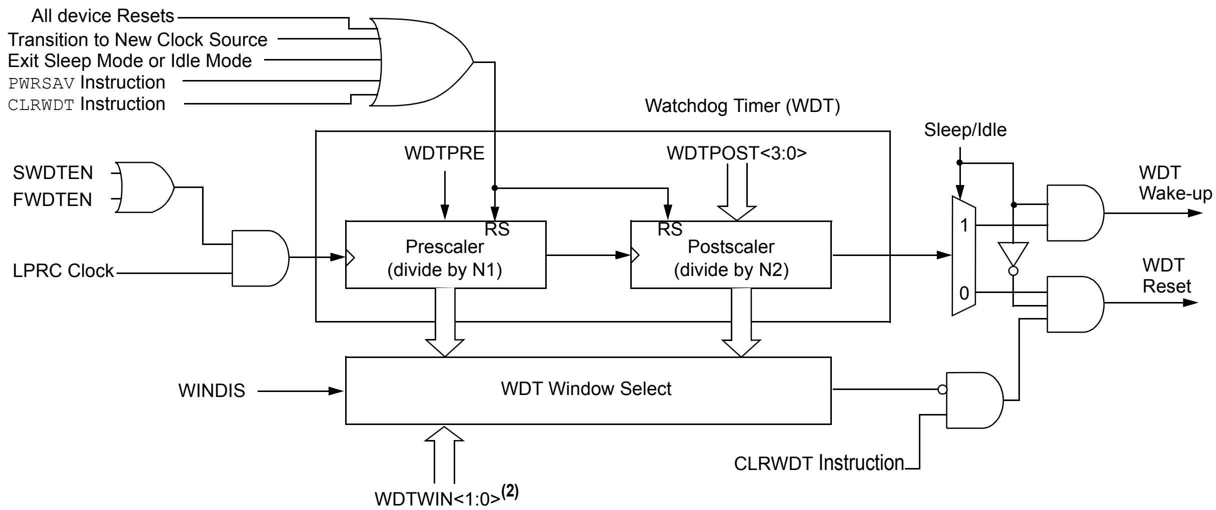
All the peripheral modules (except for I/O ports) in dsPIC33F/PIC24H devices have a control bit that can be selectively disabled to reduce power consumption. These bits, known as the Peripheral Module Disable bits (PMD), are generically named “xxxPMD” (where “xxx” is the mnemonic version of the module name). These bits are located in the PMDx Special Function Registers (SFRs). The PMD bit must be set to ‘1’ to disable the module. The PMD bit shuts down the peripheral, and effectively powering down all circuits and removing all clock sources. All of the peripherals are enabled by default. Refer to the **“Power-Saving Features”** chapter in the specific device data sheet for PMD register details.

## 9.3 WATCHDOG TIMER (WDT)

The primary function of the WDT is to reset the device during the user software malfunction. It can also be used to wake the device from Sleep or Idle mode.

The WDT consists of a programmable prescaler and postscaler clocked with the LPRC oscillator. The WDTO period is selected by configuring the prescaler and postscaler dividers. Figure 9-2 illustrates a block diagram of the WDT.

**Figure 9-2: WDT Block Diagram**




**Note 1:** For the prescaler divider ratio (N1), see Table 9-3 and for the postscaler divider ratio (N2), see Table 9-4.

**2:** Refer to the **"Special Features"** chapter in the specific device data sheet for the availability of these bits.

### 9.3.1 WDT Operation

When enabled, the WDT increments until it overflows or a time-out occurs. A WDT time-out forces a device Reset, except during Sleep or Idle mode. To prevent a WDT time-out reset, the user software must periodically clear the WDT using the `CLRWDT` instruction.

The WDT is also cleared when the device enters Sleep or Idle mode after executing the `PWRSAV` instruction. If the WDT expires during Sleep or Idle mode, the device wakes up and continues code execution from where the `PWRSAV` instruction was executed.

In either case, the WDTO bit (RCON<4>) is set to indicate that the device Reset or wake-up event is due to a WDT time-out.

If a WDT Reset occurs while Flash programming or erase operation is in progress, the Reset will remain pending until the Run-time Self Programming (RTSP) cycle is complete. For more information, refer to **Section 5. "Flash Programming"** (DS70191).

#### 9.3.1.1 ENABLING AND DISABLING THE WDT

The WDT is enabled or disabled by the Watchdog Timer Enable bit (FWDTEN) in the WDT Configuration register (FWDT<7>). When the FWDTEN bit (FWDT<7>) is set, the WDT is always enabled. This is the default value for an erased device.

If the WDT bit is disabled in the FWDT register, the user-assigned application can optionally enable the WDT by setting the Software Enable/Disable of WDT bit (SWDTEN) in the Reset Control register (RCON<5>).



The SWDTEN control bit (RCON<5>) is cleared on any device reset. This bit allows the user-assigned application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

| | |
|---|---|
| **Note:** | The WDT Configuration register (FWDT) values are written during device programming. For more information on the WDT configuration register, refer to **Section 25. "Device Configuration"** (DS70194). |

### 9.3.1.2 WDT WINDOW

The WDT has an optional Windowed mode enabled by programming the Watchdog Timer Window Enable bit, WINDIS (FWDT<6>). In Windowed mode (WINDIS = 0), the WDT should be cleared within an allowed window of the WDTO period, as illustrated in Figure 9-3 through Figure 9-6. If the WDT is cleared before the allowed window, a system Reset is generated immediately.

Windowed mode is useful for resetting the device during unexpected quick or slow execution of a critical portion of the code. Table 9-2 lists all possible window options for devices with and without the WDTWIN<1:0> bits.

**Table 9-2: Window Bit Options**

| WDTWIN<1:0> | Selected Allowed Window |
|---|---|
| Bits not implemented | 25% |
| 11 | 25% |
| 10 | 37.50% |
| 01 | 50% |
| 00 | 75% |

**Figure 9-3: Windowed WDT when WDTWIN<1:0> = 11, or when the WDTWIN<1:0> Bits are not Implemented**

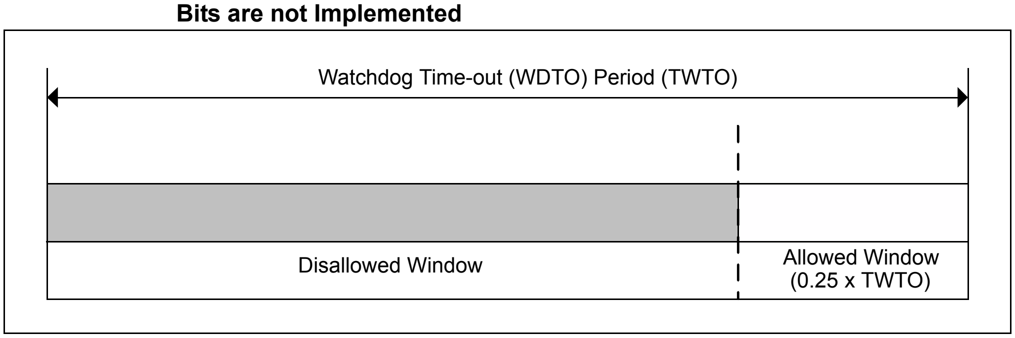



**Figure 9-4: Windowed WDT when WDTWIN<1:0> = 10**

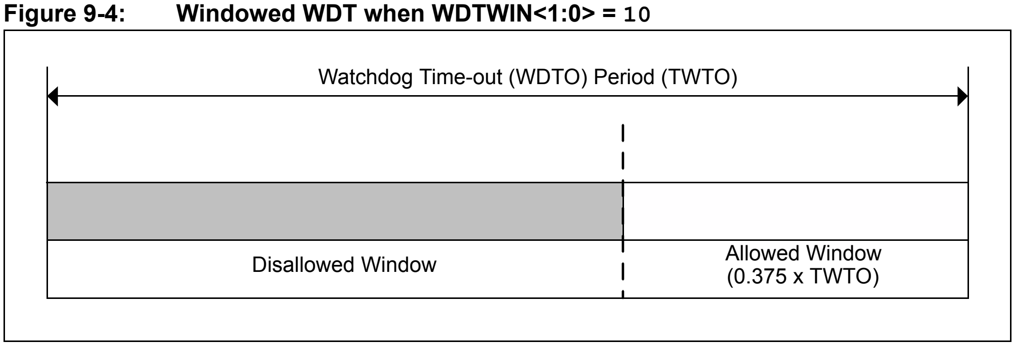


**Figure 9-5: Windowed WDT when WDTWIN<1:0> = 01**

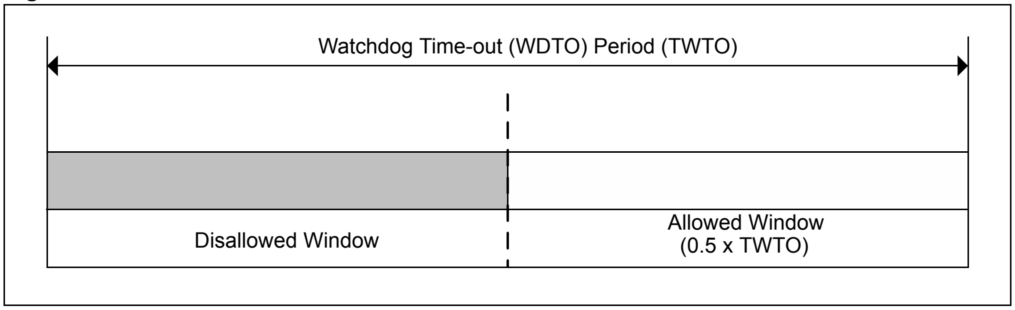
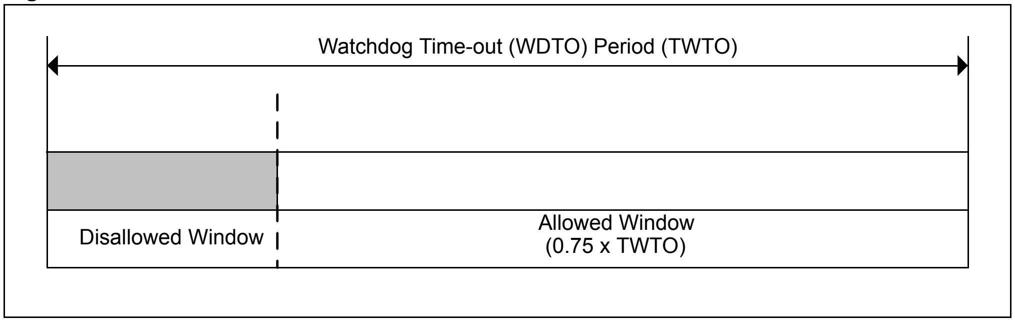



**Figure 9-6: Windowed WDT when WDTWIN<1:0> = 00**




### 9.3.2 WDTO Period Selection

The WDTO period is selected by programming the prescaler and postscaler dividers. The prescaler divider ratio is determined by the Watchdog Timer Prescaler bit, WDTPRE (FWDT<4>).

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler divider ratio is determined by the Watchdog Timer Postscaler bits, WDTPOST<3:0> (FWDT<3:0>), which provides 16 settings (from 1:1 to 1:32,768).

The WDT time-out value can be calculated using Equation 9-1.

**Equation 9-1: WDT Time-out Period**

$$T_{WTO} = (N1) \times (N2) \times (T_{LPRC})$$

Where,

$N1$ = Prescaler divider ratio (see Table 9-3)

$N2$ = Postscaler divider ratio (see Table 9-4)

$T_{LPRC}$ = LPRC clock period

| **Note:** | The WDT time-out period is directly related to the LPRC oscillator frequency (32 kHz nominal). Refer to the **"Electrical Characteristics"** chapter in the specific device data sheet for the accuracy of the LPRC frequency over temperature and voltage variations. |
|---|---|

Table 9-3 and Table 9-4 provide the WDT prescaler and postscaler divider settings.

**Table 9-3: WDT Prescaler Divider Settings**

| Prescaler Setting (WDTPRE) | Prescaler Divider Ratio (N1) |
|---|---|
| 0 | 32 |
| 1 | 128 |

**Table 9-4: WDT Postscaler Divider Settings**

| Postscaler Setting (WDTPOST<3:0>) | Postscaler Divider Ratio (N2) |
|---|---|
| 0000 | 1 |
| 0001 | 2 |
| 0010 | 4 |
| 0011 | 8 |
| 0100 | 16 |
| 0101 | 32 |
| 0110 | 64 |
| 0111 | 128 |
| 1000 | 256 |
| 1001 | 512 |
| 1010 | 1024 |
| 1011 | 2048 |
| 1100 | 4096 |
| 1101 | 8192 |
| 1110 | 16384 |
| 1111 | 32768 |

### 9.3.3 WDT Reset

The WDT is reset in the following circumstances:

- On any device Reset
- When a PWRSAV instruction is executed (that is, Sleep or Idle mode is entered)
- When the WDT is enabled in software
- On the completion of a clock switch
- By a CLRWDT instruction during normal execution or during the last 25% of the WDT time-out period, if WINDIS bit (FWDT<6>) is ‘0’

### 9.3.4 Operation of WDT in Sleep Mode and Idle Mode

If enabled, the WDT continues to run during Sleep or Idle mode. When the WDT time-out occurs, the device wakes up and code execution continues from where the PWRSAV instruction was executed.

The WDT is useful for low-power system designs because it can be used to periodically wake the device from Sleep mode to check the system status and provide action, if necessary. The SWDTEN bit (RCON<5>) is very useful in this case. If the WDT is disabled during normal operation (FWDTEN = 0), the SWDTEN bit (RCON<5>) can be used to turn on the WDT before entering Sleep mode.

## 9.4 DESIGN TIPS

***Question 1:*** ***The device resets even though I have inserted a `CLRWDT` instruction in my main software loop.***

**Answer:** Ensure that the software loop that contains the `CLRWDT` instruction meets the minimum specification of the WDT (not the typical value). Also, ensure that interrupt processing time has been accounted for.

***Question 2:*** ***What should my software do before entering Sleep mode or Idle mode?***

**Answer:** Ensure that the sources intended to wake the device have their Interrupt Enable bits set. In addition, ensure that the particular source of interrupt can wake the device. Some sources do not function when the device is in Sleep mode.

If the device is to be placed in Idle mode, ensure that the “stop-in-idle” control bit for each peripheral device is properly set. These control bits determine whether the peripheral will continue operation in Idle mode. Refer to the individual peripheral sections in this manual for further details.

***Question 3:*** ***How do I tell which peripheral woke the device from Sleep mode or Idle mode?***

**Answer:** You can poll the Interrupt Flag bits for each enabled interrupt source to determine the source of wake-up.

## 9.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F/PIC24H product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Watchdog Timer (WDT) and Power-Saving Modes module are:

| Title | Application Note # |
|---|---|
| Low Power Design Using PICmicro® Microcontrollers | AN606 |

| **Note:** | Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F/PIC24H family of devices. |
|---|---|

## 9.6 REVISION HISTORY

### Revision A (March 2007)

This is the initial released version of the document

### Revision B (March 2010)

This revision incorporates the following updates:

- Merged the dsPIC33F and PIC24H family reference manual sections titled Section 9. Watchdog Timer (WDT) and Power-Saving Modes, into this single document
- Tables:
  - Updated the postscaler setting values in binary representation (see Table 9-4)
- Note:
  - Added a note with information to customers for utilizing family reference manual sections and data sheets as a joint reference (see note above **9.1 "Introduction"**)
  - Added a note on executing the `NOP` instruction in the Doze mode section (see **9.2.3 "Hardware-Based Doze Mode"**)
- Additional minor corrections such as language and formatting updates were incorporated throughout the document

### Revision C (July 2010)

This revision includes the following updates:

- Updated the WDT block diagram (see Figure 9-2)
- Added a new paragraph to **9.3.1 "WDT Operation"**
- Added Table 9-2: Window Bit Options
- Replaced Figure 9-3 and added Figure 9-4 through Figure 9-6
- Minor corrections to text and formatting were incorporated throughout the document

### Revision D (May 2012)

This revision incorporates the following updates:

- Notes:
  - Added a note in **9.2.2.3.3 "Wake-up on Reset"**
- Minor updates to text and formatting were incorporated throughout the document

NOTES:

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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