# PIC18F97J94 FAMILY

## Flash Microcontroller Programming Specification

### 1.0 DEVICE OVERVIEW

This document includes the programming specifications for the following devices:

- PIC18F97J94
- PIC18F96J99
- PIC18F96J94
- PIC18F95J94
- PIC18F87J94
- PIC18F86J99
- PIC18F86J94
- PIC18F85J94
- PIC18F67J94
- PIC18F66J99
- PIC18F66J94
- PIC18F65J94

### 2.0 PROGRAMMING OVERVIEW OF THE PIC18F97J94 FAMILY

The PIC18F97J94 family devices are programmed using In-Circuit Serial Programming™ (ICSP™). This programming specification applies to PIC18F97J94 family devices in all package types.

### 2.1 Pin Diagrams

The pin diagrams for the PIC18F97J94 family are shown in Figure 2-1, Figure 2-2 and Figure 2-3. The pins that are required for programming are listed in Table 2-1 and shown in bold lettering in the figures.

**TABLE 2-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC18F97J94 FAMILY**

| Pin Name | During Programming | | |
|---|---|---|---|
| | Pin Name | Pin Type | Pin Description |
| $\overline{MCLR}$ | $\overline{MCLR}$ | P | Programming Enable |
| VDD and AVDD(1) | VDD | P | Power Supply |
| VSS and AVSS(1) | VSS | P | Ground |
| VDDCORE/VCAP | VDDCORE | P | Regulated Power Supply for Microcontroller Core |
| | VCAP | I | Filter Capacitor for On-Chip Voltage Regulator |
| RB6 | PGC | I | Serial Clock |
| RB7 | PGD | I/O | Serial Data |
| VUSB3V3 | VUSB3V3 | P | USB Voltage Supply |

**Legend:** I = Input, O = Output, P = Power

**Note 1:** All power supply and ground pins must be connected, including analog supplies (AVDD) and ground (AVSS).

**FIGURE 2-1: PIC18F6XJ9X PIN DIAGRAMS**

**64-Pin TQFP**

The following devices are included in 64-pin TQFP parts:

- PIC18F67J94
- PIC18F66J94
- PIC18F66J99
- PIC18F65J94

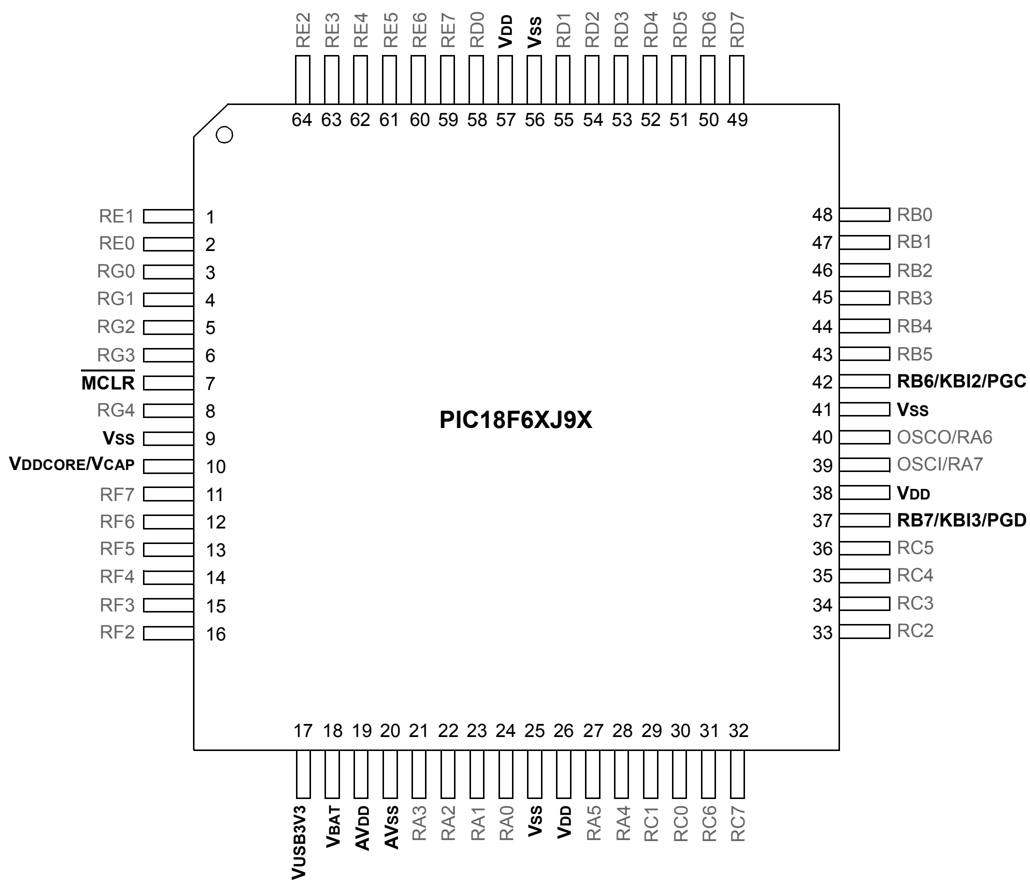


**FIGURE 2-2: PIC18F8XJ9X PIN DIAGRAMS**

### 80-Pin TQFP

The following devices are included in 80-pin TQFP parts:

- PIC18F87J94
- PIC18F86J94
- PIC18F86J99
- PIC18F85J94

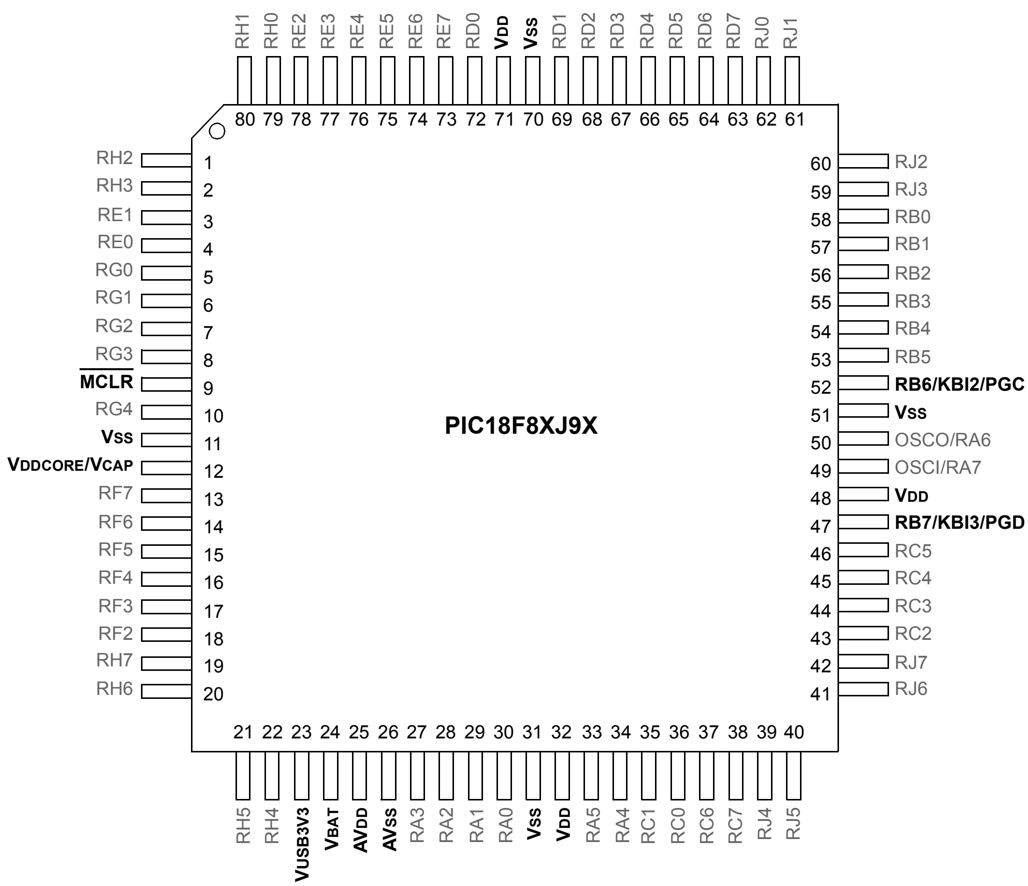
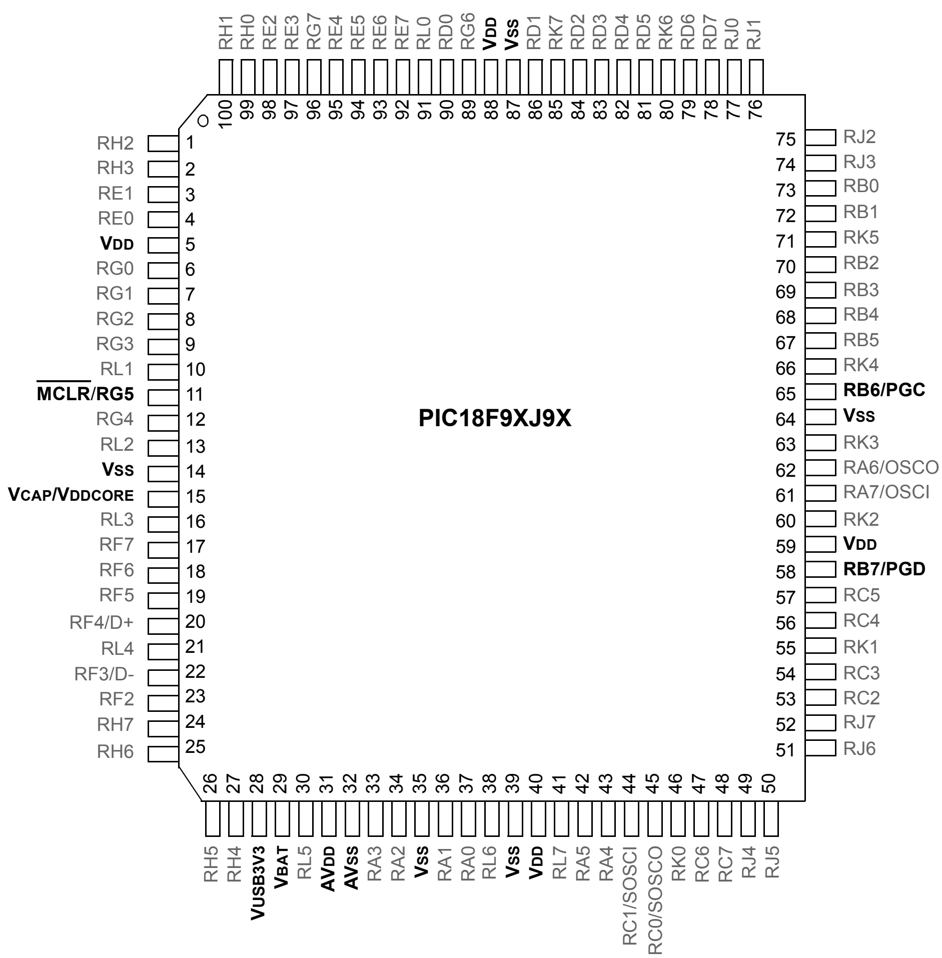


**FIGURE 2-3: PIC18F9XJ9X PIN DIAGRAMS**

**100-Pin TQFP**

The following devices are included in 100-pin TQFP parts:

- PIC18F97J94
- PIC18F96J99
- PIC18F96J94
- PIC18F95J94



#### 2.1.1 ON-CHIP VOLTAGE REGULATOR

All PIC18F97J94 family devices power their core digital logic at a nominal 1.8V. To simplify system design, all devices in the family incorporate an on-chip regulator that allows the device to run its core logic from VDD. For the PIC18F97J94 family, the regulator is always enabled, so there is no ENVREG pin on these devices.

The regulator provides power to the core from the other VDD pins. A low-ESR capacitor (such as ceramic or tantalum) must be connected to the VCAP pin. This helps to maintain the stability of the regulator.

The specifications for core voltage and capacitance are listed in **Section 6.0 "AC/DC Characteristics and Timing Requirements"**.

### 2.2 Memory Maps

The PIC18F97J94 family devices offer a total of four program memory sizes, ranging from 32 Kbytes to 128 Kbytes. The memory sizes for different members of the family are shown in Table 2-2. The overall memory maps for all devices are shown in Figure 2-4.

For purposes of code protection, the program memory for every device is treated as a single block. Enabling code protection, thus protects the entire code memory and not just individual segments.

The Configuration Words for these devices are located at addresses, 300000h through 30000Fh. These are implemented as eight pairs of volatile memory registers. Each register is automatically loaded from a copy stored at the end of program memory. For this reason, the last eight words of the code space (also called the Flash Configuration Words) should be written with configuration data and not executable code. The offset addresses of the Flash Configuration Words are also listed in Table 2-2. Refer to **Section 5.0 "Configuration Word"** for more information.

Locations, 3FFFFEh and 3FFFFFh, are reserved for the Device ID bits. These bits may be used by the programmer to identify what device type is being programmed and are described in **Section 5.1 "Device ID and Configuration Block Word"**. These Device ID bits read out normally, even after code protection.

#### 2.2.1 MEMORY ADDRESS POINTER

Memory in the device address space (000000h to 3FFFFFh) is addressed via the Table Pointer register, which in turn, is comprised of three registers:

- TBLPTRU at RAM address: 0FF8h
- TBLPTRH at RAM address: 0FF7h
- TBLPTRL at RAM address: 0FF6h

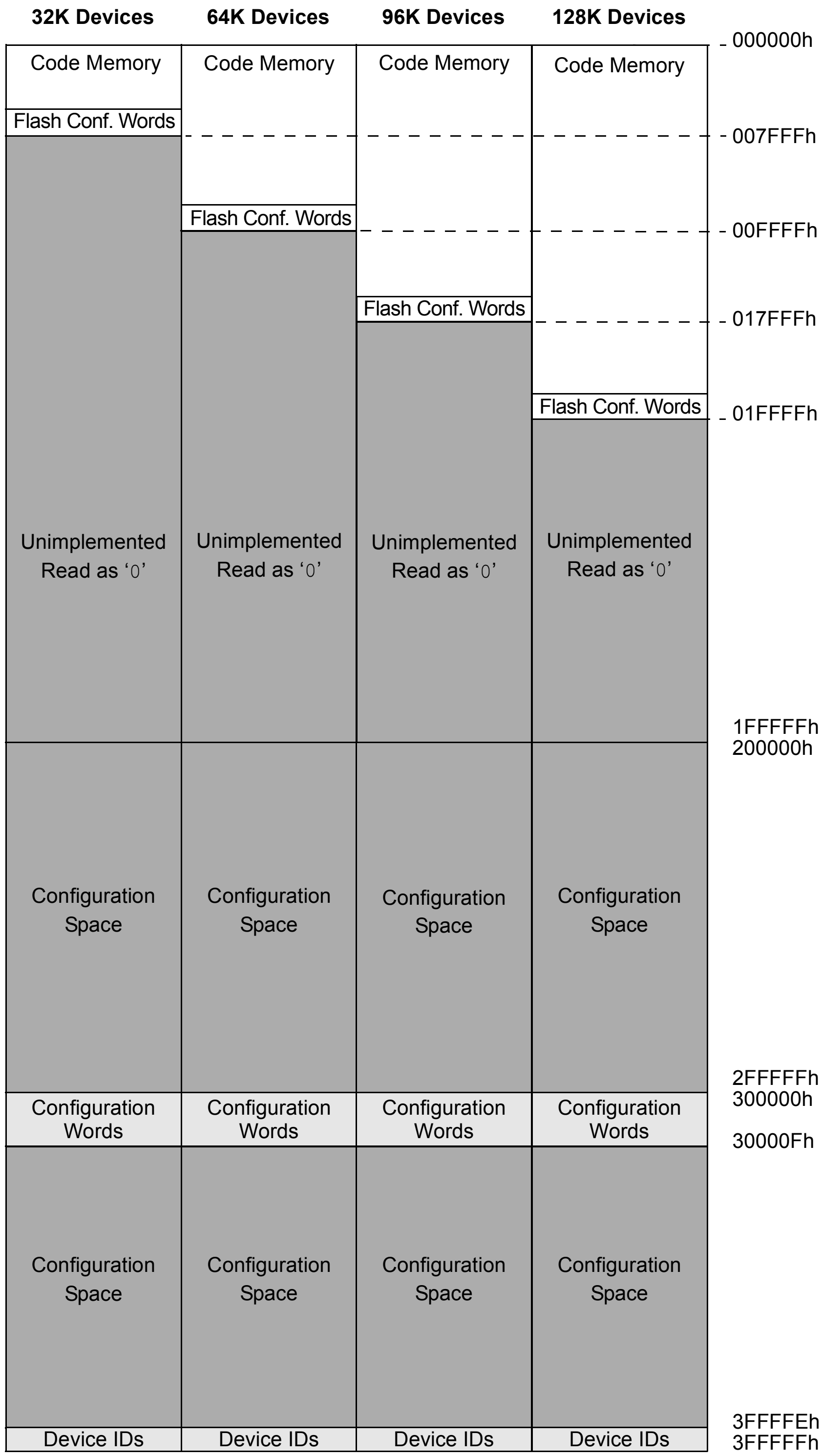
| TBLPTRU | TBLPTRH | TBLPTRL |
|---|---|---|
| Addr<21:16> | Addr<15:8> | Addr<7:0> |

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

**TABLE 2-2: PROGRAM MEMORY SIZES FOR PIC18F97J94 FAMILY DEVICES**

| Device | Program Memory (Kbytes) | Location of Flash Configuration Words |
|---|---|---|
| PIC18F95J94 | 32 | 07FF0h:07FFFh |
| PIC18F85J94 | | |
| PIC18F65J94 | | |
| PIC18F96J94 | 64 | 0FFF0h:0FFFFh |
| PIC18F86J94 | | |
| PIC18F66J94 | | |
| PIC18F96J99 | 96 | 17FF0h:17FFFh |
| PIC18F86J99 | | |
| PIC18F66J99 | | |
| PIC18F97J94 | 128 | 1FFF0h:1FFFFh |
| PIC18F87J94 | | |
| PIC18F67J94 | | |

**FIGURE 2-4: MEMORY MAPS FOR PIC18F97J94 DEVICES(1)**




Memory spaces are unimplemented or unavailable in normal execution mode and read as '0'.

Memory spaces are read-only (Device IDs) or cannot be directly programmed by ICSP™ (Configuration Words).

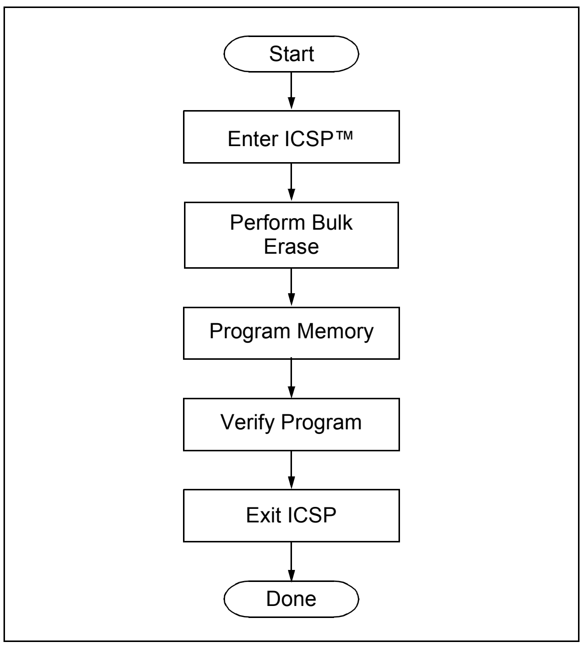
**Note 1:** Sizes of memory areas are not to scale. Sizes of accessible memory areas are enhanced to show detail.

## 2.3 Overview of the Programming Process

Figure 2-5 shows the high-level overview of the programming process. First, a Bulk Erase is performed. Next, the code memory is programmed. Since the only nonvolatile Configuration Words are within the code memory space, they too are programmed as if they were code. Code memory (including the Configuration Words) is then verified to ensure that programming was successful.

| | |
|---|---|
| **Note:** | In order to maintain the endurance of the cells, each Flash byte should not be programmed more than twice between erase operations. A Bulk Erase of the device is required before attempting to modify the contents a third time. |

**FIGURE 2-5: HIGH-LEVEL PROGRAMMING FLOW**




## 2.4 Entering and Exiting ICSP Program/Verify Mode

Entry into ICSP modes for PIC18F97J94 family devices is somewhat different than previous PIC18 devices. As shown in Figure 2-6, entering ICSP Program/Verify mode requires four steps:

1. Voltage is briefly applied to the $\overline{\text{MCLR}}$ pin.
2. A 32-bit key sequence is presented on PGD.
3. Voltage is reapplied to $\overline{\text{MCLR}}$.
4. A single `NOP` is executed.

The programming voltage applied to $\overline{\text{MCLR}}$ is $V_{IH}$, or usually, $V_{DD}$. There is no minimum time requirement for holding at $V_{IH}$. After $V_{IH}$ is removed, an interval of at least P19 must elapse before presenting the key sequence on PGD.

The key sequence is a specific 32-bit pattern, '`0100 1101 0100 0011 0100 1000 0101 0000`' (more easily remembered as 4D434850h in hexadecimal). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit (MSb) of the most significant nibble must be shifted in first.

Once the key sequence is complete, $V_{IH}$ must be applied to $\overline{\text{MCLR}}$ and held at that level for as long as Program/Verify mode is to be maintained. An interval of at least time, P20 and P12, must elapse before presenting data on PGD. Signals appearing on PGD before P12 has elapsed may not be interpreted as valid. The first instruction after the key sequence should be a single `NOP` instruction made of 20 bit clocks of data 0.

On successful entry, the program memory can be accessed and programmed in serial fashion. While in the Program/Verify mode, all unused I/Os are placed in the high-impedance state.

Exiting Program/Verify mode is done by removing $V_{IH}$ from $\overline{\text{MCLR}}$, as shown in Figure 2-7. The only requirement for exit is that an interval, P16, should elapse between the last clock, and the program signals on PGC and PGD before removing $V_{IH}$.

When $V_{IH}$ is reapplied to $\overline{\text{MCLR}}$, the device will enter the ordinary operational mode and begin executing the application instructions.

**FIGURE 2-6: ENTERING PROGRAM/VERIFY MODE**

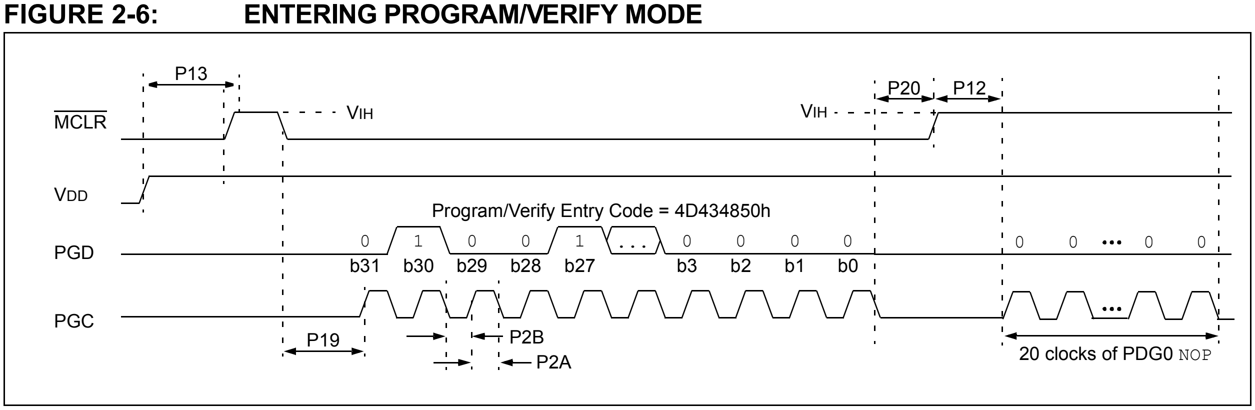
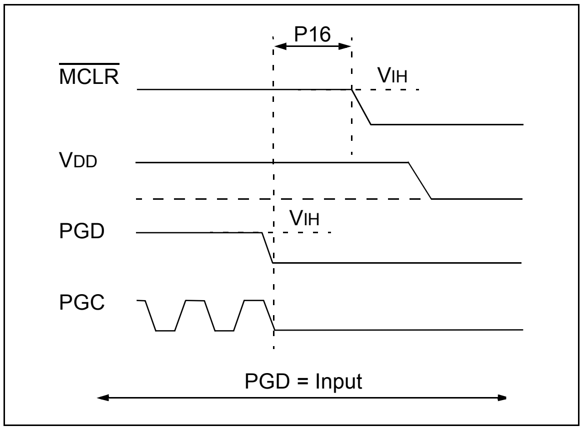


**FIGURE 2-7: EXITING PROGRAM/VERIFY MODE**




## 2.5 Serial Program/Verify Operation

The PGC pin is used as a clock input pin and the PGD pin is used for entering command bits and data input/output during serial operation. Commands and data are transmitted on the rising edge of PGC, latched on the falling edge of PGC, and are Least Significant bit (LSb) first.

### 2.5.1 4-BIT COMMANDS

All instructions are 20 bits, consisting of a leading 4-bit command followed by a 16-bit operand, which depends on the type of command being executed. To input a command, PGC is cycled four times. The commands needed for programming and verification are shown in Table 2-3.

Depending on the 4-bit command, the 16-bit operand represents 16 bits of input data or eight bits of input data and eight bits of output data.

Throughout this specification, commands and data are presented as illustrated in Table 2-4. The 4-bit command is shown, Most Significant bit (MSb) first. The command operand, or “Data Payload”, is shown <MSB><LSB>. Figure 2-8 demonstrates how to serially present a 20-bit command/operand to the device.

### 2.5.2 CORE INSTRUCTION

The core instruction passes a 16-bit instruction to the CPU core for execution. This is needed to set up registers as appropriate for use with other commands.

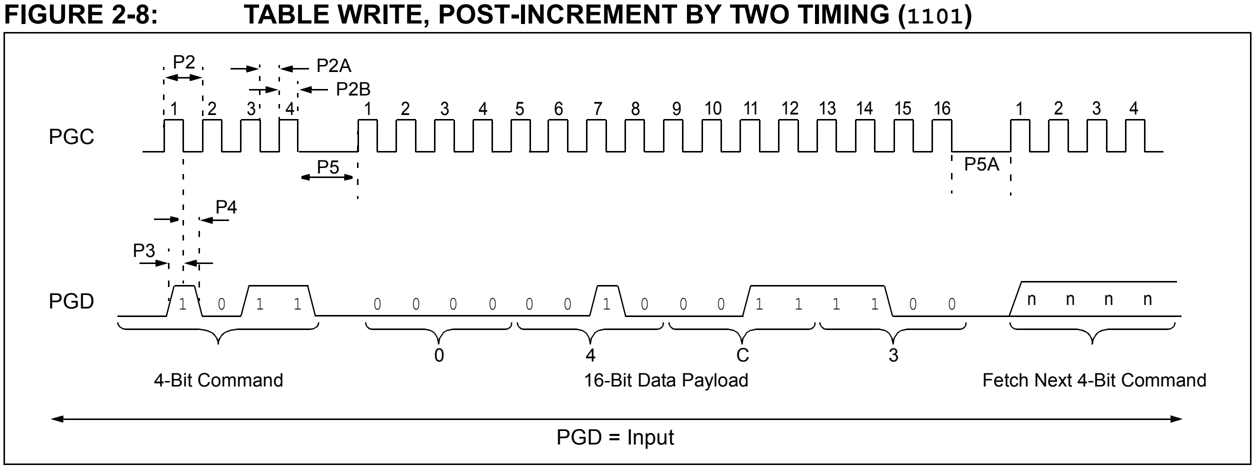
**TABLE 2-3: COMMANDS FOR PROGRAMMING**

| Description | 4-Bit Command |
|---|---|
| Core Instruction (shift in 16-bit instruction) | `0000` |
| Shift Out TABLAT Register | `0010` |
| Table Read | `1000` |
| Table Read, Post-Increment | `1001` |
| Table Read, Post-Decrement | `1010` |
| Table Read, Pre-Increment | `1011` |
| Table Write | `1100` |
| Table Write, Post-Increment by 2 | `1101` |
| Table Write, Start Programming, Post-Increment by 2 | `1110` |
| Table Write, Start Programming | `1111` |

**TABLE 2-4: SAMPLE COMMAND SEQUENCE**

| 4-Bit Command | Data Payload | Core Instruction |
|---|---|---|
| `1101` | `3C 40` | `Table Write, post-increment by 2` |

**FIGURE 2-8: TABLE WRITE, POST-INCREMENT BY TWO TIMING (`1101`)**



## 3.0 DEVICE PROGRAMMING

Programming includes the ability to erase or write the memory within the device.

### 3.1 ICSP Erase

#### 3.1.1 ICSP BULK ERASE

The PIC18F97J94 family devices may be Bulk Erased by writing 0180h to the table address, 3C0005h:3C0004h. The basic sequence is shown in Table 3-1 and demonstrated in Figure 3-1.

Since the code-protect Configuration bit is stored in the program code within code memory, a Bulk Erase operation will also clear any code-protect settings for the device.

The actual Bulk Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the `NOP` command), serial execution will cease until the erase completes (Parameter P11). During this time, PGC may continue to toggle but PGD must be held low.

> **Note:** A Bulk Erase is the only way to reprogram the code-protect Configuration bit from an ON state to an OFF state.

**TABLE 3-1: BULK ERASE COMMAND SEQUENCE**

| 4-Bit Command | Data Payload | Core Instruction |
|---|---|---|
| 0000 | 0E 3C | MOVLW 3Ch |
| 0000 | 6E F8 | MOVWF TBLPTRU |
| 0000 | 0E 00 | MOVLW 00h |
| 0000 | 6E F7 | MOVWF TBLPTRH |
| 0000 | 0E 05 | MOVLW 05h |
| 0000 | 6E F6 | MOVWF TBLPTRL |
| 1100 | 01 01 | Write 01h to 3C0005h |
| 0000 | 0E 3C | MOVLW 3Ch |
| 0000 | 6E F8 | MOVWF TBLPTRU |
| 0000 | 0E 00 | MOVLW 00h |
| 0000 | 6E F7 | MOVWF TBLPTRH |
| 0000 | 0E 04 | MOVLW 04h |
| 0000 | 6E F6 | MOVWF TBLPTRL |
| 1100 | 80 80 | Write 80h TO 3C0004h to erase entire device. |
| | | NOP |
| 0000 | 00 00 | Hold PGD low until erase |
| 0000 | 00 00 | completes. |

**FIGURE 3-1: BULK ERASE FLOW**

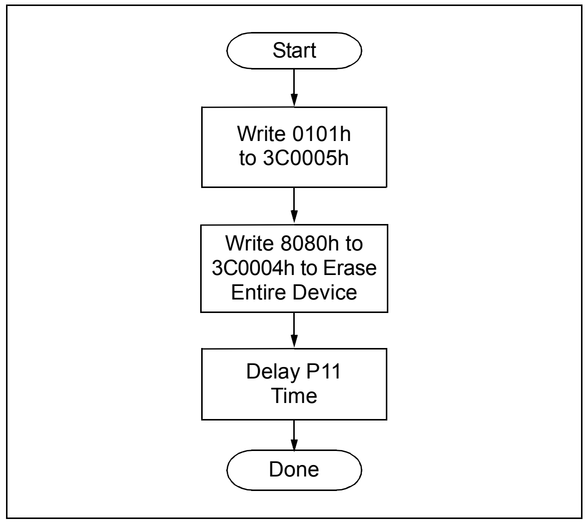
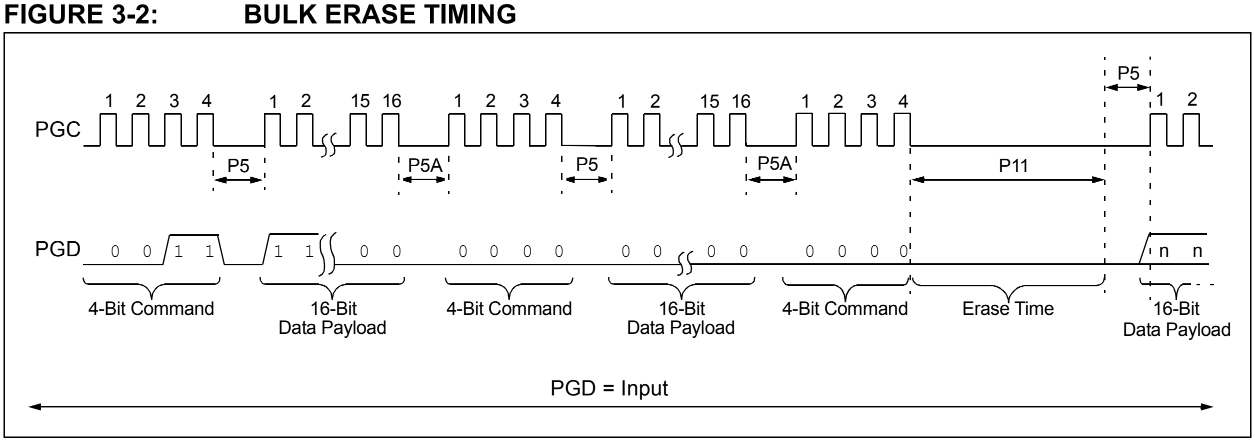



**FIGURE 3-2: BULK ERASE TIMING**



### 3.1.2 ICSP ROW ERASE

It is possible to erase a single row (512 bytes of data), provided the block is not code-protected. Rows are located at static boundaries, beginning at program memory address, 000000h, extending to the internal program memory limit (see **Section 2.2 "Memory Maps"**).

The Row Erase duration is internally timed. After the WR bit in EECON1 is set, a `NOP` is issued, where the 4th PGC is held high for the duration of the Row Erase time, P10.

The code sequence to Row Erase a PIC18F97J94 family device is shown in Table 3-2. The flowchart, shown in Figure 3-3, depicts the logic necessary to completely erase a PIC18F97J94 family device. The timing diagram that details the "Row Erase" operation and Parameter P10, is shown in Figure 3-3.

| **Note:** | The TBLPTR register can point at any byte within the row intended for erase. |
|---|---|

**FIGURE 3-3: ROW ERASE CODE MEMORY FLOW**

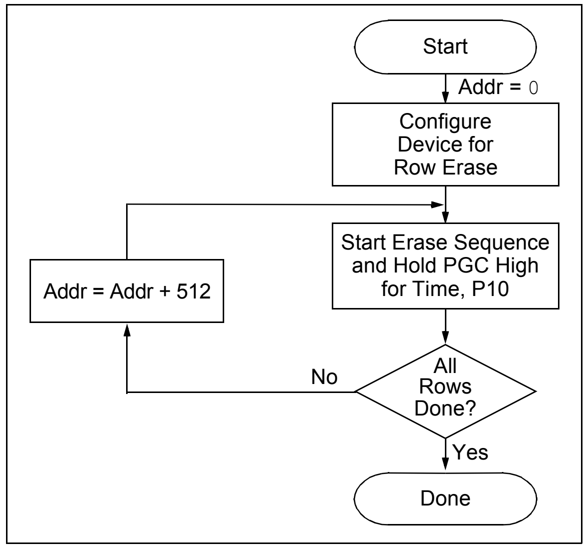



**TABLE 3-2: ERASE CODE MEMORY CODE SEQUENCE**

| 4-Bit Command | Data Payload | Core Instruction |
|---|---|---|
| Step 1: Enable memory writes. | | |
| 0000<br>0000 | 84 7F<br>6A 7F | BSF EECON1, WREN<br>CLRF EECON1 |
| Step 2: Point to first row in code memory. | | |
| 0000<br>0000<br>0000 | 6A F8<br>6A F7<br>6A F6 | CLRF TBLPTRU<br>CLRF TBLPTRH<br>CLRF TBLPTRL |
| Step 3: Enable erase and erase single row. | | |
| 0000<br>0000<br>0000<br>0000 | 88 7F<br>82 7F<br>00 00<br>00 00 | BSF EECON1, FREE<br>BSF EECON1, WR<br>NOP<br>NOP - hold PGC high for time P10. |
| Step 4: Repeat Step 3 with Address Pointer incremented by 512 until all rows are erased. | | |

## 3.2 Code Memory Programming

Programming code memory is accomplished by first loading data into the write buffer and then initiating a programming sequence. The write buffer for all PIC18F97J94 family devices is 64 bytes. It can be mapped to any integral boundary of 64 bytes, beginning at 000000h. The actual memory write sequence takes the contents of this buffer and programs the 64 bytes of code memory that contain the Table Pointer.

Write buffer locations are not cleared following a write operation. The buffer retains its data after the write is complete. This means that the buffer must be written with 64 bytes on each operation. If there are locations in the code memory that are to remain empty, the corresponding locations in the buffer must be filled with FFFFh. This avoids rewriting old data from the previous cycle.

The programming duration is internally timed. After a Start Programming command is issued (4-bit command, '`1111`'), a `NOP` is issued, where the 4th PGC is held high for the duration of the programming time, P9.

The code sequence to program a PIC18F97J94 family device is shown in Table 3-3. The flowchart shown in Figure 3-4 depicts the logic necessary to completely write a PIC18F97J94 family device. The timing diagram that details the Start Programming command and Parameter P9 is shown in Figure 3-5.

> **Note 1:** To maintain the endurance specification of the Flash program memory cells, each 64-byte block of program memory should never be programmed more than twice between erase operations. If any byte within a 64-byte block of program memory is written, that entire block must not be written to again until a Bulk Erase on the part, or a Row Erase on the row containing the modified 64-byte block, has been performed.
>
> **2:** The TBLPTR register must point to the same region when initiating the programming sequence, as it did when the write buffers were loaded.

**TABLE 3-3: WRITE CODE MEMORY CODE SEQUENCE**

| 4-Bit Command | Data Payload | Core Instruction |
|---|---|---|
| Step 1: Enable writes. | | |
| 0000 | 84 7F | BSF EECON1, WREN |
| Step 2: Load write buffer. | | |
| 0000<br>0000<br>0000<br>0000<br>0000<br>0000 | 0E <Addr[21:16]><br>6E F8<br>0E <Addr[15:8]><br>6E F7<br>0E <Addr[7:0]><br>6E F6 | MOVLW <Addr[21:16]><br>MOVWF TBLPTRU<br>MOVLW <Addr[15:8]><br>MOVWF TBLPTRH<br>MOVLW <Addr[7:0]><br>MOVWF TBLPTRL |
| Step 3: Repeat for all but the last two bytes. Any unused locations should be filled with FFFFh. | | |
| 1101 | <MSB><LSB> | TBLWT *+ Write 2 bytes and post-increment address by 2. |
| Step 4: Load write buffer for last two bytes. | | |
| 1111<br>0000 | <MSB><LSB><br>00 00 | TBLWT *+ Write 2 bytes and start programming.<br>NOP - hold PGC high for time P9. |
| To continue writing data, repeat Steps 2 through 4, where the Address Pointer is incremented by 2 at each iteration of the loop. | | |

**FIGURE 3-4: PROGRAM CODE MEMORY FLOW**

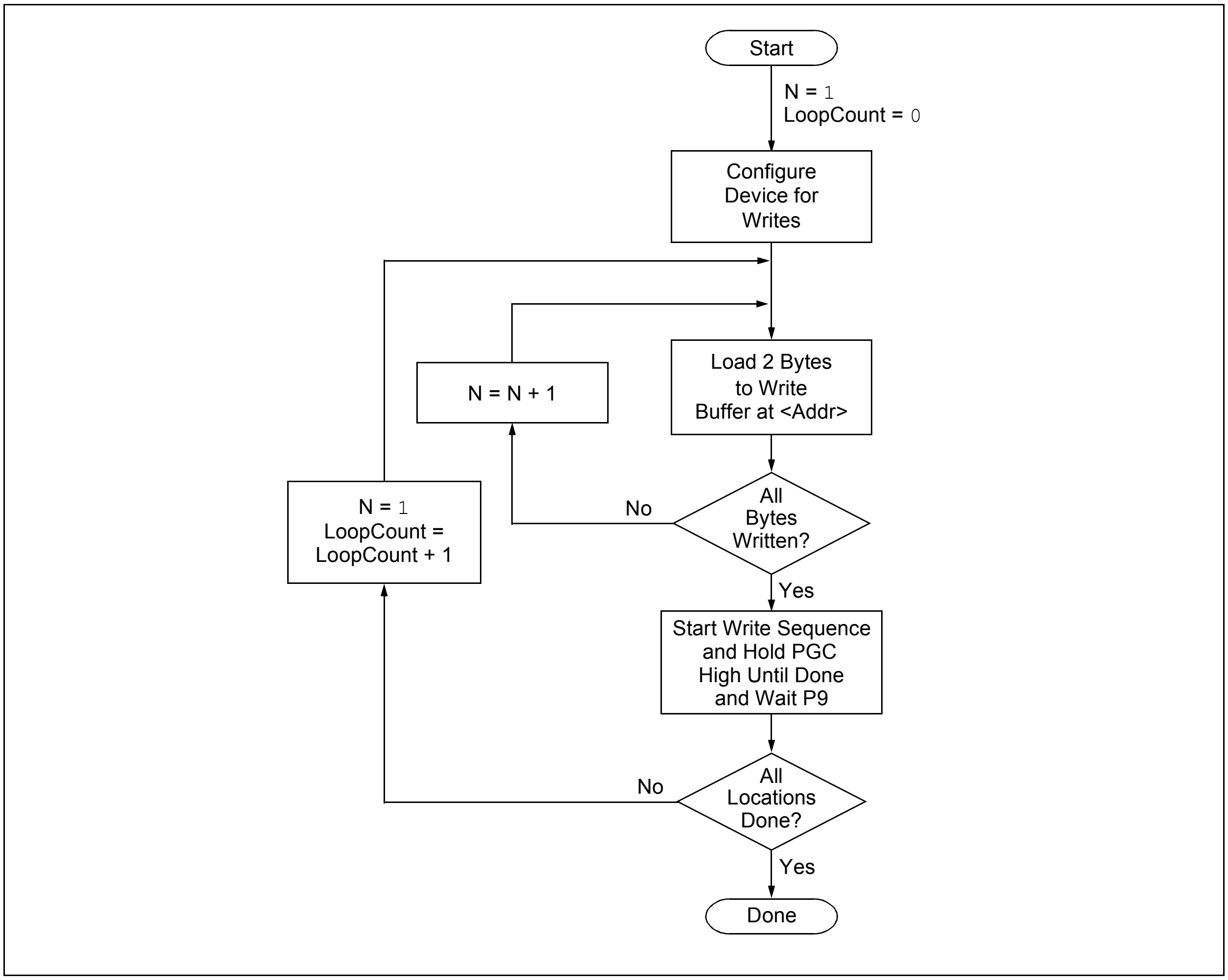
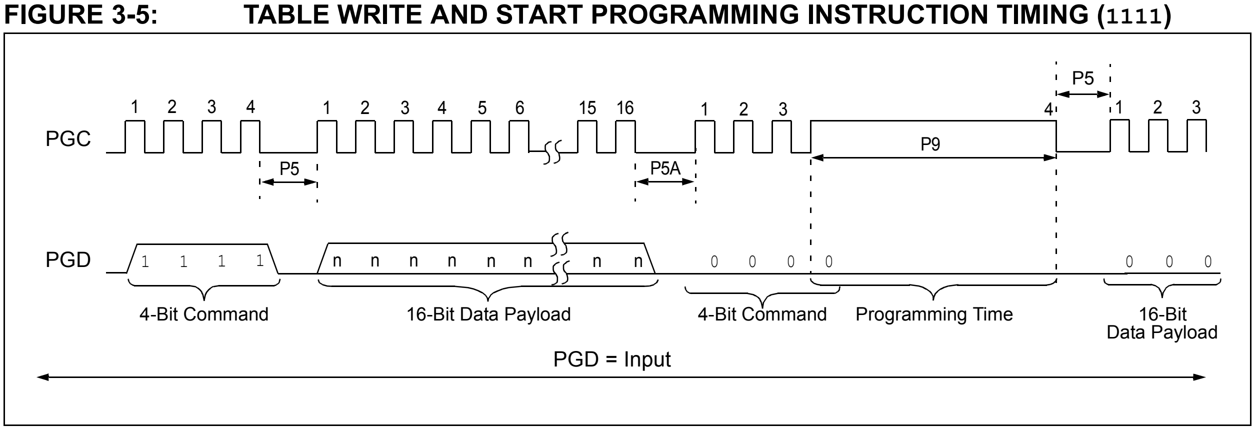



**FIGURE 3-5: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING (1111)**



### 3.2.1 MODIFYING CODE MEMORY

The previous programming example assumed that the device had been Bulk Erased prior to programming. It may be the case, however, that the user wishes to modify only a section of an already programmed device.

The appropriate number of bytes required for the erase buffer (512 bytes) must be read out of code memory (as described in **Section 4.2 "Verify Code Memory and Configuration Word"**) and buffered; modifications can be made on this buffer. Then, the row of code memory that was read out must be erased and rewritten with the modified data. The code sequence is shown in Table 3-4. The WREN bit must be set if the WR bit in EECON1 is used to initiate a write sequence.

### 3.2.2 CONFIGURATION WORD PROGRAMMING

Since the Flash Configuration Words are stored in program memory, they are programmed as if they were program data. Refer to **Section 3.2 "Code Memory Programming"** and **Section 3.2.1 "Modifying Code Memory"** for methods and examples on programming or modifying program memory. Also, see **Section 5.0 "Configuration Word"** for additional information on the Configuration Words.

**TABLE 3-4: MODIFYING CODE MEMORY**

| 4-Bit Command | Data Payload | Core Instruction |
|---|---|---|
| Step 1: Direct access to code memory. | | |
| 0000<br>0000<br>0000<br>0000<br>0000<br>0000 | 0E <Addr[21:16]><br>6E F8<br>0E <Addr[8:15]><br>6E F7<br>0E <Addr[7:0]><br>6E F6 | MOVLW <Addr[21:16]><br>MOVWF TBLPTRU<br>MOVLW <Addr[8:15]><br>MOVWF TBLPTRH<br>MOVLW <Addr[7:0]><br>MOVWF TBLPTRL |
| Step 2: Set-up for an erase. | | |
| 0000<br>0000 | 84 7F<br>88 7F | BSF EECON1, WREN<br>BSF EECON1, FREE |
| Step 3: Erase the block of memory. | | |
| 0000<br>0000 | 82 7F<br>00 00 | BSF EECON1, WR<br>BSF NOP – hold PGC high for time P10. |
| Step 4: Load write buffer. The correct bytes will be selected based on the Table Pointer. | | |
| 0000<br>0000<br>0000<br>0000<br>0000<br>0000<br>1101<br>.<br>.<br>.<br>1111<br>0000 | 0E <Addr[21:16]><br>6E F8<br>0E <Addr[8:15]><br>6E F7<br>0E <Addr[7:0]><br>6E F6<br><MSB><LSB><br>.<br>.<br>.<br><MSB><LSB><br>00 00 | MOVLW <Addr[21:16]><br>MOVWF TBLPTRU<br>MOVLW <Addr[8:15]><br>MOVWF TBLPTRH<br>MOVLW <Addr[7:0]><br>MOVWF TBLPTRL<br>Write 2 bytes and post-increment address by 2.<br><br>Repeat as many times as necessary to fill the write buffer.<br><br>Write 2 bytes and start programming.<br>NOP - hold PGC high for time P9. |
| Step 5: Disable writes. | | |
| 0000 | 94 7F | BCF EECON1, WREN |
| Step 6: To continue modifying data, repeat, where the Address Pointer is incremented by 512 bytes at each iteration of the loop. | | |

# 4.0 READING THE DEVICE

## 4.1 Read Code Memory

Code memory is accessed, one byte at a time, via the 4-bit command, '1001' (table read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

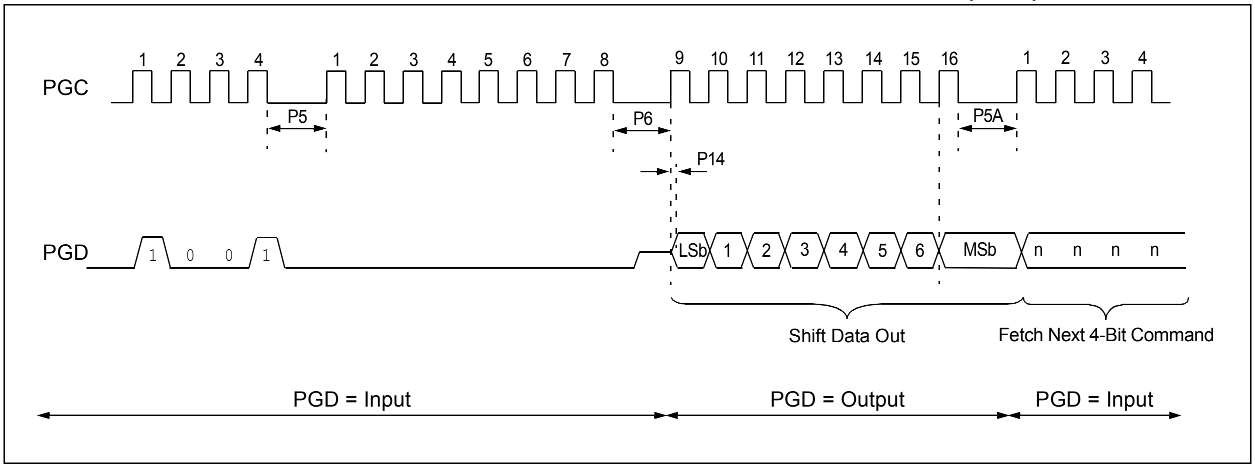
The 4-bit command is shifted in, LSb first. The read is executed during the next eight clocks, then shifted out on PGD during the last eight clocks, LSb to MSb. A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see Figure 4-1). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFh address space, so it also applies to reading the Configuration registers.

TABLE 4-1: READ CODE MEMORY SEQUENCE

| 4-Bit Command | Data Payload | Core Instruction |
|---|---|---|
| Step 1: Set Table Pointer. | | |
| 0000<br>0000<br>0000<br>0000<br>0000<br>0000 | 0E <Addr[21:16]><br>6E F8<br>0E <Addr[15:8]><br>6E F7<br>0E <Addr[7:0]><br>6E F6 | MOVLW Addr[21:16]<br>MOVWF TBLPTRU<br>MOVLW <Addr[15:8]><br>MOVWF TBLPTRH<br>MOVLW <Addr[7:0]><br>MOVWF TBLPTRL |
| Step 2: Read memory and then shift out on PGD, LSb to MSb. | | |
| 1001 | 00 00 | TBLRD *+ |

FIGURE 4-1: TABLE READ, POST-INCREMENT INSTRUCTION TIMING (1001)



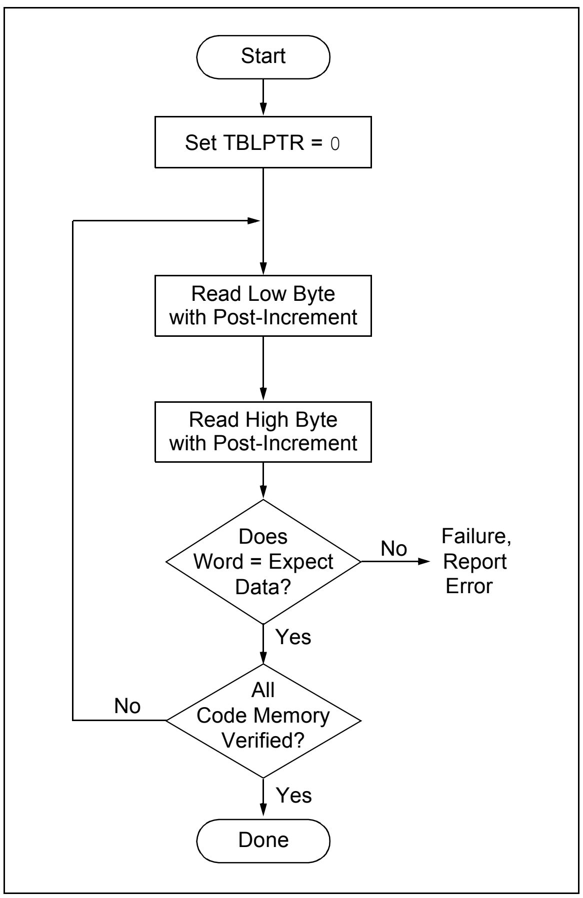
### 4.2 Verify Code Memory and Configuration Word

The verify step involves reading back the code memory space and comparing it against the copy held in the programmer's buffer. Because the Flash Configuration Words are stored at the end of program memory, it is verified with the rest of the code at this time.

The verify process is shown in the flowchart in Figure 4-2. Memory reads occur a single byte at a time, so two bytes must be read to compare against the word in the programmer's buffer. Refer to **Section 4.1 "Read Code Memory"** for implementation details of reading code memory.

| **Note:** | Because the Flash Configuration Word contains the device code protection bit, code memory should be verified immediately after writing if code protection is enabled. This is because the device will not be readable or verifiable if a device Reset occurs after the Flash Configuration Words (and the CP0 bit) have been cleared. |
|---|---|

**FIGURE 4-2: VERIFY CODE MEMORY FLOW**




### 4.3 Blank Check

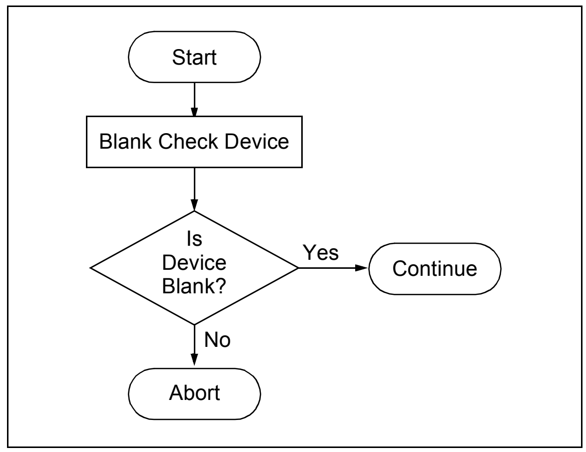
The term, "Blank Check", means to verify that the device has no programmed memory cells. All memories must be verified: code memory and Configuration bits. The Device ID registers (3FFFFEh:3FFFFFh) should be ignored.

A "blank" or "erased" memory cell will read as '1', so Blank Checking a device merely means to verify that all bytes read as FFh. The overall process flow is shown in Figure 4-3.

| **Note:** | Following a device Bulk Erase, the Configuration Words will read as shown in Table 5-2. |
|---|---|

Given that Blank Checking is merely code verification with FFh expect data, refer to **Section 4.2 "Verify Code Memory and Configuration Word"** for implementation details.

**FIGURE 4-3: BLANK CHECK FLOW**



## 5.0 CONFIGURATION WORD

The Configuration Words of the PIC18F97J94 family devices are implemented as volatile memory registers, as opposed to the programmable nonvolatile memory used in other PIC18 devices. All of the Configuration registers (CONFIG1L:CONFIG8H) are automatically loaded following each device Reset.

The data for these registers is taken from the eight Flash Configuration Words located at the end of program memory. Configuration data is stored in order, starting with CONFIG1L in the lowest Flash address and ending with CONFIG8H in the last address. The mapping to specific Configuration Words is shown in Table 5-1. Eight words are reserved in program memory (CONFIG1L through CONFIG8H) for device configuration. Users should always reserve these locations for Configuration Word data and write their application code accordingly.

The upper four bits of each Flash Configuration Word should always be stored in program memory as '`1111`'. This is done so these program memory addresses will always be '`1111 xxxx xxxx xxxx`' and interpreted as a `NOP` instruction if they were ever to be executed. Because the corresponding bits in the Configuration Words are unimplemented, they will not change the device's configuration.

The Configuration and Device ID registers are summarized in Table 5-2. A listing of the individual Configuration bits and their options is provided in Table 5-3.

**TABLE 5-1: MAPPING OF THE FLASH CONFIGURATION WORDS TO THE CONFIGURATION REGISTERS**

| Configuration Byte | Code Space Address(1) | Configuration Register Address |
|---|---|---|
| CONFIG1L | XXFF0h | 300000h |
| CONFIG1H | XXFF1h | 300001h |
| CONFIG2L | XXFF2h | 300002h |
| CONFIG2H | XXFF3h | 300003h |
| CONFIG3L | XXFF4h | 300004h |
| CONFIG3H(2) | XXFF5h | 300005h |
| CONFIG4L | XXFF6h | 300006h |
| CONFIG4H | XXFF7h | 300007h |
| CONFIG5L | XXFF8h | 300008h |
| CONFIG5H | XXFF9h | 300009h |
| CONFIG6L | XXFFAh | 30000Ah |
| CONFIG6H | XXFFBh | 30000Bh |
| CONFIG7L | XXFFCh | 30000Ch |
| CONFIG7H(2) | XXFFDh | 30000Dh |
| CONFIG8L | XXFFEh | 30000Eh |
| CONFIG8H | XXFFFh | 30000Fh |

**Note 1:** See Table 2-2 for the complete addresses within code space for specific devices and memory sizes.

**2:** Unimplemented in PIC18F97J94 family devices.

## TABLE 5-2: CONFIGURATION BITS AND DEVICE IDs

| File Name | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default/ Unprog. Value |
|---|---|---|---|---|---|---|---|---|---|---|
| 300000h | CONFIG1L | $\overline{\text{DEBUG}}$ | XINST | STVREN | — | — | — | — | — | `111- ----` |
| 300001h | CONFIG1H | —(1) | —(1) | —(1) | —(1) | —(2) | CP0 | BORV | BOREN | `---- 0111` |
| 300002h | CONFIG2L | IESO | — | CLKOEN | — | SOSCSEL | FOSC2 | FOSC1 | FOSC0 | `---- 1111` |
| 300003h | CONFIG2H | —(1) | —(1) | —(1) | —(1) | PLLDIV3 | PLLDIV2 | PLLDIV1 | PLLDIV0 | `---- 1111` |
| 300004h | CONFIG3L | — | — | FSCM1 | FSCM0 | — | — | POSCMD1 | POSCMD0 | `--11 --11` |
| 300005h | CONFIG3H | —(1) | —(1) | —(1) | —(1) | — | — | — | — | `---- ----` |
| 300006h | CONFIG4L | WPFP7 | WPFP6 | WPFP5 | WPFP4 | WPFP3 | WPFP2 | WPFP1 | WPFP0 | `1111 1111` |
| 300007h | CONFIG4H | —(1) | —(1) | —(1) | —(1) | — | WPCFG | WPEND | WPDIS | `---- -111` |
| 300008h | CONFIG5L | WAIT | BW | ABW1 | ABW0 | EASHFT | — | CINASEL | T5GSEL | `1111 1-11` |
| 300009h | CONFIG5H | —(1) | —(1) | —(1) | —(1) | MSSPMSK1 | MSSPMSK2 | LS48MHZ | IOL1WAY | `---- 1111` |
| 30000Ah | CONFIG6L | WDPS3 | WDPS2 | WDPS1 | WDPS0 | WDTCLK1 | WDTCLK0 | WDTWIN1 | WDTWIN0 | `1111 1111` |
| 30000Bh | CONFIG6H | —(1) | —(1) | —(1) | —(1) | WPSA | WINDIS | WDTEN1 | WDTEN0 | `---- 1111` |
| 30000Ch | CONFIG7L | — | — | — | DSBOREN | DSZPBOR | VBTBOR | — | $\overline{\text{RETEN}}$ | `---1 1101` |
| 30000Dh | CONFIG7H | —(1) | —(1) | —(1) | —(1) | — | — | — | — | `---- ----` |
| 30000Eh | CONFIG8L | DSWDTPS4 | DSWDTPS3 | DSWDTPS2 | DSWDTPS1 | DSWDTPS0 | — | — | — | `1111 1---` |
| 30000Fh | CONFIG8H | —(1) | —(1) | —(1) | —(1) | — | — | DSWDTOSC | DSWDTEN | `---- --11` |
| 3FFFFEh | DEVID1(3) | DEV2 | DEV1 | DEV0 | REV4 | REV3 | REV2 | REV1 | REV0 | See Table 5-4 |
| 3FFFFFh | DEVID2(3) | DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | DEV3 | See Table 5-4 |

**Note 1:** The value of these bits in program memory should always be ‘`1`’. This ensures that the location is executed as a `NOP` if it is accidentally executed.

**2:** This bit should always be maintained as ‘`0`’.

**3:** DEVID registers are read-only and cannot be programmed by the user.

**TABLE 5-3: PIC18F97J94 FAMILY BIT DESCRIPTIONS**

| Bit Name | Configuration Words | Description |
|---|---|---|
| $\overline{\text{DEBUG}}$ | CONFIG1L | Background Debugger Enable bit<br>1 = Background debugger is disabled; RB6 and RB7 are configured as general purpose I/O pins<br>0 = Background debugger is enabled; RB6 and RB7 are dedicated to In-Circuit Debug |
| XINST | CONFIG1L | Extended Instruction Set Enable bit<br>1 = Instruction set extension and Indexed Addressing mode are enabled<br>0 = Instruction set extension and Indexed Addressing mode are disabled (Legacy mode) |
| STVREN | CONFIG1L | Stack Overflow/Underflow Reset Enable bit<br>1 = Reset on stack overflow/underflow is enabled<br>0 = Reset on stack overflow/underflow is disabled |
| CP0 | CONFIG4H | Code Protection bit<br>1 = Program memory is not code-protected<br>0 = Program memory is code-protected |
| BORV | CONFIG1H | BOR Trip Point Select bit<br>1 = BOR trip point is 1.8V<br>0 = BOR trip point is 2.0V |
| BOREN | CONFIG1H | Brown-out Reset Enable bit<br>1 = BORMV is enabled outside of Deep Sleep (BORMV is always disabled in Deep Sleep)<br>0 = BORMV is disabled |
| IESO | CONFIG2L | Internal/External Oscillator Switchover bit<br>1 = Oscillator Switchover mode is enabled<br>0 = Oscillator Switchover mode is disabled |
| CLKOEN | CONFIG2L | CLKO Enable Configuration bit<br>1 = CLKO output signal is active on the OSCO pin; the Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active<br>0 = CLKO output is disabled |
| SOSCSEL | CONFIG2L | Secondary Oscillator Selection Configuration bit<br>1 = Low-Power Secondary Oscillator circuit is selected (typical $I_{DD}$ of 1 µA)<br>0 = Digital (SCLKI) mode |
| FOSC<2:0> | CONFIG2L | Oscillator Selection bits<br>000 = Fast RC Oscillator (FRC)<br>001 = Fast RC Oscillator with divide-by-N and PLL module (FRCDIV+PLL)<br>010 = Primary Oscillator (MS, HS, EC)<br>011 = Primary Oscillator with PLL module (MS+PLL, HS+PLL, EC+PLL)<br>100 = Secondary Oscillator (SOSC)<br>101 = Low-Power RC Oscillator (LPRC)<br>110 = Fast RC Oscillator (FRC) divided by 16 (500 kHz)<br>111 = Fast RC Oscillator with divide-by-N (FRCDIV) |

**Note 1:** These bits are not available on 64-pin devices.

**TABLE 5-3: PIC18F97J94 FAMILY BIT DESCRIPTIONS (CONTINUED)**

| Bit Name | Configuration Words | Description |
|---|---|---|
| PLLDIV<3:0> | CONFIG2H | Frequency Multiplier Select bits<br>1111 = No PLL used – PLLGO bit is not available to user<br>1110 = 8x PLL is selected<br>1101 = 6x PLL is selected<br>1100 = 4x PLL is selected<br>1011 = Reserved (do not use)<br>1010 = Reserved (do not use)<br>1001 = Reserved (do not use)<br>1000 = Reserved (do not use)<br>0111 = 96 MHz PLL is selected – Oscillator is divided by 12 (48 MHz input)<br>0110 = 96 MHz PLL is selected – Oscillator is divided by 10 (40 MHz input)<br>0101 = 96 MHz PLL is selected – Oscillator is divided by 6 (24 MHz input)<br>0100 = 96 MHz PLL is selected – Oscillator is divided by 5 (20 MHz input)<br>0011 = 96 MHz PLL is selected – Oscillator is divided by 4 (16 MHz input)<br>0010 = 96 MHz PLL is selected – Oscillator is divided by 3 (12 MHz input)<br>0001 = 96 MHz PLL is selected – Oscillator is divided by 2 (8 MHz input)<br>0000 = 96 MHz PLL is selected – No divide (4 MHz input) |
| FSCM<1:0> | CONFIG3L | Clock Switching and Monitor Selection Configuration bits<br>1x = Clock switching is disabled, Fail-Safe Clock Monitor (FSCM) is disabled<br>01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled<br>00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled |
| POSCMD<1:0> | CONFIG3L | Primary Oscillator Configuration bits<br>11 = Primary Oscillator is disabled<br>10 = HS Oscillator mode is selected (10 MHz-40 MHz)<br>01 = MS Oscillator mode is selected (3.5 MHz-10 MHz)<br>00 = External Clock mode is selected |
| WPFP<7:0> | CONFIG4L | Write Protection Program Flash Pages bits (valid when WPDIS = 0)<br>When WPEND = 0:<br>Write/erase protection of Flash memory pages, starting at Page 0 and ending with Page WPFP<7:0>.<br>When WPEND = 1:<br>Write/erase protection of Flash memory pages, starting at Page WPFP<7:0> and ending with the last page in user Flash memory. |
| WPCFG | CONFIG4H | Write/Erase Protection Last Page in User Flash Memory bit<br>1 = Write/erase protection of last page is disabled, regardless of the WPFP<7:0> bits setting<br>0 = Write/erase protection of last page is enabled, regardless of the WPFP<7:0> bits setting |
| WPEND | CONFIG4H | Write Protection End Page bit<br>1 = Write/erase protection of Flash memory pages, starting at Page WPFP<7:0> and ending with the last page in user Flash memory<br>0 = Write/erase protection of Flash memory pages, starting at Page 0 and ending with Page WPFP<7:0> |
| WPDIS | CONFIG4H | Write Protection Disable bit<br>1 = WPFP<7:0>, WPEND and WPCFG bits are ignored<br>0 = WPFP<7:0>, WPEND and WPCFG bits are enabled – write-protect is active |
| WAIT(1) | CONFIG5L | External Bus Wait Enable bit<br>1 = Wait states for operations on External Memory Bus (EMB) are disabled<br>0 = Wait states for operations on External Memory Bus are enabled |

**Note 1:** These bits are not available on 64-pin devices.

**TABLE 5-3: PIC18F97J94 FAMILY BIT DESCRIPTIONS (CONTINUED)**

| Bit Name | Configuration Words | Description |
|---|---|---|
| BW[1] | CONFIG5L | Data Bus Width Select bit<br>1 = 16-Bit External Bus mode<br>0 = 8-Bit External Bus mode |
| ABW<1:0>[1] | CONFIG5L | External Memory Bus Configuration bits<br>00 = Extended Microcontroller mode, 20-Bit Addressing mode<br>01 = Extended Microcontroller mode, 16-Bit Addressing mode<br>10 = Extended Microcontroller mode, 12-Bit Addressing mode<br>11 = Microcontroller mode – external bus is disabled |
| EASHFT[1] | CONFIG5L | External Address Bus Shift Enable bit<br>1 = Address shifting is enabled – address on external bus is offset to start at 000000h<br>0 = Address shifting is disabled – address on external bus reflects the PC value |
| CINASEL | CONFIG5L | CxINA Gate Select bit<br>1 = C1INA and C3INA are both remapped to RA5 pin<br>0 = C1INA and C3INA are on their default pin locations |
| T5GSEL | CONFIG5L | TMR5 Gate Select bit<br>1 = C1INA and C3INA are both remapped to RA5TMR5 pin; gate is driven by the T5G input<br>0 = C1INA and C3INA are both remapped to RA5TMR5 pin; gate is driven by the T3G input |
| MSSPMSK1 | CONFIG5H | MSSP1 7-Bit Address Masking Mode Enable bit<br>1 = 7-Bit Address Masking mode is enabled<br>0 = 5-Bit Address Masking mode is enabled |
| MSSPMSK2 | CONFIG5H | MSSP2 7-Bit Address Masking Mode Enable bit<br>1 = 7-Bit Address Masking mode is enabled<br>0 = 5-Bit Address Masking mode is enabled |
| LS48MHZ | CONFIG5H | USB Low-Speed Clock Select bit<br>1 = Divide-by-2 (P1 clock must be 12 MHz)<br>0 = Divide-by-1 (P1 clock must be 6 MHz) |
| IOL1WAY | CONFIG5H | IOLOCK Bit One-Way Set Enable bit<br>1 = The IOLOCK bit can only be set once (provided an unlocking sequence is executed); once IOLOCK is set, this prevents any possible future RP register changes<br>0 = The IOLOCK bit can be set and cleared as needed (provided an unlocking sequence is executed) |

**Note 1:** These bits are not available on 64-pin devices.

**TABLE 5-3: PIC18F97J94 FAMILY BIT DESCRIPTIONS (CONTINUED)**

| Bit Name | Configuration Words | Description |
|---|---|---|
| WDPS<3:0> | CONFIG6L | Watchdog Timer Postscale Select bits<br>1111 = 1:32,768<br>1110 = 1:16,384<br>1101 = 1:8,192<br>1100 = 1:4,096<br>1011 = 1:2,048<br>1010 = 1:1,024<br>1001 = 1:512<br>1000 = 1:256<br>0111 = 1:128<br>1010 = 1:64<br>0101 = 1:32<br>0100 = 1:16<br>0011 = 1:8<br>1010 = 1:4<br>0001 = 1:2<br>0000 = 1:1 |
| WDTCLK<1:0> | CONFIG6L | Watchdog Timer Clock Source bits<br>00 = Use P1 clock when system clock is not INTOSC/LPRC and device is not in Sleep – otherwise, use INTOSC/LPRC<br>01 = SOSC clock source<br>10 = INTOSC/LPRC clock source<br>11 = FRC when WINDIS = 0, system clock is not INTOSC/LPRC and device is not in Sleep – otherwise, use INTOSC/LPRC |
| WDTWIN<1:0> | CONFIG6L | Watchdog Timer Window Width bits<br>00 = 75%<br>01 = 50%<br>10 = 37.5%<br>11 = 25% |
| WPSA | CONFIG6H | WDT Prescaler bit<br>1 = WDT prescaler ratio of 1:128<br>0 = WDT prescaler ratio of 1:32 |
| WINDIS | CONFIG6H | Windowed Watchdog Timer disable bit<br>1 = Standard WDT is selected – windowed WDT is disabled<br>0 = Windowed WDT is enabled – note that executing a CLRWDT instruction while the WDT is disabled in hardware, software (FWDTEN<1:0> = 00 and SWDTEN (RCON<5> = 0, will not cause a device Reset |
| WDTEN<1:0> | CONFIG6H | Watchdog Timer Enable bits<br>11 = WDT is enabled in hardware<br>10 = WDT is controlled with the SWDTEN bit setting<br>01 = WDT is only enabled while device is active and disabled in Sleep; SWDTEN bit is disabled<br>00 = WDT is disabled in hardware; SWDTEN bit is disabled |
| DSBITEN | CONFIG7L | Deep Sleep Enable bit<br>1 = Deep Sleep is controlled by the register bit, DSEN<br>0 = Deep Sleep operation is always disabled |
| DSBOREN | CONFIG7L | Deep Sleep BOR Enable bit<br>1 = BOR is enabled in Deep Sleep<br>0 = BOR is disabled in Deep Sleep (does not effect operation in non-Deep Sleep modes) |

**Note 1:** These bits are not available on 64-pin devices.

**TABLE 5-3: PIC18F97J94 FAMILY BIT DESCRIPTIONS (CONTINUED)**

| Bit Name | Configuration Words | Description |
|---|---|---|
| VBTBOR | CONFIG7L | VBAT BOR Enable bit<br>1 = VBAT BOR is enabled<br>0 = VBAT BOR is disabled |
| $\overline{\text{RETEN}}$ | CONFIG7L | Retention Voltage Regulator Control Enable bit<br>1 = Retention feature is not available<br>0 = Retention feature is available and controlled by SRETEN during Sleep |
| DSWDTPS<4:0> | CONFIG8L | Deep Sleep Watchdog Timer Postscale Select bits<br>The DS WDT prescaler is 32; this creates an approximate base time unit of 1 ms.<br>11111 = 1:$2^{36}$ (25.7 days)<br>11110 = 1:$2^{35}$ (12.8 days)<br>11101 = 1:$2^{34}$ (6.4 days)<br>11100 = 1:$2^{33}$ (77.0 hours)<br>11011 = 1:$2^{32}$ (38.5 hours)<br>11010 = 1:$2^{31}$ (19.2 hours)<br>11001 = 1:$2^{30}$ (9.6 hours)<br>11000 = 1:$2^{29}$ (4.8 hours)<br>10111 = 1:$2^{28}$ (2.4 hours)<br>10110 = 1:$2^{27}$ (72.2 minutes)<br>10101 = 1:$2^{26}$ (36.1 minutes)<br>10100 = 1:$2^{25}$ (18.0 minutes)<br>10011 = 1:$2^{24}$ (9.0 minutes)<br>10010 = 1:$2^{23}$ (4.5 minutes)<br>10001 = 1:$2^{22}$ (135.3s)<br>10000 = 1:$2^{21}$ (67.7s)<br>01111 = 1:$2^{20}$ (33.825s)<br>01110 = 1:$2^{19}$ (16.912s)<br>01101 = 1:$2^{18}$ (8.456s)<br>01100 = 1:$2^{17}$ (4.228s)<br>01011 = 1:65536 (2.114s)<br>01010 = 1:32768 (1.057s)<br>01001 = 1:16384 (528.5 ms)<br>01000 = 1:8192 (264.3 ms)<br>00111 = 1:4096 (132.1 ms)<br>00110 = 1:2048 (66.1 ms)<br>00101 = 1:1024 (33 ms)<br>00100 = 1:512 (16.5 ms)<br>00011 = 1:256 (8.3 ms)<br>00010 = 1:128 (4.1 ms)<br>00001 = 1:64 (2.1 ms)<br>00000 = 1:32 (1 ms) |
| DSWDTOSC | CONFIG8H | DSWDT Reference Clock Select bit<br>1 = DSWDT uses INTOSC/LPRC as the reference clock<br>0 = DSWDT uses T1OSC/SOSC as the reference clock |
| DSWDTEN | CONFIG8H | Deep Sleep Watchdog Timer Enable bit<br>1 = DSWDT is enabled<br>0 = DSWDT is disabled |

**Note 1:** These bits are not available on 64-pin devices.

## 5.1 Device ID

The Device ID Word for PIC18F97J94 family devices is located at: 3FFFFEh:3FFFFFh. These read-only bits may be used by the programmer to identify what device type is being programmed and read out normally, even after code protection has been enabled. The process for reading the Device IDs is shown in Figure 5-1. A complete list of Device ID values for PIC18F97J94 family devices is presented in Table 5-4.

**FIGURE 5-1: READ DEVICE ID WORD FLOW**

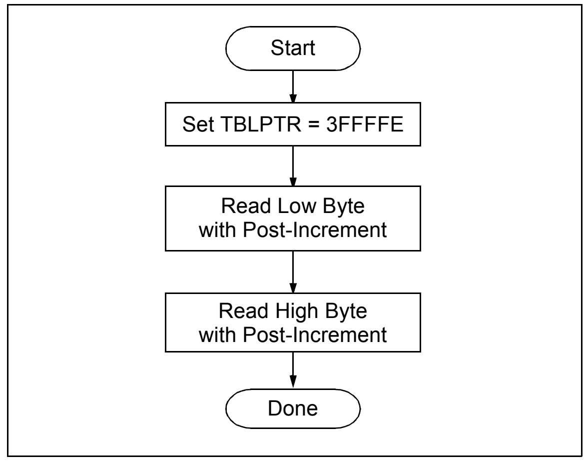



**TABLE 5-4: DEVICE ID VALUE**

| Device | Device ID Value | |
|---|---|---|
| | DEVID2 | DEVID1 |
| PIC18F97J94 | 62h | `101x xxxx` |
| PIC18F96J99 | 62h | `110x xxxx` |
| PIC18F96J94 | 62h | `111x xxxx` |
| PIC18F95J94 | 63h | `000x xxxx` |
| PIC18F87J94 | 63h | `001x xxxx` |
| PIC18F86J99 | 63h | `010x xxxx` |
| PIC18F86J94 | 63h | `011x xxxx` |
| PIC18F85J94 | 63h | `100x xxxx` |
| PIC18F67J94 | 63h | `101x xxxx` |
| PIC18F66J99 | 63h | `110x xxxx` |
| PIC18F66J94 | 63h | `111x xxxx` |
| PIC18F65J94 | 64h | `000x xxxx` |

**Legend:** The ‘`x`’s in DEVID1 are reserved for the device revision code.

## 5.2 Checksum Computation

The checksum is calculated by summing the following:

- The contents of all code memory locations
- The Configuration Block (CFGB), appropriately masked
- ID locations

The Least Significant 16 bits of this sum are the checksum.

The Configuration Block for PIC18F97J94 family devices is located at 300000h:300000Fh. To compute the CFG80/100-pin checksum, perform a logical AND between each byte of data in the Configuration Word location and its corresponding hex value in the CFG80/100-pin column as shown in Table 5-5. To compute the CFG64-pin checksum, perform a logical AND between each byte of data in the Configuration Word location and its corresponding hex value in the CFG64-pin column as shown in Table 5-5.

Sum the AND'ed values of all Configuration Words as part of the checksum calculation.

Table 5-6 describes how to calculate the checksum for each device.

> **Note:** The checksum calculation differs depending on the code-protect setting. Since the code memory locations read out differently depending on the code-protect setting, the table describes how to manipulate the actual code memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire code memory can simply be read and summed.

**TABLE 5-5: CONFIGURATION WORD LOCATION OF CFG80/100 AND CFG64 PINS**

| Configuration Word | Location | CFG80/100 Pin | CFG64 Pin |
|---|---|---|---|
| CW1 | Last Location – 16 | FFE0h | FFE0h |
| CW2 | Last Location – 14 | FFAFh | FFAFh |
| CW3 | Last Location – 12 | F033h | F033h |
| CW4 | Last Location – 10 | F7FFh | F7FFh |
| CW5 | Last Location – 8 | FFFBh | FF03h |
| CW6 | Last Location – 6 | FFFFh | FFFFh |
| CW7 | Last Location – 4 | F01Dh | F01Dh |
| CW8 | Last Location – 2 | F3F8h | F3F8h |

**TABLE 5-6: CHECKSUM EQUATION FOR PIC18F97J94 FAMILY**

| Family | Device | Read Code Protection | Checksum Computation | Blank Checksum |
|---|---|---|---|---|
| PIC18F97J94 | PIC18F97J94 | Disabled | CFG80/100 + SUM (00000h:1FFEFh) | 0xFD9E |
| | | Enabled | 0000h | |
| | PIC18F96J99 | Disabled | CFG80/100 + SUM (00000h:17FEFh) | 0x7D9E |
| | | Enabled | 0000h | |
| | PIC18F96J94 | Disabled | CFG80/100 + SUM (00000h:0FFEFh) | 0xFD9E |
| | | Enabled | 0000h | |
| | PIC18F95J94 | Disabled | CFG80/100 + SUM (00000h:07FEFh) | 0x7D9E |
| | | Enabled | 0000h | |
| | PIC18F87J94 | Disabled | CFG80/100 + SUM (00000h:1FFEFh) | 0xFD9E |
| | | Enabled | 0000h | |
| | PIC18F86J99 | Disabled | CFG80/100 + SUM (00000h:17FEFh) | 0x7D9E |
| | | Enabled | 0000h | |
| | PIC18F86J94 | Disabled | CFG80/100 + SUM (00000h:0FFEFh) | 0xFD9E |
| | | Enabled | 0000h | |
| | PIC18F85J94 | Disabled | CFG80/100 + SUM (00000h:07FEFh) | 0x7D9E |
| | | Enabled | 0000h | |
| | PIC18F67J94 | Disabled | CFG60 + SUM (00000h:1FFEFh) | 0xFCA6 |
| | | Enabled | 0000h | |
| | PIC18F66J99 | Disabled | CFG60 + SUM (00000h:17FEFh) | 0x7CA6 |
| | | Enabled | 0000h | |
| | PIC18F66J94 | Disabled | CFG60 + SUM (00000h:0FFEFh) | 0xFCA6 |
| | | Enabled | 0000h | |
| | PIC18F65J94 | Disabled | CFG60 + SUM (00000h:07FEFh) | 0x7CA6 |
| | | Enabled | 0000h | |

**Legend:** Item — Description
SUM(a:b) = Byte sum of locations, a to b, inclusive (all three bytes of code memory)
\+ = Addition

## 6.0 AC/DC CHARACTERISTICS AND TIMING REQUIREMENTS

**Standard Operating Conditions**
Operating Temperature: +25°C is recommended

| Param No. | Symbol | Characteristic | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| D111 | VDD | Supply Voltage During Programming | 2.20 | 3.60 | V | Normal programming(1) |
| D112 | IPP | Programming Current on $\overline{\text{MCLR}}$ | — | 5 | μA | |
| D113 | IDDP | Supply Current During Programming | — | 16 | mA | |
| D031 | VIL | Input Low Voltage | VSS | 0.2 VDD | V | |
| D041 | VIH | Input High Voltage | 0.8 VDD | VDD | V | |
| D080 | VOL | Output Low Voltage | — | 0.4 | V | IOL = 8.5 mA @ 3.6V |
| D090 | VOH | Output High Voltage | 3.0 | — | V | IOH = -3.0 mA @ 3.6V |
| D012 | CIO | Capacitive Loading on I/O Pin (PGEDx) | — | 50 | pF | To meet AC specifications |
| D013 | CF | Filter Capacitor Value on VCAP | 10 | — | μF | Required for controller core |
| D014 | CDEC | Decoupling capacitance between VDD and VSS | 1 | — | μF | |
| P1 | TPGEC | Serial Clock (PGCx) Period | 100 | — | ns | ICSP™ mode |
| P1A | TPGECL | Serial Clock (PGCx) Low Time | 40 | — | ns | ICSP mode |
| P1B | TPGECH | Serial Clock (PGCx) High Time | 40 | — | ns | ICSP mode |
| P2 | TSET1 | Input Data Setup Time to Serial Clock ↑ | 15 | — | ns | |
| P3 | THLD1 | Input Data Hold Time from PGCx ↑ | 15 | — | ns | |
| P4 | TDLY1 | Delay Between 4-Bit Command and Command Operand | 40 | — | ns | |
| P4A | TDLY1A | Delay Between 4-Bit Command Operand and Next 4-Bit Command | 40 | — | ns | |
| P5 | TDLY2 | Delay Between Last PGC ↓ of Command Byte to First PGC ↑ of the Read of Data Word | 20 | — | ns | |
| P6 | TSET2 | VDD ↑ Setup Time to $\overline{\text{MCLR}}$ | 100 | — | ns | |
| P7 | THLD2 | Input Data Hold Time from $\overline{\text{MCLR}}$ | 25 | — | ms | |
| P8 | TDLY3 | Delay Between Last PGCx ↓ of Command Byte to PGC ↑ of the Programming Executive | 12 | — | μs | |
| P9 | TDLY4 | Programming Executive Command Processing Time | 40 | — | μs | |
| P10 | TDLY6 | PGCx Low Time After Programming | 400 | — | ns | |
| P11 | TDLY7 | Chip Erase Time | 20 | 40 | ms | |
| P12 | TDLY8 | Page Erase Time | 20 | 40 | ms | |
| P13 | TDLY9 | Row Programming Time | 1.5 | — | ms | |
| P14 | TR | $\overline{\text{MCLR}}$ Rise Time to Enter ICSP mode | — | 1.0 | μs | |
| P15 | TVALID | Data Out Valid from PGCx ↑ | 10 | — | ns | |
| P16 | TDLY10 | Delay Between Last PGCx ↓ and $\overline{\text{MCLR}}$ ↓ | 0 | — | s | |
| P17 | THLD3 | $\overline{\text{MCLR}}$ ↓ to VDD ↓ | 100 | — | ns | |
| P18 | TKEY1 | Delay from First $\overline{\text{MCLR}}$ ↓ to First PCGx ↑ for the Key Sequence on PGDx | 10 | — | ms | |
| P19 | TKEY2 | Delay from Last PGCx ↓ for the Key Sequence on PGDx to the Second $\overline{\text{MCLR}}$ ↑ | 1 | — | ms | |
| P20 | TDLY11 | Delay Between the PGDx ↓ by the Programming Executive to PGDx, Driven by Host | 23 | — | μs | |
| P21 | TDLY12 | Delay Between Programming Executive Command Response Words | 8 | — | ns | |

**Note 1:** VDD must also be supplied to the AVDD pins during programming. AVDD and AVSS should always be within ±0.3V of VDD and Vss, respectively. When the internal voltage regulator is enabled, the nominal VCAP is 1.8V.

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