HCSXXX Memory Programming Specification

This document includes the programming specifications for the following devices:

- HCS200
- HCS201
- HCS300
- HCS301
- HCS320
- HCS360
- HCS361
- HCS362
- HCS410
- HCS412
- HCS500
- HCS512
- HCS515

1.0 PROGRAMMING THE HCSXXX

All of the KEELOQ® devices are programmed using a serial method. This Serial mode allows KEELOQ devices to be programmed while in users' systems, which increases the flexibility of designing cryptographic encoders, decoders and transponders into electronic systems. While some of the devices are capable of being programmed through wireless communications, the subject of this document is focused on wired programmers that make contact with the KEELOQ products while the components are in-circuit or in a programmer socket. Additionally, this programming specification only applies to all KEELOQ devices listed above in all packages.

Note:	For the purpose of this document, "KEELOQ devices" and "KEELOQ products" refers to all of the components listed above.

1.1 Programming Algorithm Requirements

Depending on the device being programmed, the method for entering Programming mode can be achieved through the use of a combination of logic level signals applied to the programming pins. One or two pins are capable of accepting clock signals, while another pin is dedicated to bidirectional data. These pins are detailed in Table 1-1.

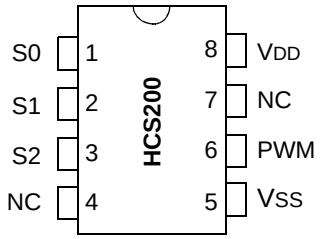
Additionally, the programming voltage range for VDD is +5V ± 10% for all the KEELOQ devices. There is not a requirement to apply high voltages to any of the pins beyond the level of VDD in order to enter the Programming mode. For more details about pin configurations during programming, refer to Table 1-1.

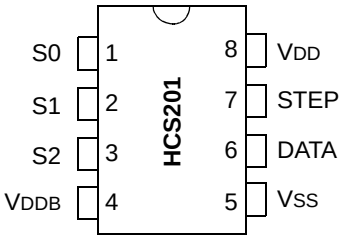
1.2 Program/Verify Mode

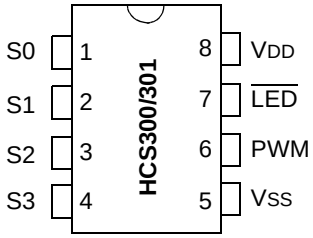
The Program/Verify mode for the KEELOQ devices allows programming for all memory locations within the device being programmed. With the exception of the decoders, these pins are also used to verify the memory arrays.

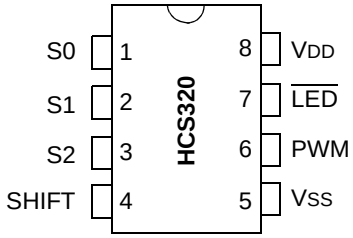
Pin Diagrams

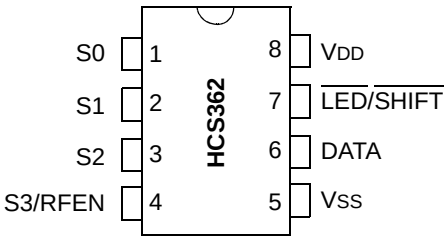
PDIP, SOIC

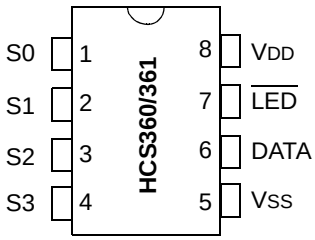


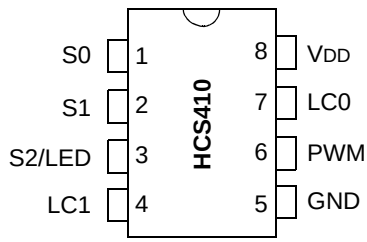


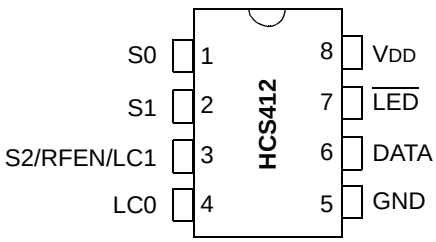


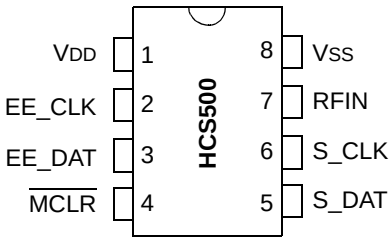






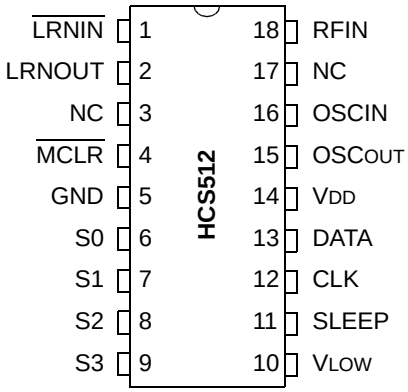


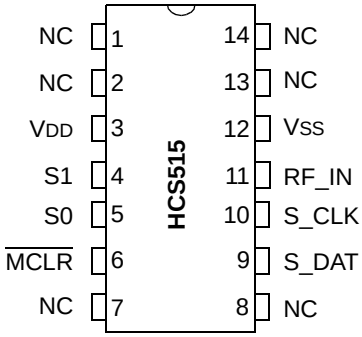




Pin Diagrams (Continued)

PDIP, SOIC





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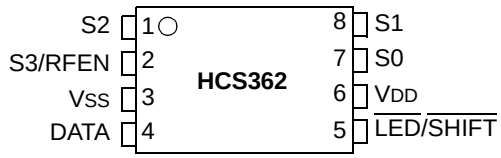


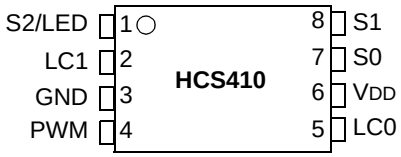


TABLE 1-1: PIN DESCRIPTIONS (DURING PROGRAMMING)

Device	Pin Number					Comments
	Power Supply	Ground	Clock	Data	Other	
HCS200	8	5	3	6	—	
HCS201	8	5	3	6	—	**(Notes 1)**
HCS300	8	5	3, 4	6	—	**(Notes 2)**
HCS301	8	5	3, 4	6	—	**(Notes 2)**
HCS320	8	5	3	6	—	**(Notes 2)**
HCS360	8	5	3, 4	6	2	**(Notes 2)**
HCS361	8	5	3, 4	6	2	**(Notes 2)**
HCS362	8	5	3, 4	6	—	**(Notes 2)**
HCS410	8	5	3	6	—	
HCS412	8	5	3	6	—	**(Note 1)**
HCS500	1	8	6	5	—	**(Notes 2, 3, 4, 7, 8)**
HCS512	14	5	12	13	4	**(Notes 5, 6, 8, 9)**
HCS515	3	12	10	9	—	**(Notes 7, 8)**

Note 1: Sends calibration pulse during ACK periods.

2: V_{DD} pin must be driven low after a Program/Verify cycle.

3: In-circuit programming recommended.

4: Used in conjunction with a Microchip Technology 24LC02B device.

5: $\overline{MCLR}$, pin 4, is used to enter Program mode.

6: Must apply external clock source to OSCIN while programming.

7: Requires command byte preceding data packet.

8: Verify function not available.

9: Uses checksum in data packet.

2.0 MEMORY MAPPING

The program memory maps for KEELOQ products begin at 0x000 and extend as shown in the tables that follow. As a device is being programmed, the address counter automatically increments to the next word location after receiving a data word. The memory maps for all KEELOQ encoders and transponders were designed so that each word is 16 bits wide. Decoder memory maps are 8 bits wide.

2.1 Encoder Memory Maps

TABLE 2-1: HCS200 12 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY_0	Word 0 (LSb's) of 64-bit crypt key
0x01	KEY_1	Word 1 of 64-bit crypt key
0x02	KEY_2	Word 2 of 64-bit crypt key
0x03	KEY_3	Word 3 (MSb's) of 64-bit crypt key
0x04	SYNC	16-bit synchronization value
0x05	Reserved	Set to 0x0000
0x06	SER_0	Word 0 (LSb's) of 32-bit serial number
0x07	SER_1	Word 1 (MSb's) of 32-bit serial number
0x08	SEED_0	Word 0 (LSb's) of 32-bit seed value
0x09	SEED_1	Word 1 (MSb's) of 32-bit seed value
0x0A	Reserved	Set to 0x0000
0x0B	CONFIG	Configuration Word

TABLE 2-2: HCS201 12 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY_0	Word 0 (LSb's) of 64-bit crypt key
0x01	KEY_1	Word 1 of 64-bit crypt key
0x02	KEY_2	Word 2 of 64-bit crypt key
0x03	KEY_3	Word 3 (MSb's) of 64-bit crypt key
0x04	SYNC	16-bit synchronization value
0x05	Reserved	Set to 0x0000
0x06	SER_0	Word 0 (LSb's) of 32-bit serial number
0x07	SER_1	Word 1 (MSb's) of 32-bit serial number
0x08	SEED_0	Word 0 (LSb's) of 32-bit seed value
0x09	SEED_1	Word 1 (MSb's) of 32-bit seed value
0x0A	DISC	Discrimination Word
0x0B	CONFIG	Configuration Word

TABLE 2-3: HCS300 12 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY_0	Word 0 (LSb's) of 64-bit crypt key
0x01	KEY_1	Word 1 of 64-bit crypt key
0x02	KEY_2	Word 2 of 64-bit crypt key
0x03	KEY_3	Word 3 (MSb's) of 64-bit crypt key
0x04	SYNC	16-bit synchronization value
0x05	Reserved	Set to 0x0000
0x06	SER_0	Word 0 (LSb's) of 32-bit serial number
0x07	SER_1(1)	Word 1 (MSb's) of 32-bit serial number
0x08	SEED_0	Word 0 (LSb's) of 32-bit seed value
0x09	SEED_1	Word 1 (MSb's) of 32-bit seed value
0x0A	Reserved	Set to 0x0000
0x0B	CONFIG	Configuration Word

Note 1: MSb of this word is used for auto-shutoff timer.

TABLE 2-4: HCS301 12 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY_0	Word 0 (LSb's) of 64-bit crypt key
0x01	KEY_1	Word 1 of 64-bit crypt key
0x02	KEY_2	Word 2 of 64-bit crypt key
0x03	KEY_3	Word 3 (MSb's) of 64-bit crypt key
0x04	SYNC	16-bit synchronization value
0x05	Reserved	Set to 0x0000
0x06	SER_0	Word 0 (LSb's) of 32-bit serial number
0x07	SER_1(1)	Word 1 (MSb's) of 32-bit serial number
0x08	SEED_0	Word 0 (LSb's) of 32-bit seed value
0x09	SEED_1	Word 1 (MSb's) of 32-bit seed value
0x0A	Reserved	Set to 0x0000
0x0B	CONFIG	Configuration Word

Note 1: MSb of this word is used for auto-shutoff timer.

TABLE 2-5: HCS320 12 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY_0	Word 0 (LSb's) of 64-bit crypt key
0x01	KEY_1	Word 1 of 64-bit crypt key
0x02	KEY_2	Word 2 of 64-bit crypt key
0x03	KEY_3	Word 3 (MSb's) of 64-bit crypt key
0x04	SYNC	16-bit synchronization value
0x05	Reserved	Set to 0x0000
0x06	SER_0	Word 0 (LSb's) of 32-bit serial number
0x07	SER_1(1)	Word 1 (MSb's) of 32-bit serial number
0x08	—	Not used
0x09	—	Not used
0x0A	Reserved	Set to 0x0000
0x0B	CONFIG	Configuration Word

Note 1: MSb of this word is used for auto-shutoff timer.

TABLE 2-6: HCS360 12 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY_0	Word 0 (LSb's) of 64-bit crypt key
0x01	KEY_1	Word 1 of 64-bit crypt key
0x02	KEY_2	Word 2 of 64-bit crypt key
0x03	KEY_3	Word 3 (MSb's) of 64-bit crypt key
0x04	SYNC_A	16-bit synchronization value A
0x05	SYNC_B	16-bit synchronization value B or Seed Value (Word 2)
0x06	Reserved	Set to 0x0000
0x07	SEED_0	Word 0 (LSb's) of 32-bit seed value
0x08	SEED_1	Word 1 (MSb's) of 32-bit seed value
0x09	SER_0	Word 0 (LSb's) of 32-bit serial number
0x0A	SER_1	Word 1 (MSb's) of 32-bit serial number
0x0B	CONFIG	Configuration Word

TABLE 2-7: HCS361 12 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY_0	Word 0 (LSb's) of 64-bit crypt key
0x01	KEY_1	Word 1 of 64-bit crypt key
0x02	KEY_2	Word 2 of 64-bit crypt key
0x03	KEY_3	Word 3 (MSb's) of 64-bit crypt key
0x04	SYNC_A	16-bit synchronization value A
0x05	SYNC_B/SEED_2	16-bit synchronization value B or Seed Value (Word 2)
0x06	Reserved	Set to 0x0000
0x07	SEED_0	Word 0 (LSb's) of 32-bit seed value
0x08	SEED_1	Word 1 (MSb's) of 32-bit seed value
0x09	SER_0	Word 0 (LSb's) of 32-bit serial number
0x0A	SER_1	Word 1 (MSb's) of 32-bit serial number
0x0B	CONFIG	Configuration Word

TABLE 2-8: HCS362 18 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY1_0	Word 0 (LSb's) of 64-bit crypt key 1
0x01	KEY1_1	Word 1 of 64-bit crypt key 1
0x02	KEY1_2	Word 2 of 64-bit crypt key 1
0x03	KEY1_3	Word 3 (MSb's) of 64-bit crypt key 1
0x04	KEY2_0	Word 0 (LSb's) of 64-bit crypt key 2
0x05	KEY2_1	Word 1 of 64-bit crypt key 2
0x06	KEY2_2	Word 2 of 64-bit crypt key 2
0x07	KEY2_3	Word 3 (MSb's) of 64-bit crypt key 2
0x08	SEED_0	Word 0 (LSb's) of 64-bit seed value
0x09	SEED_1	Word 1 of 64-bit seed value
0x0A	SEED_2	Word 2 of 64-bit seed value
0x0B	SEED_3	Word 3 (MSb's) of 64-bit seed value
0x0C	CONFIG_0	Configuration Word (LSb's)
0x0D	CONFIG_1	Configuration Word (MSb's)
0x0E	SERIAL_0	Word 0 (LSb's) of 32-bit serial number
0x0F	SERIAL_0	Word 1 (MSb's) of 32-bit serial number
0x10	SYNC	16-bit synchronization value
0x11	Reserved	Set to 0x0000

TABLE 2-9: HCS500 9 X 8-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	CONFIG	Configuration Word
0x01	KEY0	Byte 0 (LSb's) of 64-bit manufacturer key
0x02	KEY1	Byte 1 of 64-bit manufacturer key
0x03	KEY2	Byte 2 of 64-bit manufacturer key
0x04	KEY3	Byte 3 of 64-bit manufacturer key
0x05	KEY4	Byte 4 of 64-bit manufacturer key
0x06	KEY5	Byte 5 of 64-bit manufacturer key
0x07	KEY6	Byte 6 of 64-bit manufacturer key
0x08	KEY7	Byte 7 (MSb's) of 64-bit manufacturer key

TABLE 2-10: HCS512 10 X 8-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY0	Byte 0 (LSb's) of 64-bit manufacturer key
0x01	KEY1	Byte 1 of 64-bit manufacturer key
0x02	KEY2	Byte 2 of 64-bit manufacturer key
0x03	KEY3	Byte 3 of 64-bit manufacturer key
0x04	KEY4	Byte 4 of 64-bit manufacturer key
0x05	KEY5	Byte 5 of 64-bit manufacturer key
0x06	KEY6	Byte 6 of 64-bit manufacturer key
0x07	KEY7	Byte 7 (MSb's) of 64-bit manufacturer key
0x08	CONFIG	Configuration byte
0x09	Checksum	Checksum byte

TABLE 2-11: HCS515 9 X 8-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	CONFIG	Configuration byte
0x01	KEY0	Byte 0 (LSb's) of 64-bit manufacturer key
0x02	KEY1	Byte 1 of 64-bit manufacturer key
0x03	KEY2	Byte 2 of 64-bit manufacturer key
0x04	KEY3	Byte 3 of 64-bit manufacturer key
0x05	KEY4	Byte 4 of 64-bit manufacturer key
0x06	KEY5	Byte 5 of 64-bit manufacturer key
0x07	KEY6	Byte 6 of 64-bit manufacturer key
0x08	KEY7	Byte 7 (MSb's) of 64-bit manufacturer key

2.2 Transponder Memory Maps

TABLE 2-12: HCS410 16 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY_0	Word 0 (LSb's) of 64-bit crypt key
0x01	KEY_1	Word 1 of 64-bit crypt key
0x02	KEY_2	Word 2 of 64-bit crypt key
0x03	KEY_3	Word 3 (MSb's) of 64-bit crypt key
0x04	DISC	Ext. Config. Word/10-bit Discriminator
0x05	CONFIG	16-bit Configuration Word
0x06	SER_0	Word 0 (LSb's) of 32-bit serial number
0x07	SER_1	Word 1 (MSb's) of 32-bit serial number
0x08	SEED_0	Word 0 (LSb's) of 64-bit seed value
0x09	SEED_1	Word 1 of 64-bit seed value
0x0A	SEED_2	Word 2 of 64-bit seed value
0x0B	SEED_3	Word 3 (MSb's) of 64-bit seed value
0x0C	USR_0	Word 0 (LSb's) of 64-bit user area
0x0D	USR_1	Word 1 of 64-bit user area
0x0E	USR_2	Word 2 of 64-bit user area
0x0F	USR_3	Word 3 (MSb's) of 64-bit user area SYNC

TABLE 2-13: HCS412 18 X 16-BIT EEPROM MEMORY MAP

Word Address	Mnemonic	Description
0x00	KEY0	Word 0 (LSb's) of 64-bit crypt key 1
0x01	KEY1	Word 1 of 64-bit crypt key 1
0x02	KEY2	Word 2 of 64-bit crypt key 1
0x03	KEY3	Word 3 (MSb's) of 64-bit crypt key 1
0x04	SEED0	Word 0 (LSb's) of 60-bit seed value
0x05	SEED1	Word 1 of 60-bit seed value
0x06	SEED2	Word 2 of 60-bit seed value
0x07	CFG/SEED3	Word 3 of 60-bit seed value/Configuration in top nibble
0x08	CONFIG1	Configuration Word 1 (security options)
0x09	CONFIG2	Configuration Word 2
0x0A	SER0	Word 0 (LSb's) of 32-bit serial number
0x0B	SER1	Word 1 (MSb's) of 32-bit serial number
0x0C	USR0	Word 0 (LSb's) of 64-bit user area
0x0D	USR1	Word 1 of 64-bit user area
0x0E	USR2	Word 2 of 64-bit user area
0x0F	USR3	Word 3 (MSb's) of 64-bit user area

2.3 Entering Program Mode

Entering the Program/Verify mode will be dependent upon the type of device in use. Most KEELOQ devices use a serial clock and bidirectional data line to access the chips' memory maps. In order to enter the Programming mode, a Start condition is sent to the target device, where the clock and data lines must be held high and low for specified periods of time. That is, all lines are held low while the clock line is driven high. After a short delay, the data line is driven high. At this point, both lines must remain high for another delay period prior to dropping back to ground. After dropping both lines low and providing another delay, the state machine for the KEELOQ device will enter the Programming mode and begin to wait for data, or depending on the component, a bulk erase is performed on the memory array.

For the HCS360 and HCS361 devices, the Programming mode is entered by providing a clock source on the clock line and a Start pulse on the data line, as described in the previous paragraph. However, the difference is with driving the S1 pin, as shown in Figure 5-5. Bit 0 of the data packet must be driven on the S1 pin and kept at that level throughout the programming cycles and through verification.

The HCS512 is another device that does not conform to the 2-wire protocol described above. For this device, the $\overline{\text{MCLR}}$ pin is driven high while data is held low. After the minimum setup time has been realized, the clock pin is driven high and then low for a minimum amount of time in order to send the HCS512 a Start condition and complete the Entry mode for the next programming sequence. The associated waveform is detailed in **Section 5.0 "Program/Verify Mode Electrical Characteristics"**. The HCS512 is also the only device that requires a checksum be sent to the target device while it is being programmed. See the Checksum Section in the HCS512 Data Sheet, "*KEELOQ® Code Hopping Decoder*" (DS40151), for details on calculating the checksum.

Note:	The HCS512 requires an external clock signal for the OSCIN pin. This signal is necessary throughout the Programming mode.

2.4 Bulk Write Device

All transponders and encoders are bulk erased and programmed with zeros following the Start condition. The bulk erase/write time frame is specified as TPBW, which is minimally 4.0 ms. After the bulk function is complete, the programming state machine continues into the Program mode where it begins to wait for data and clock signals.

2.5 Serial Program/Verify Operation

For all of the encoders and transponders, the memory maps have been designed to be in 16-bit format, which means that each address location contains 16 bits of information including “don't care” bits that are read as zeros. Details relating to the designated pins for clock and data signals are outlined in Table 1-1. The decoders, on the other hand, were designed with memory maps in 8-bit format, so they are discussed separately in the next couple of paragraphs.

For specific information relating to the size of the memory maps for a given family of devices, be sure to review the tables in **Section 2.1 “Encoder Memory Maps”**.

The following paragraphs were written with the assumption that the target device has been placed into the Programming mode and is now waiting for data or a command byte to continue programming the memory array.

2.5.1 ENCODERS/TRANSPONDERS

To input data to the target KEELOQ encoder or transponder, 16 clock cycles are applied to the clock pin of the target device while data is driven into the data pin. Data is clocked into the target device on the falling edge of the clock signal. Also, the minimum high time and low time for the clock signals are 50 µs. During verification, data must be sampled on the rising edge of the clock.

2.5.2 DECODERS

To input data to the target KEELOQ decoder, 8 clock cycles are applied to the clock pin of the target device while data is driven into the data pin. Data is clocked into the target device on the falling edge of the clock signals. Also, the minimum high time and minimum low time for the clock signals are 50 µs. For the decoder family, there are no verification functions.

2.6 Begin Programming

Write cycles are performed a bit-at-a-time throughout the entire programming sequence for KEELOQ products. The total write cycle, which includes internal processing and programming time, is specified to take a minimum of 50 ms. As a result, programmers can include a delay for the minimum write cycle time or they can poll the target device as discussed in **Section 2.7 “Polling Write Cycle”**.

2.7 Polling Write Cycle

2.7.1 HCS201 AND HCS412

Once the 16th clock cycle for the data word has been generated and the next minimum low time for the clock passes, the clock pin can be driven high to poll the completion of the write cycle. Before the write cycle is complete, the data pin for the target KEELOQ device will be low. After the write cycle is complete, the data pin on the HCS201 and the HCS412 will begin to provide pulses to the programmer in order to signal the completion of the write cycle. As a result, the programmer data pin should be set to high-impedance (input) so that it can read the pulses. After reading the pulses on the data pin, the programmer should drive the clock pin low and make the data pin an output so that data can continue to be driven into the target device. These pulses can be used for calibration sequences for the HCS201 and the HCS412. For information relating to oscillator calibration refer to **Section 5.0 “Program/Verify Mode Electrical Characteristics”**, which discusses oscillator tuning. If the programmer polls the target device for the end of a write cycle, these two devices will continue to emit calibration pulses until their clock lines are driven low. In order to measure the calibration pulses, the clock pin must be driven high prior to the end of the write cycle, otherwise the calibration pulses will not appear.

2.7.2 ALL OTHER KEELOQ DEVICES

Once the 16th clock cycle for the data word has been generated for any of the encoders or transponders or the last clock cycle for a decoder data packet is generated, the clock pin can be driven high to poll for the completion of the write cycle. Before the write cycle is complete, the data pin for the target KEELOQ device will be low. As a result, the programmer data pin should be set to high-impedance (input) so that it can sense the rising edge of data. After the write cycle is complete, the data pin will be driven high until the clock line is driven low again.

2.8 Verify Mode

In terms of verify operations, all KEELOQ encoders and transponders incorporate a security feature that only allows one verify operation to be completed, and it must be completed at the end of the programming sequence before exiting the Programming mode.

When implementing polling routines to sense the end of the last write cycle and after driving the clock line low, the programmer can begin to read data by continuing to provide clock cycles to the target device. Note that there is not an Acknowledge bit from KEELOQ devices during the Verify mode.

In the case where the programmer provides a time delay to allow for write cycle completion, the programmer can provide clock cycles after the delay to begin reading data.

Note:	Decoders do not incorporate a verify function.

3.0 CONFIGURATION WORD

For detailed descriptions of bit functions for the configuration words of the KEELOQ devices, be sure to download the latest Data Sheet for the respective device from the Microchip Technology web site (www.microchip.com). Configuration word architectures are also shown earlier in **Section 2.0 "Memory Mapping"**.

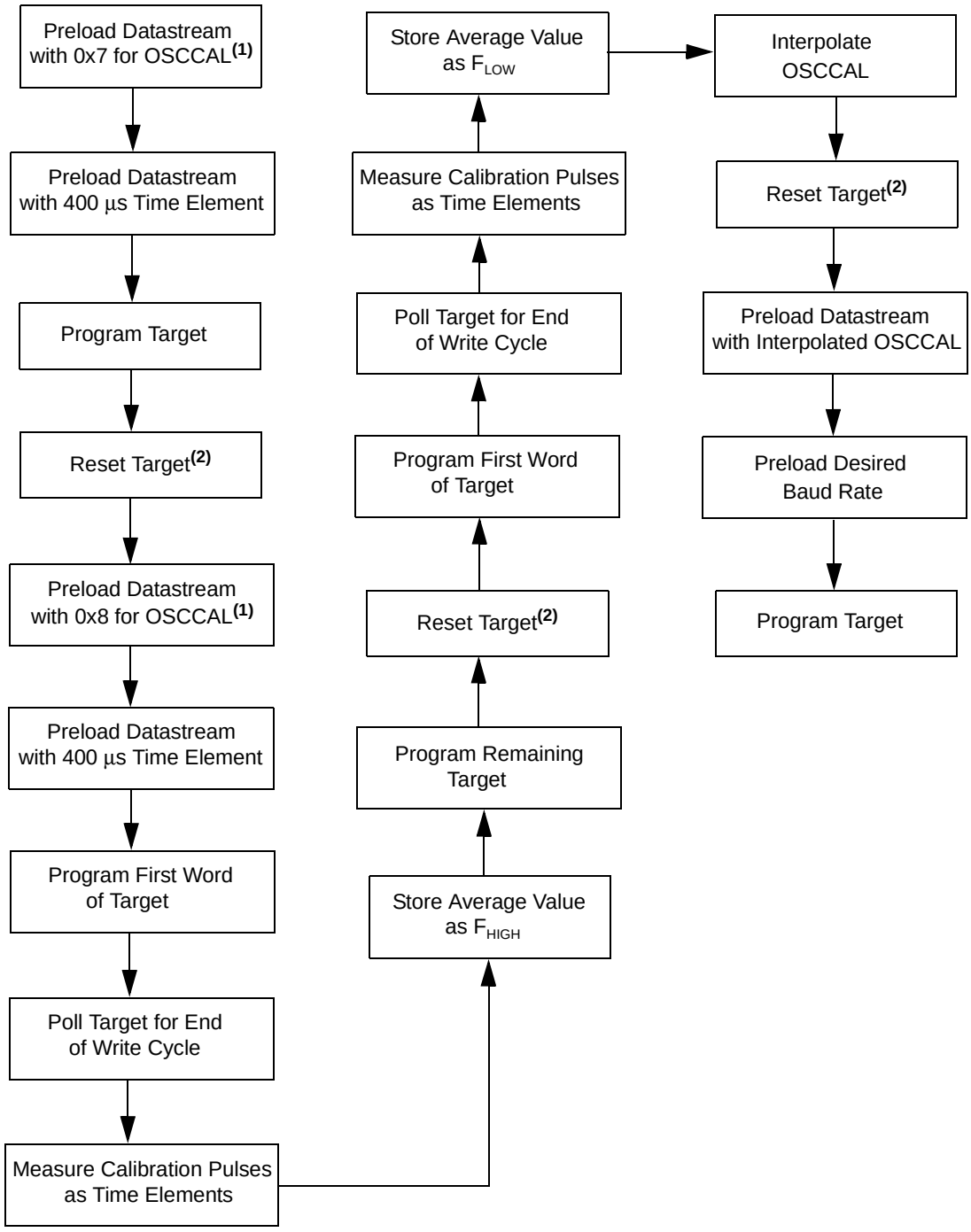
4.0 OSCILLATOR TUNING

Calibrating the oscillator of select devices can be completed a number of ways. For the purpose of this document, calibration will be completed using the Two-Point Calibration Algorithm, which is described in Application Note AN824, "*KEELOQ® Encoders Oscillator Calibration*" (DS00824). The algorithm is as follows:

- OSCCAL = -8
- Program target device
- Measure oscillator frequency FHIGH
- OSCCAL = +7
- Program target device
- Measure oscillator frequency FLOW
- Interpolate:
  - OSCCAL = 16*(FIDEAL - FLOW)/(FHIGH - FLOW)
- Program target device

For a better understanding of how to implement this algorithm, the following flow charts are being provided:

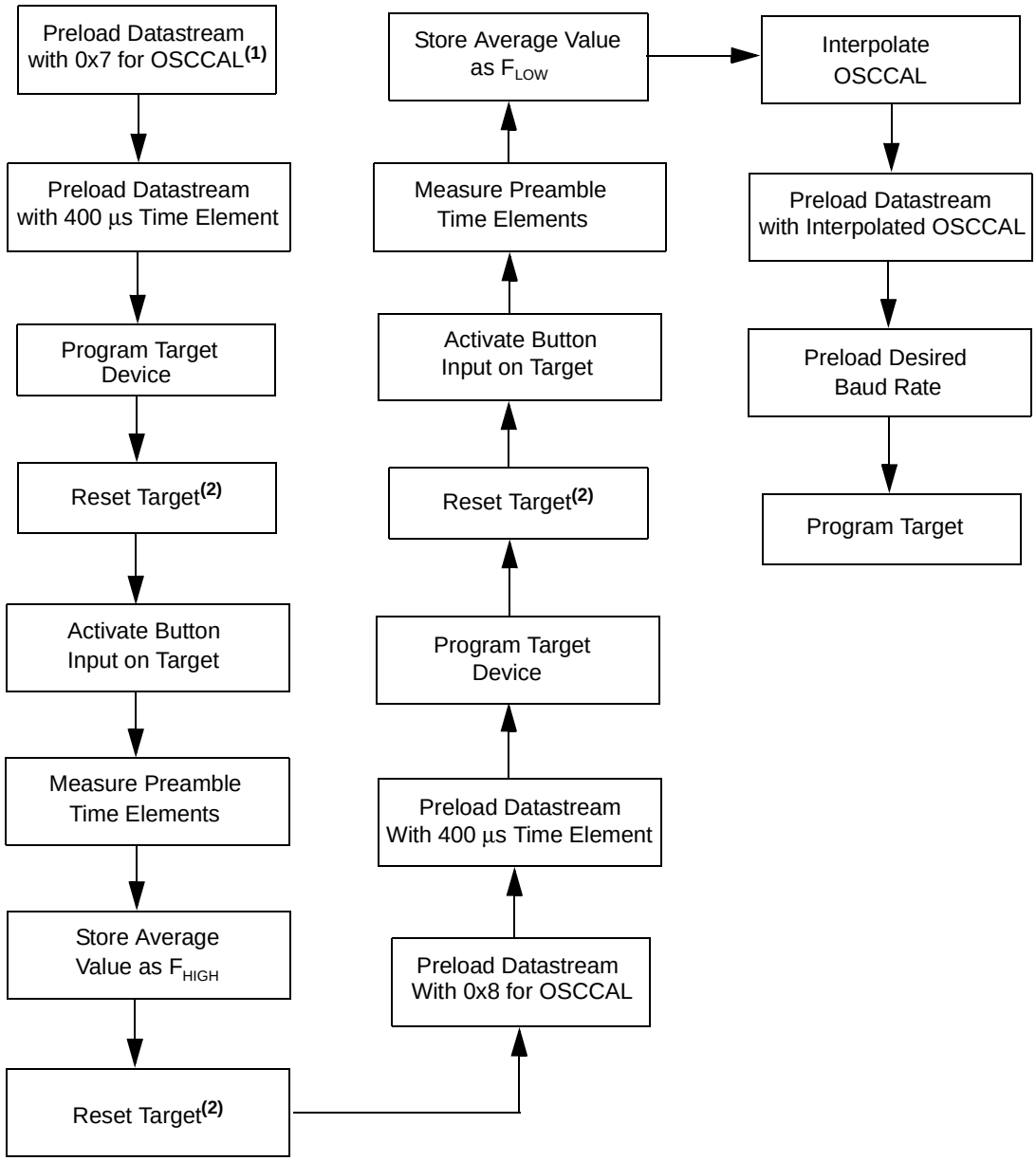
FIGURE 4-1: HCS201 AND HCS412 OSCILLATOR TUNING



Note 1: -8_d = 0x7, and $+7_d$ = 0x8

2: Cycle Power

FIGURE 4-2: HCS362 AND HCS410 OSCILLATOR TUNING



Note 1: -8_d = 0x7, and $+7_d$ = 0x8

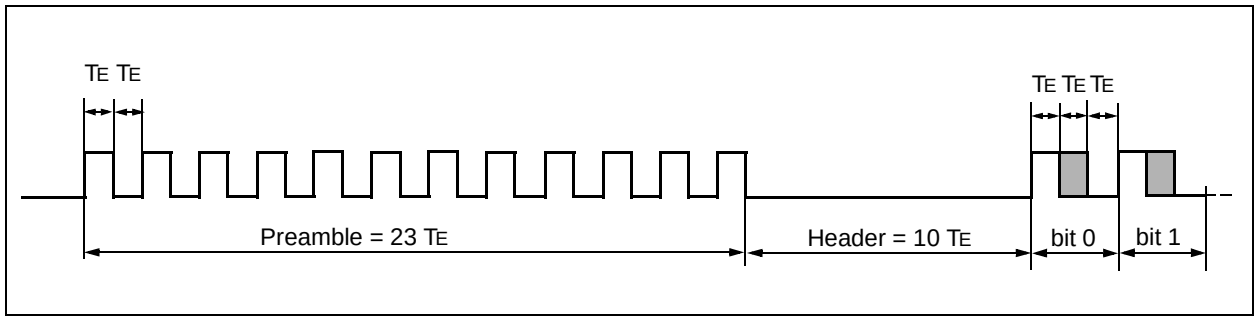
2: Cycle Power

KEELOQ devices that are capable of oscillator tuning include the HCS201, HCS362, HCS410 and the HCS412. Though, only the HCS201 and HCS412 transmit calibration pulses when polling the chips at the end of write cycles.

The other two devices must be tuned according to the preamble pulses that they transmit at the beginning of a data packet. For the best accuracy, use multiple time elements to achieve an average time element value. Typically, a number that is a power of 2^n is used in order to simplify the resultant quotient (i.e., 4 or 8). In order to obtain the most accurate time element measurement, the widest possible baud rate should be chosen. For simplifying the two flow diagrams below, a common time element was chosen to the devices that share algorithms.

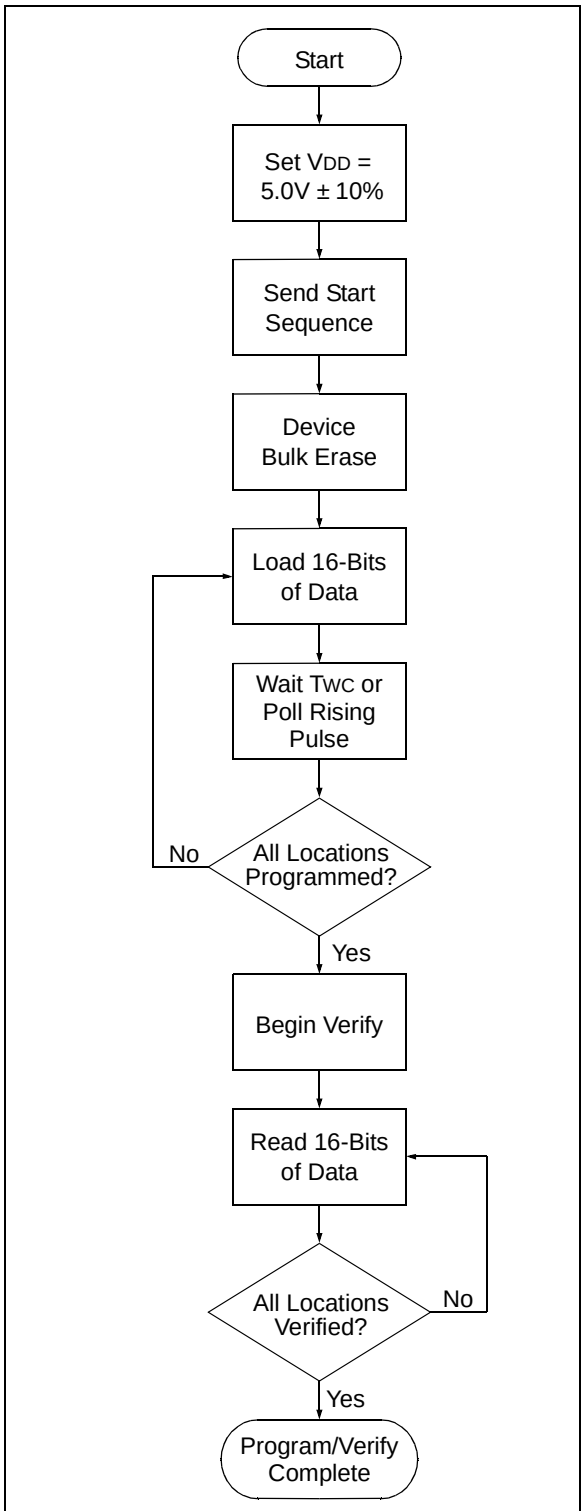
The HCS362 and the HCS410 oscillator tuning register can also be tuned as shown in the algorithm above, but with the caveat that after the device is programmed, the programmer must activate the target device in order to measure the time element in the communication preamble. A typical preamble is shown in Figure 4-3.

FIGURE 4-3: PWM CODE WORD TRANSMISSION TIMINGS



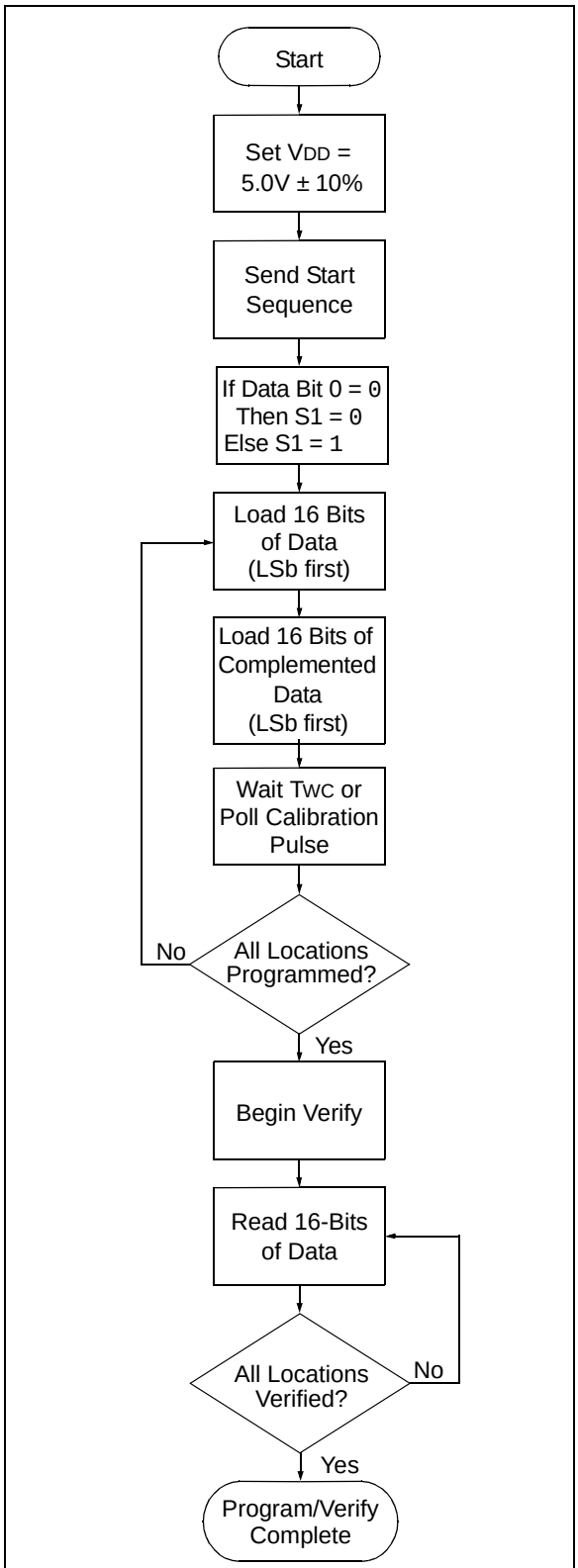
4.1 Programming Flow Charts

FIGURE 4-4: PROGRAMMING FLOW CHART 1



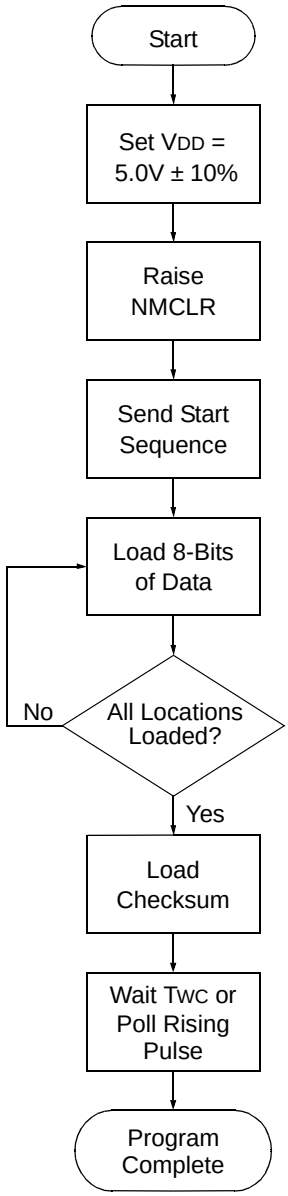
Note: Applies to HCS200, HCS201, HCS300, HCS301, HCS320, HCS362, HCS410 and HCS412 only.

FIGURE 4-5: PROGRAMMING FLOW CHART 2



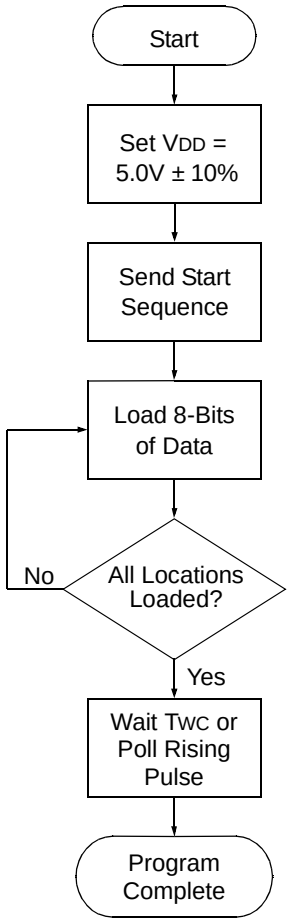
Note: Applies to HCS360 and HCS361 only.

FIGURE 4-6: PROGRAMMING FLOW CHART 3



Note: Applies to HCS512 only.

FIGURE 4-7: PROGRAMMING FLOW CHART 4



Note: Applies to HCS500 and HCS515 only.

5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

5.1 Timing Requirements for Program/Verify Mode – Encoders

AC/DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating Temperature +25°C ± 5°C Operating Voltage 4.5V ≤ VDD ≤ 5.5V			
Sym	**Characteristics**	**Min**	**Max**	**Units**	**Conditions/Comments**
HCS200, HCS300, HCS301, HCS320 and HCS362					
TCLKH	Clock high time	50	—	µs	
TCLKL	Clock low time	50	—	µs	
TDH	Data hold time	30	—	µs	
TDS	Data setup time	0	—	µs	
TDV	Data out valid time	—	30	µs	
TPBW	Bulk Write time	4.0	—	ms	
TPH1	Hold Time 1	3.5	—	ms	
TPH2	Hold Time 2	50	—	µs	
TPROG	Program delay time	4.0	—	ms	
TPS	Program mode setup time	3.5	4.5	ms	
TWC	Program cycle time	50	—	ms	
HCS201					
TACKH	Data out valid time	800	—	µs	
TACKL	Data hold time	800	—	µs	
TCLKH	Clock high time	50	—	µs	
TCLKL	Clock low time	50	—	µs	
TDH	Data hold time	18	—	µs	
TDS	Data setup time	0	—	µs	
TDV	Data out valid time	—	30	µs	
TPBW	Bulk Write time	4.0	—	ms	
TPH1	Hold Time 1	4.0	—	ms	
TPH2	Hold Time 2	50	—	µs	
TPHOLD	Hold time	100	—	µs	
TPROG	Program delay time	4.0	—	ms	
TPS	Program mode setup time	2.0	5.0	ms	
TWC	Program cycle time	50	—	ms	
HCS360, HCS361					
T_1	Hold Time 1	9.0	—	ms	
T_2	Program mode setup time	0	4.0	ms	
TCLKH	Clock high time	50	—	µs	
TCLKL	Clock low time	50	—	µs	
TDH	Data hold time	30	—	µs	
TDS	Data setup time	0	—	µs	
TDV	Data out valid time	—	30	µs	
TWC	Program cycle time	50	—	ms	

5.2 Timing Requirements for Program/Verify Mode – Transponders

AC/DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating Temperature +25°C ± 5°C Operating Voltage 4.5V ≤ V_{DD} ≤ 5.5V			
Sym	**Characteristics**	**Min**	**Max**	**Units**	**Conditions/Comments**
HCS410, HCS412					
T_{AS}	ACK start time	100	—	µs	
T_{CLKH}	Clock high time	50	—	µs	
T_{CLKL}	Clock low time	50	—	µs	
T_{DH}	Data hold time	20	—	µs	
T_{DS}	Data stable time	20	—	µs	
T_{DV}	Data valid time	—	20	µs	
T_{PH1}	Program Hold Time 1	4	—	ms	
T_{PH2}	Program Hold Time 2	100	—	µs	
T_{PROG}	Bulk write time	2.2	—	ms	
T_{PS}	Program mode setup time	3	5	ms	
T_{WC}	EEPROM write time	36	—	ms	

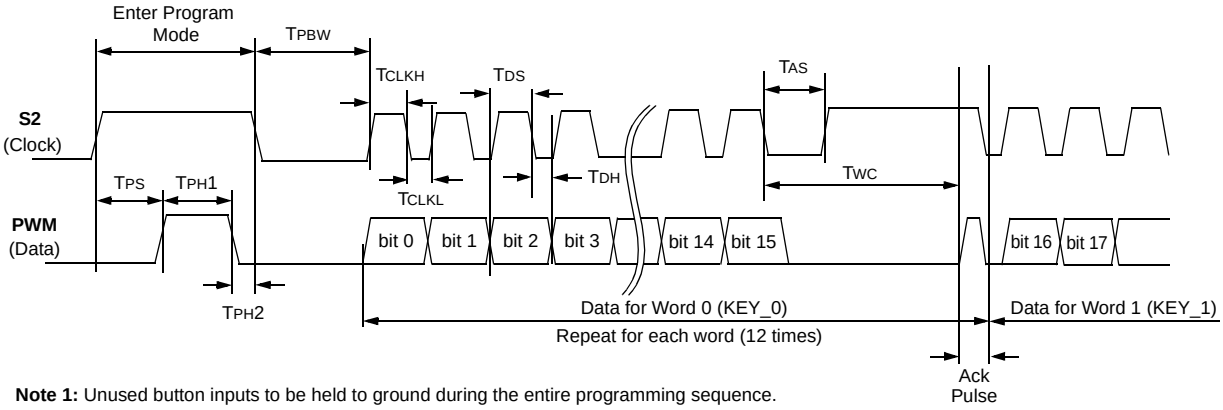
5.3 Timing Requirements for Program/Verify Mode – Decoders

AC/DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating Temperature +25°C ± 5°C Operating Voltage 4.5V ≤ VDD ≤ 5.5V				
Sym	**Characteristics**	**Sugg. Value**	**Min**	**Max**	**Units**	**Conditions/Comments**
HCS500						
TPP1	Command request time	—	—	500	ms	
TPP2	Decoder acknowledge time	—	—	1	ms	
TPP3	Start Command mode to first command bit	20	—	1000	µs	
TPP4	Data line low before tri-stated	—	—	5	µs	
TCLKH	Clock high time	20	—	1000	µs	
TCLKL	Clock low time	20	—	1000	µs	
FCLK	Clock frequency	500	—	25000	Hz	
TDS	Data hold time	—	—	5	µs	
TCMD	Command validate time	—	—	10	µs	
TACK	Command acknowledge time	30	—	240	ms	
TWT2	Acknowledge respond time	20	—	1000	µs	
TALW	Data low after clock low	—	—	10	µs	
HCS512						
TACK	Acknowledge time	—	—	80	ms	FOSC = 4 MHz
TACKH	Acknowledge duration	—	1	—	ms	FOSC = 4 MHz
TCLKH	Clock high time	—	0.05	320	ms	FOSC = 4 MHz
TCLKL	Clock low time	—	0.05	320	ms	FOSC = 4 MHz
TPH1	Hold Time 1	—	8	128	ms	FOSC = 4 MHz
TPH2	Hold Time 2	—	0.05	320	ms	FOSC = 4 MHz
TPS	Program mode setup time	—	1	64	ms	FOSC = 4 MHz
HCS515						
TACK	Command acknowledge time	*	30	240	ms	
TCLKH	Clock high time	100	20	1000	µs	
TCLKL	Clock low time	100	20	1000	µs	
TDATA	Command last bit to data first bit	100	10	1000	µs	
TDS	Data hold time	50	14	1000	µs	
TREQ	Command request time	*	0.005	500	ms	
TRESP	Acknowledge time	100	10	1000	µs	
TSTART	Command request to first command bit	100	20	1000	µs	
TWTH	Acknowledge respond time	100	20	1000	µs	
TWTL	Clock low to next command	100	10	—	µs	

* Depends on decoder status.

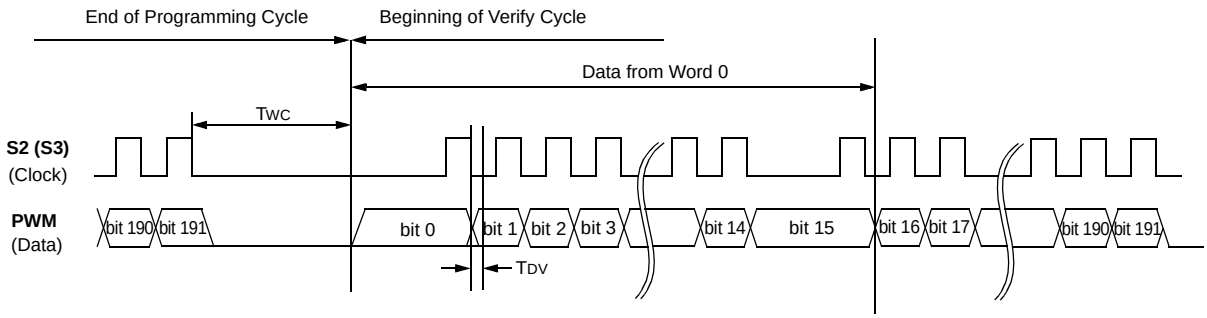
5.4 Programming Waveforms (HCS200, HCS300, HCS301, HCS320, HCS362)

FIGURE 5-1: PROGRAMMING WAVEFORMS



Note 1: Unused button inputs to be held to ground during the entire programming sequence.

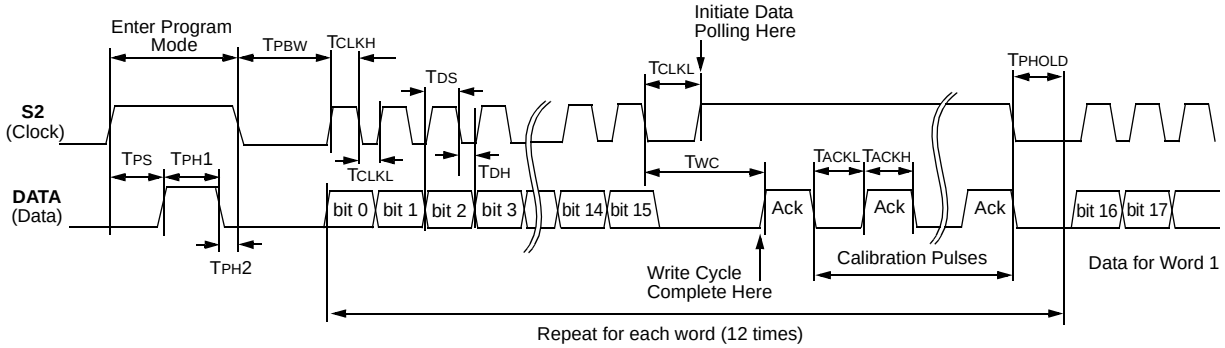
FIGURE 5-2: VERIFY WAVEFORMS



Note: If a Verify operation is to be done, then it must immediately follow the Program cycle.

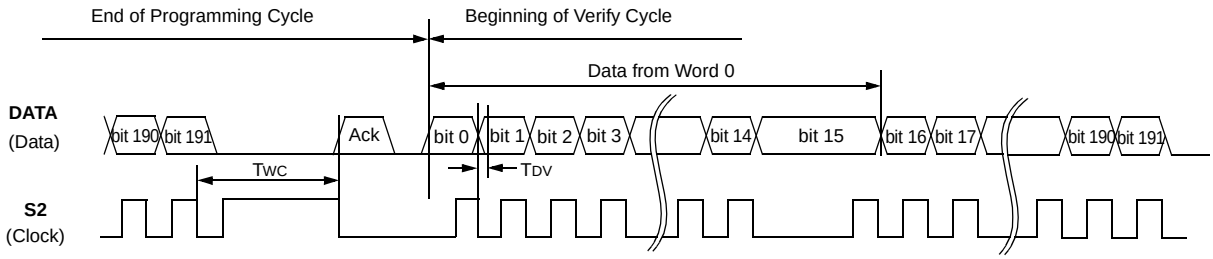
5.5 Programming Waveforms (HCS201)

FIGURE 5-3: PROGRAMMING WAVEFORMS (HCS201)



Note: S0 and S1 button inputs to be held to ground during the entire programming sequence.

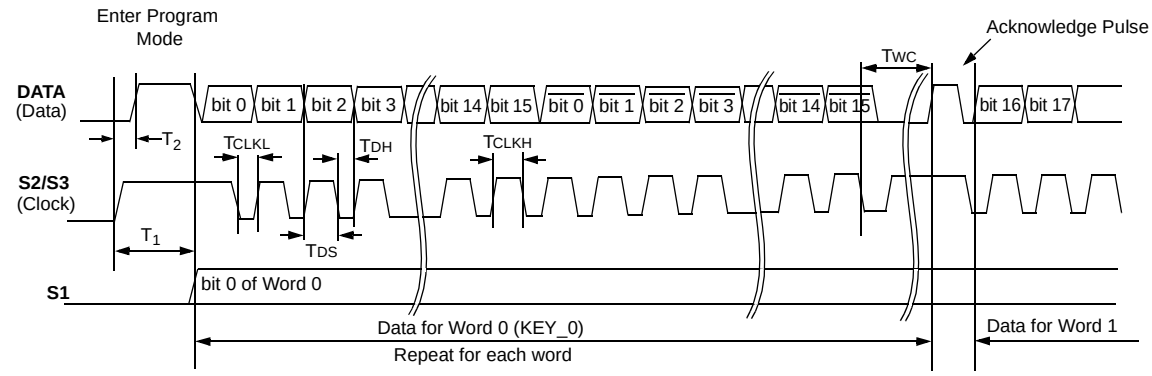
FIGURE 5-4: VERIFY WAVEFORMS



Note: If a Verify operation is to be done, then it must immediately follow the Program cycle.

5.6 Programming Waveforms (HCS360, HCS361)

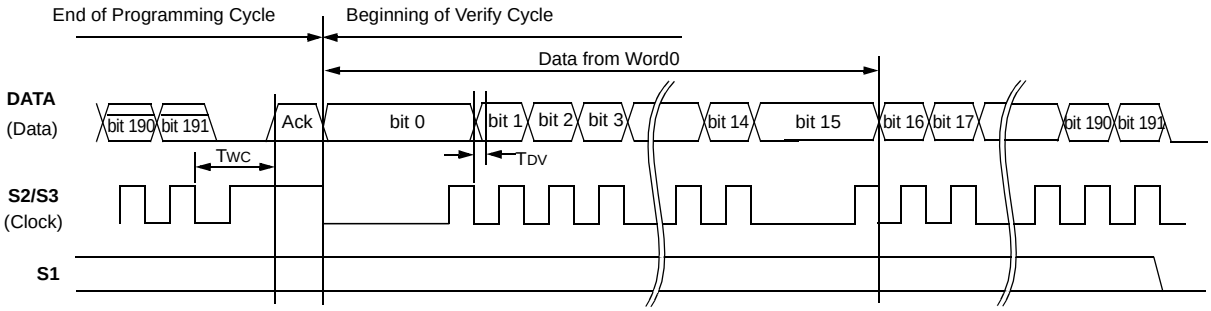
FIGURE 5-5: PROGRAMMING WAVEFORMS



Note 1: Unused button inputs to be held to ground during the entire programming sequence.

2: The V_{DD} pin must be taken to ground after a Program/Verify cycle.

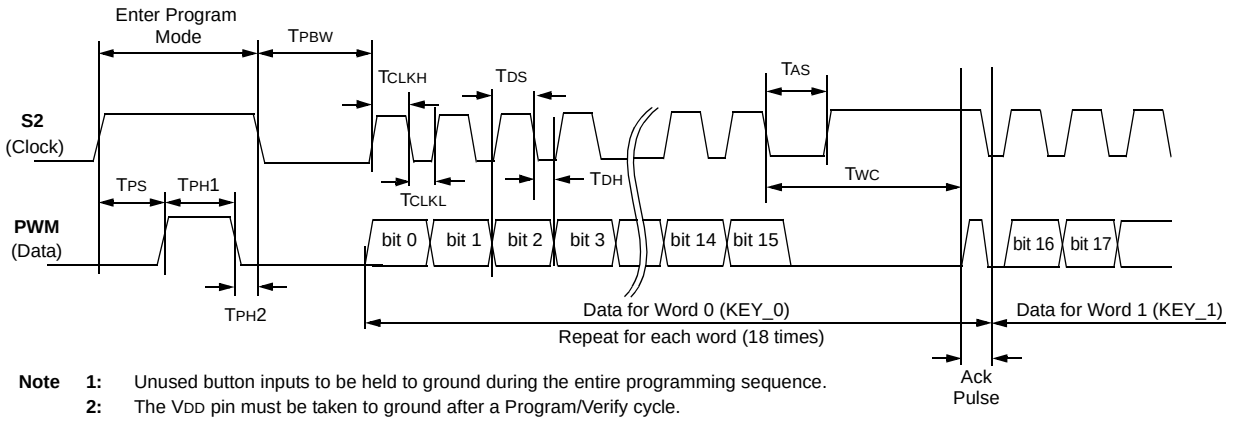
FIGURE 5-6: VERIFY WAVEFORMS



Note 1: A Verify sequence is performed only once immediately after the Program cycle.

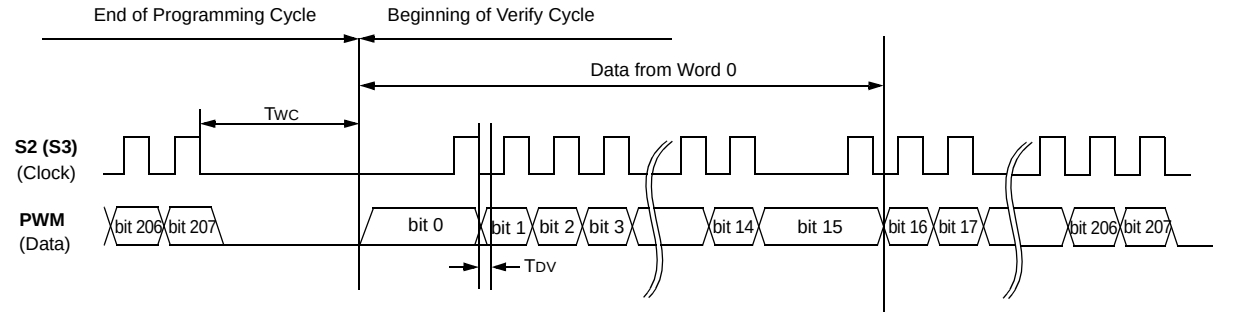
5.7 Programming Waveforms (HCS410, HCS412)

FIGURE 5-7: PROGRAMMING WAVEFORMS



Note 1: Unused button inputs to be held to ground during the entire programming sequence.
2: The VDD pin must be taken to ground after a Program/Verify cycle.

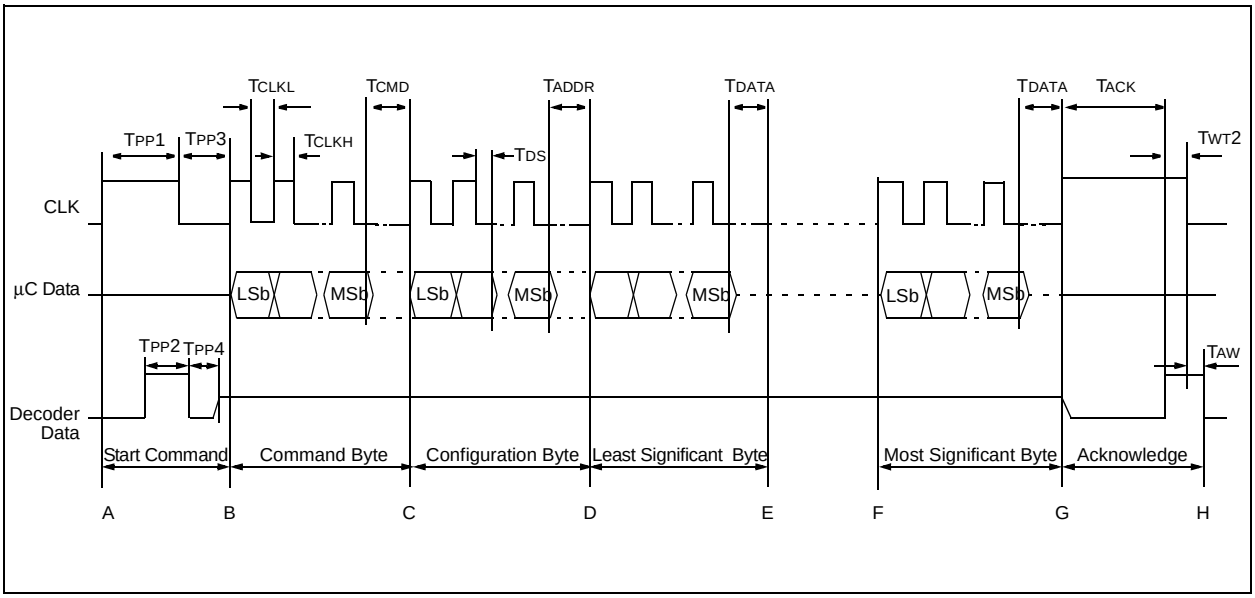
FIGURE 5-8: VERIFY WAVEFORMS



Note: If a Verify operation is to be done, then it must immediately follow the Program cycle.

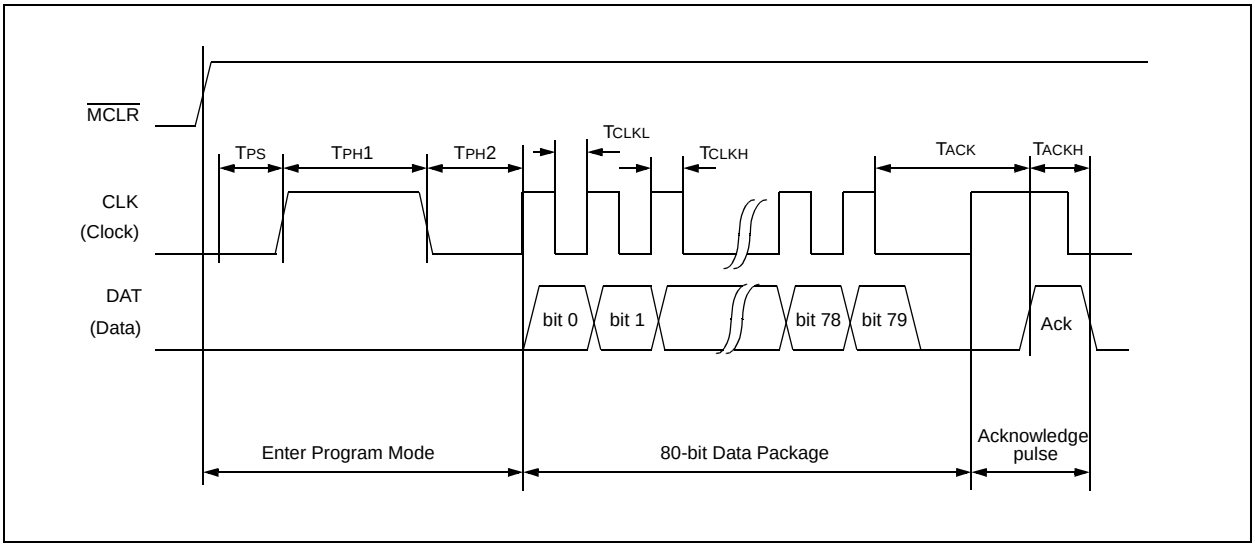
5.8 Programming Waveforms (HCS500)

FIGURE 5-9: PROGRAMMING WAVEFORMS



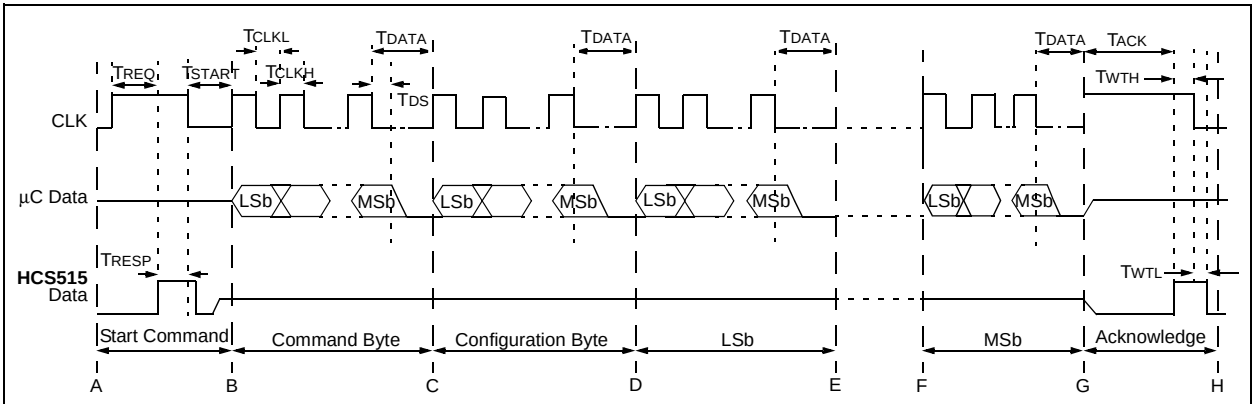
5.9 Programming Waveforms (HCS512)

FIGURE 5-10: PROGRAMMING WAVEFORMS



5.10 Programming Waveforms (HCS515)

FIGURE 5-11: PROGRAMMING WAVEFORMS



Note: The programming command consists of the following:

- Command Request Sequence (A to B)
- Command Byte (B to C)
- Configuration Byte (C to D)
- Manufacturer's Code Eight Data Bytes (D to G)
- Activation and Acknowledge Sequence (G to H)

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