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DC/DC LLC Reference Design Using the dsPIC® DSC

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Of the many DC/DC converter topologies available today, a designer usually selects one of them as a trade-off between a number of contrasting needs. Most often, the important features that are pursued in the design process are efficiency, power density (i.e., size of the converter), and cost.

As presented in this application note, resonant converters – LLC resonant converters in particular – have all of the features mentioned above, resulting in a compact and highly efficient design. Their ability to keep the output voltage regulated, over a very wide input voltage range, contributes to reducing the overall system cost.

The relatively simple architecture of these parts permits the implementation of control and supervision/management tasks with a small pin count dsPIC DSC from Microchip. Sophisticated control is possible, using the DSP capabilities of dsPIC DSC devices.

RESONANT CONVERTERS

Resonant converters are included in a wide range of converters. The strategy of using one is to design a highly efficient converter while eliminating a common disadvantage of traditional implementations based on Pulse-Width Modulation (PWM) – high switching losses. Many different solutions have been suggested, implemented, and tested in recent years, and many of them are now widely used in commercial products.

Resonant Converter Theory

The basic idea behind a resonant converter is to operate the MOSFETs with either a sinusoidal voltage or by running a sinusoidal current through it. The switching instant must be selected in proximity to the zero crossing of the sinusoidal voltage or current. The dissipated power will then be very small.

An approach that can be used in most converters is to design a “resonant-switch” converter. In this case, reactive elements (caps and inductors) are added around the switch in order to generate the mentioned sinusoidal voltage or current. Almost any topology can take advantage of this approach; however, the resulting network requires more components and the overall improvements do not match the increased complexity.

RESONANT TOPOLOGIES

There are three main classes of resonant converters:

- Series converter (the load is connected in series with the tank)
- Parallel converter (the load is connected in parallel to the tank)
- Series-parallel converter (the tank circuit is a combination of the series and parallel classes of converters)

From a high-level perspective, the architecture of any such converter can be described, as shown in Figure 1. According to the selected type, the resonant tank box will contain one of the circuits shown in Figure 2.

FIGURE 1: HIGH-LEVEL RESONANT CONVERTER BLOCK DIAGRAM

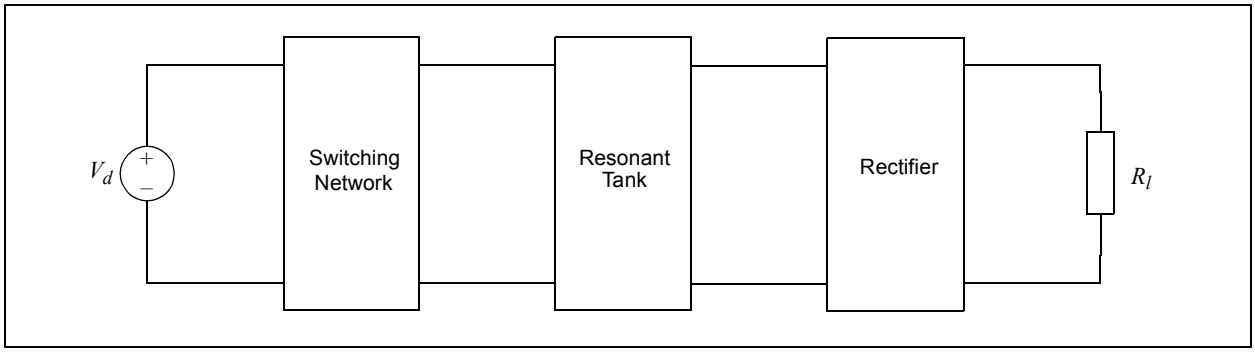
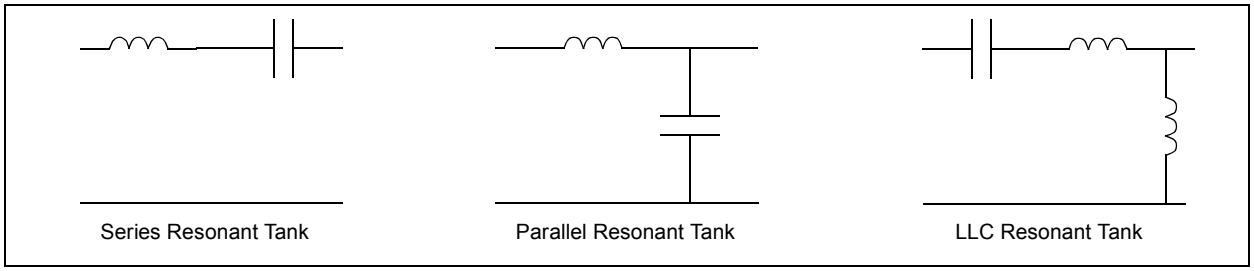


FIGURE 2: RESONANT TANK TYPES



MOSFET Losses

Before discussing the resonant converter categories in greater detail, the process that generates losses during MOSFET switching will be reviewed, using the simple circuit of Figure 3, where a half-bridge leg is represented. Each switching element is also represented with the anti-parallel diode, which could be an external diode or the component body diode. An input voltage (V_d) is applied and an output current (I_0) is considered. The lower MOSFET is initially closed and it is opened at time t_0. The MOSFET is closed again at time t_1. The idealized waveforms for both voltage and current are shown in Figure 4. Please note that the shaded areas consist of the power losses that are repeated at each PWM cycle, which is termed “hard-switching”.

FIGURE 3: HALF-BRIDGE CIRCUIT

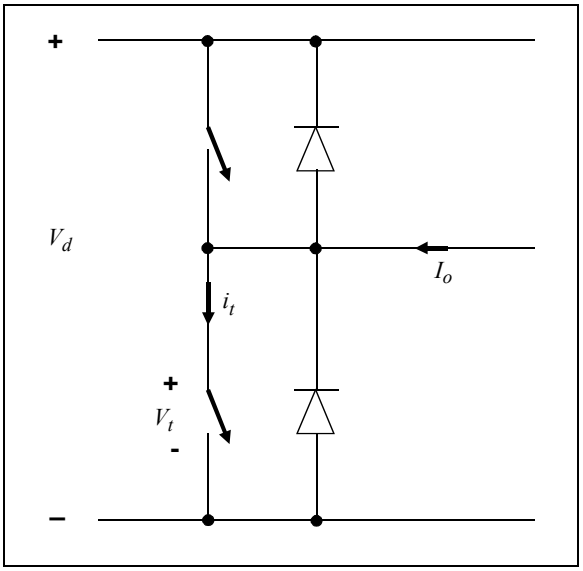
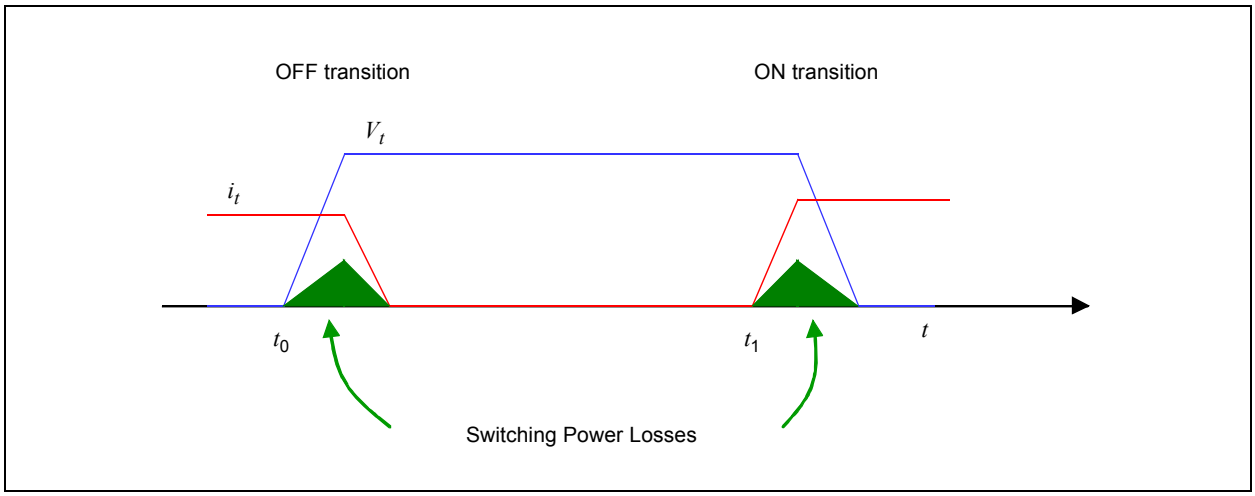


FIGURE 4: MOSFET SWITCHING LOSSES



An additional problem related to high voltages and current being switched in a short period of time is the (over)stress that MOSFETs have to withstand during commutation. Overvoltages and/or overcurrents can easily be a by-product of fast commutation.

Figure 5 shows the voltage and current trajectories for a MOSFET; the axes are the voltage on the MOSFET and the current flowing through it. During the turn-on transition, the voltage remains almost constant to its maximum value while the current is increasing; only at the very end does the voltage drop to zero. Similar and reversed behavior can be observed at the turn-off transition (see Figure 4). A first solution to this component overstressing has traditionally been the use of Snubbers, which are circuits made up of R, C, L and diodes. Snubbers work well for component stress, but since they usually are dissipative, they do not help in the attempt to preserve energy. Figure 6 shows the trajectories using Snubbers.

Ultimately, the best solution is to try to design a switch circuit, or operate the system in such a way that during the switching time, the MOSFET voltage and/or current is as close to zero as possible. This constraint would make the switching power losses (dissipated power) very small. Figure 7 shows the corresponding trajectories.

FIGURE 5: MOSFET TRANSITION TRAJECTORIES

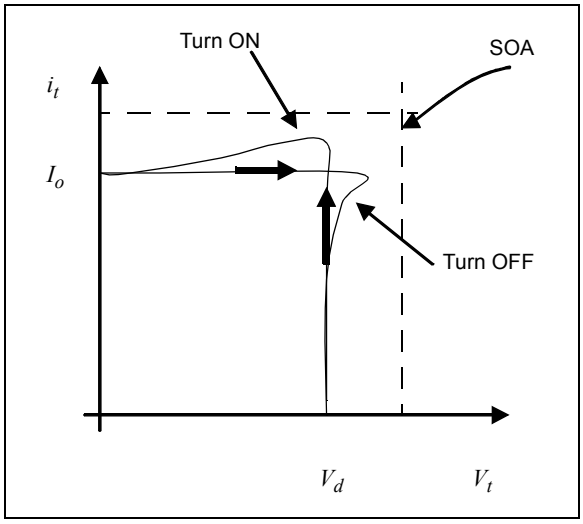


FIGURE 6: MOSFET TRANSITION TRAJECTORIES USING SNUBBERS

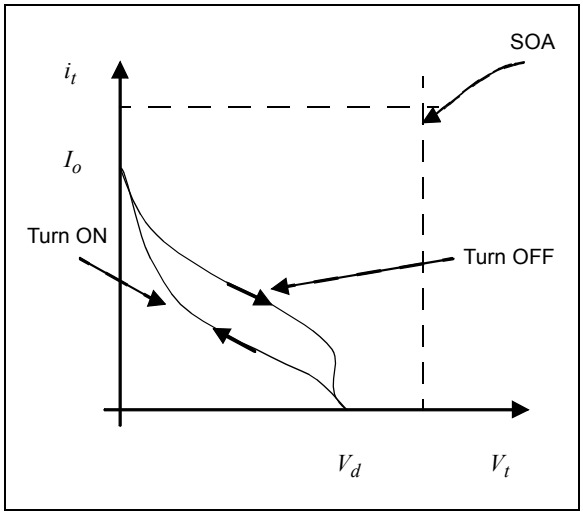
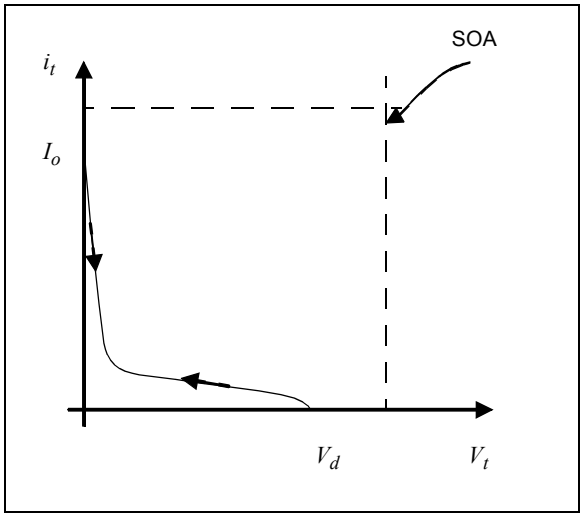


FIGURE 7: MOSFET TRANSITION TRAJECTORIES WITH SOFT-SWITCHING



LLC CONVERTERS

A more attractive approach (in terms of circuit simplicity and overall efficiency), is the design of “load-resonant” converters. A typical circuit consists of a half-bridge or full-bridge converter followed by a tank circuit to which the load can be connected (either in series or in parallel). The tank will force the voltage/current to be sinusoidal so that, again, it is possible to synchronize the switch operation to the zero crossing of the voltage or current. Switching losses are therefore “naturally” reduced.

A high-level description of how such converters work is as follows. The switching network, whose MOSFETs are driven by PWM signals, generates a square wave for the resonant tank circuit. However, because of the presence of the tank circuit, only fundamental sinusoidal waveforms can be supported by the circuit. The output rectifier, in one of its multiple possible topologies, is then used to rectify the sinusoidal waveform and get the desired DC output voltage. The resonant topology can then incorporate a transformer as the parallel inductance, permitting operation in a galvanically-isolated environment.

These converters are characterized by two operating frequencies:

1. the switching frequency, as imposed by the control electronics (the frequency at which the MOSFETs are operated)
2. the natural resonant frequency of the tank

   While the resonant frequency is fixed; as soon as the circuit components (capacitors, inductors and/or transformers) are selected, the switching frequency can be dynamically changed.

This is how the power transfer is managed and the output voltage is controlled, versus load and input voltage changes. The relationship between the switching and resonant frequency translates into a voltage gain, which is demonstrated in subsequent sections.

While the three resonant converters, discussed previously, share the same fundamental working methodology, there are some advantages and disadvantages in using each of them.

One of the main things to consider when comparing the topologies is how they behave during no load conditions. One key characteristic of these converters is that some current may be flowing in the converter even at no load; this is due to the resonant nature of the circuit. This current is normally called a “tank circulating current” and does not play an active role in the power transfer from the input to the output. Therefore, one design goal will be to keep it as small as possible. This current is also responsible for general low-efficiency at low load, since they do not, or at least only weakly, depend on output load currents.

There are some differences in the three resonant converter topologies: series, parallel, and series-parallel. The differences are apparent when the efficiencies and deficiencies are highlighted.

Series Resonant Converter

- The series resonant converter can sustain an output short circuit if the switching frequency is far away, either above or below the resonant frequency. This is because, at resonance, the circuit impedance is extremely low, which gives rise to a very high current, which can be so high that it could destroy the MOSFETS.
- One benefit is the ability of the series resonant converter to work at no load, since no current will be flowing in the resonant circuit, but it cannot regulate the output voltage.
- The efficiency of the series resonant converter is higher at partial load than at full load.

Parallel Resonant Converter

- The parallel resonant converter is self-protected against output short-circuit.
- The parallel resonant converter can be destroyed when operating in an open circuit, at a switching frequency that is close to the resonant frequency.
- The parallel resonant converter has a decreasing efficiency when the load resistance increases.

LLC CONVERTER APPLICATIONS

Applications in which the LLC converter is used can take advantage of these two main features:

1. very low switching losses (high efficiency)
2. the capability to control the output voltage at all load and line conditions

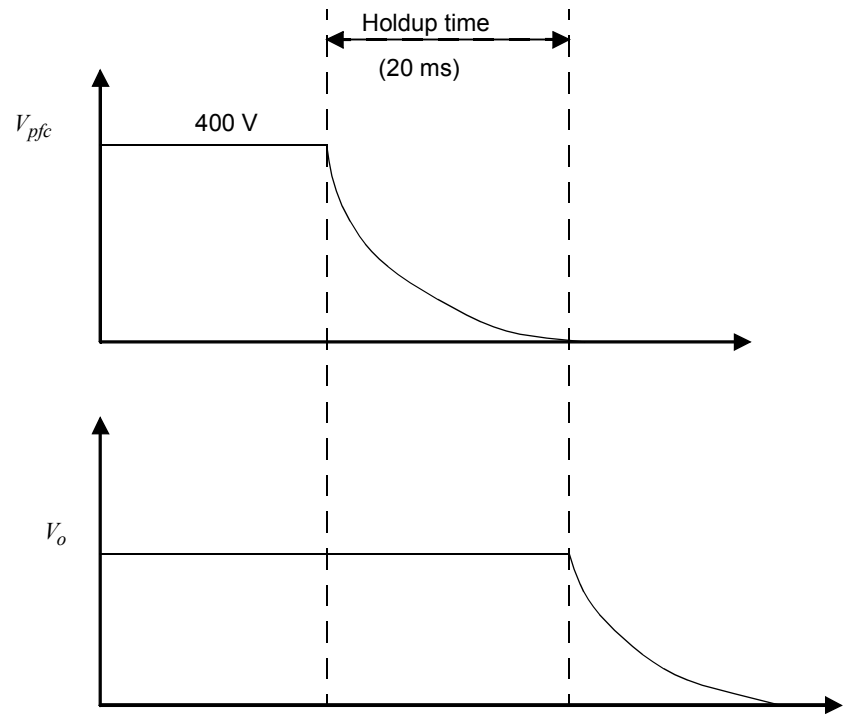
In telecom applications, the LLC converter is widely used as the DC/DC converter following a PFC in an AC-DC system. The typical PFC output voltage is approximately 400V, and can be directly fed into the LLC converter.

One typical requirement of such systems is to guarantee the output voltage with the rated power for a predetermined amount of time (called holdup time, typically 20 ms) after the AC voltage is removed. The reason for this is that the telecom equipment requires some time to perform housekeeping functions before shutting down.

A typical situation is shown in Figure 8, where V_{pfc}, the PFC output voltage, is fed into the LLC converter and its output (V_o) is powering the system equipment. In traditional systems, a big capacitor in the DC link is required to keep the voltage at the rated output during the holdup time. This directly impacts the system size and cost. The resonant converter with the ability of regulating the output voltage versus a very wide input voltage range (80-100V is a reasonable range) will allow the big bulk capacitor to be replaced with a smaller one.

Another typical application of such converters is where small size and reduced height are a premium. Here the main requirements are to have small units with a very high efficiency, which again allows for removal of fans and a reduction or omission of heat sinks, thereby enabling the unit to fit into small space constraints. For example, flat panel televisions.

FIGURE 8: PFC OUTPUT VOLTAGE AND REQUESTED OUTPUT VOLTAGE FROM DC/DC CONVERTER



Note: The system must keep the nominal output voltage for at least the hold-time.

LLC REFERENCE DESIGN

Figure 9 shows a high-level block diagram of Microchip's LLC Resonant Converter Reference Design. The design specifications are summarized in Table 1.

The switching circuit is implemented with a half-bridge topology, so that the output voltage will swing between 0V and V_d = 400 V_{dc} nominal. A full-bridge circuit would also have been possible, but the half-bridge has been selected for its simplicity and reduced number of components.

The resonant tank circuit is made up of a capacitor, an inductor, and the isolating transformer. The second "missing" inductor is implemented via the transformer magnetizing inductance. Note that sometimes even the first inductor may be "lumped" into the transformer. This configuration would reduce converter size, cost, and complexity. At the secondary side, a synchronous rectifier has been implemented to improve the overall system efficiency.

The selection of a switching frequency of 200 kHz is primarily dictated by the requirement of using small passive components (including the transformer). The control loop implementation, although sophisticated, still leaves enough bandwidth to the dsPIC DSC to perform auxiliary tasks like fault monitoring, temperature monitoring, and communication.

The system is completely digital. The loop (voltage loop) is closed through the implementation of a PID within the dsPIC DSC, which completely takes care of all the system operations (including fault and temperature monitoring).

The system requires two low voltage supplies: +12 V for the MOSFET drivers and a 3.3V for the dsPIC DSC and analog components. The auxiliary power supply circuit is used at start-up (and when normal operation is restored after faults), deriving a 12V output from the high-voltage input rail. A high-efficiency buck converter is then used to derive from 12V the 3.3V required to power the controller. During normal operation, when the primary LLC converter is running, the 12V supply for the drivers is directly derived from the converter output voltage, which is also the input to the buck converter. The auxiliary power supply circuit can be switched ON and OFF. A series diode is used to decouple the two 12V supplies. Since one of the main design targets is high efficiency, specific care has been used in the implementation of the auxiliary power supply circuit to make its power consumption as low as possible.

FIGURE 9: REFERENCE DESIGN HIGH-LEVEL BLOCK DIAGRAM

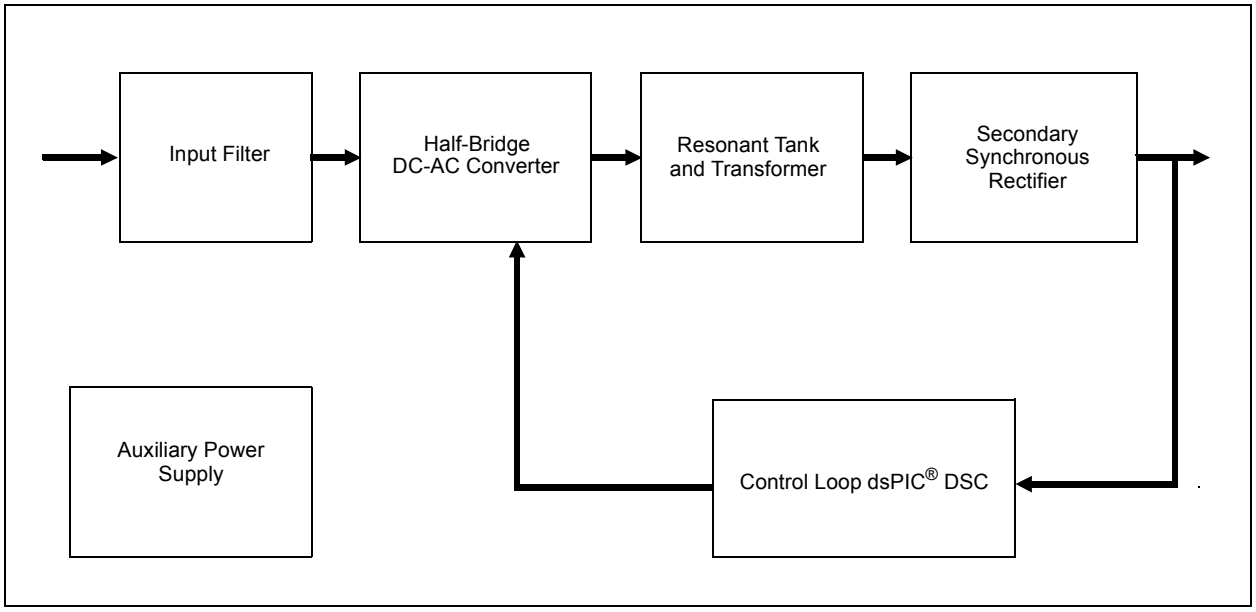


Table 1 provides the reference design specifications.

TABLE 1: MICROCHIP REFERENCE DESIGN SPECIFICATIONS

Spec	Value
Input Voltage Range	350 V_{dc} – 420 V_{dc} 400 $V_{dc,nom}$
Output Voltage	12 V_{dc}
Power Rating	200W
Nominal Resonant Frequency	210 kHz
Nominal Switching Frequency	205 kHz
Efficiency	95% (target)

Table 2 lists the dsPIC resources used in the design.

TABLE 2: dsPIC RESOURCE USED (dsPIC33FJ16GS502)

Resource	Value
Program Memory	3.5 Kb
Data Memory	650 bytes
PWM	2 channels
ADC	4 channels
Comparators	1 channel

LLC CIRCUIT ANALYSIS AND MODEL

Figure 10 shows the basic LLC model that will be used to derive the equations describing the system behavior. Starting from the left side of the drawing, the following stages can be observed:

1. DC Input

   The voltage generator represents the input voltage, which normally is approximately 400 V_{dc}.

2. Switch Circuit

   The switch network has been implemented as a half-bridge; note that the body (or external) anti-parallel diodes and the parasitic output capacitances of the MOSFETs are explicitly shown, since they play an important role in the circuit operation and performance and cannot be neglected.

3. Resonant Tank

   This circuit is made of three components: a resonating capacitance (C_r), a resonating inductance (L_r) and the transformer magnetizing inductance (L_m). C_r, L_r, L_m are the three components that characterize the LLC converter. Note that in this topology the magnetizing inductance plays an active role and is in fact a design parameter. The presence of these reactive components generate two resonating frequencies in the network, as will be explained later.

4. Ideal Transformer

   Since the magnetizing inductance is clearly shown, we can replace the transformer with its ideal model. Note that this is not completely correct, since we should also show the primary and secondary leakage inductances. While this is true and these inductance play an important role in the transformer specs definition, they are currently not fundamental to determine the overall system behavior and are therefore removed from the model.

5. Rectifier

   In the drawing a diode-based, full-wave rectifier is shown. A number of different topologies can be used: single diode rectifier, full wave, bridge rectifier or even synchronous rectifier. The latter is the solution used in the reference design. However, at this point we are not interested in the implementation details, so a full-wave rectifier is more than adequate for computations.

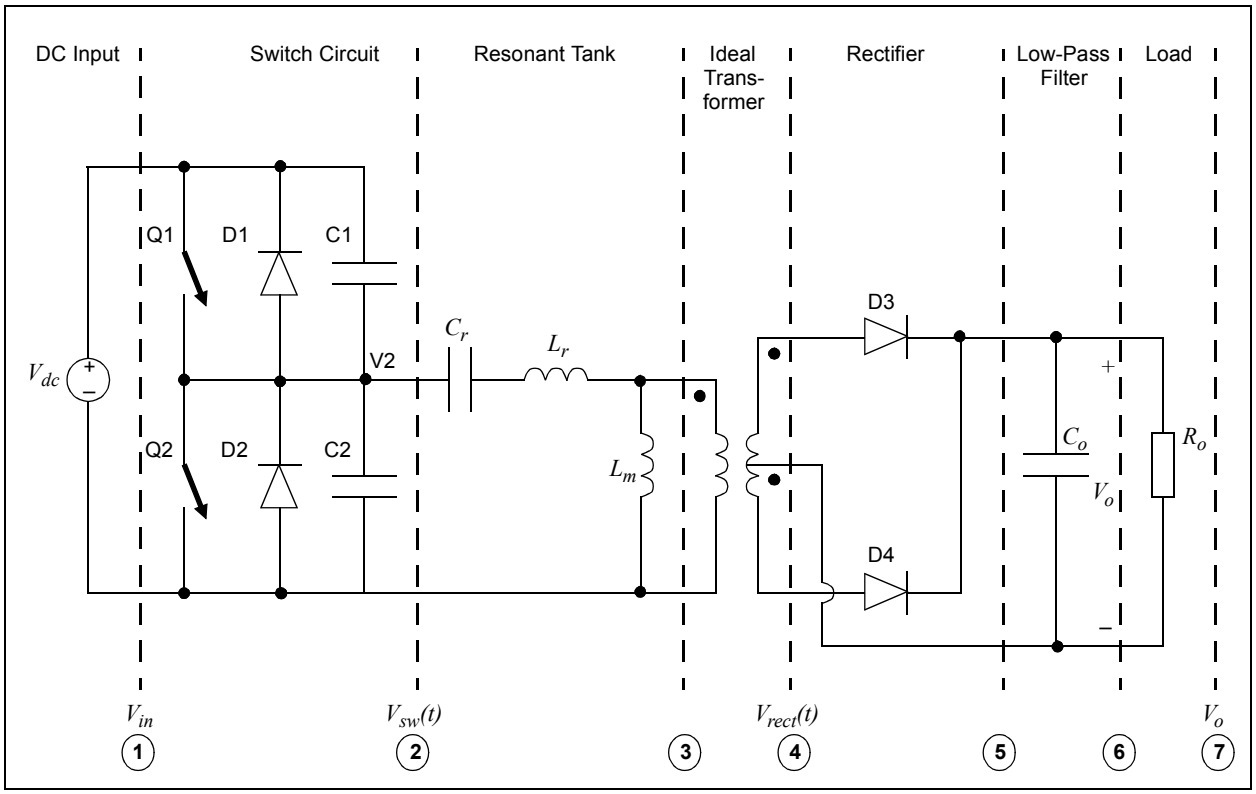
6. Low-Pass Filter

   This filter is implemented with a single capacitor (C_o).

7. Load

   The resistor R_o represents the output load.

FIGURE 10: LLC CIRCUIT COMPONENTS AND SECTIONS



Looking at the different stages in the circuit, it is clear that at interface 1 a DC voltage is present, at interface 2 a (nominally) square waveform, at interface 3 a sinusoidal waveform, and finally at interface 6 a rectified sinusoidal waveform, which will give a DC voltage. The circuit operation is quite complex and it is not possible to directly obtain the system transfer function using classical linear system analytical methods. The approach taken is to pay attention to the tank circuit. The transfer function of a tank circuit is bell shaped around the resonant frequency. As a consequence, only a sinusoidal signal at that frequency will be transferred, while all other frequencies (harmonics) will be attenuated.

The system was designed and the tank components were selected so that, nominally, the switching frequency of the MOSFETs equals the tank resonant frequency. Therefore, if the tank circuit is "good", it will only allow sinusoidal waveforms to be "transferred" to the output.

The two MOSFETS, Q1 and Q2, operate in Complimentary mode, with a fixed dead-time (to avoid shoot-through) with a (nominally fixed) 50% duty cycle. Voltage V2 will then equal V_{dc} when MOSFET Q1 is closed, and equals 0V when Q2 is closed. Therefore, the output of the switch circuit ($v_{sw}(t)$) is a square wave (50% ON time), in the range 0-V_{dc}V.

In the following paragraphs, a system model equation set will be developed, allowing an easy relationship between input and output voltages to be derived. As such, the development is based on the consideration that only the voltage and currents at the fundamental frequency should be taken into consideration due to the presence of the tank circuit.

In the computations that follow, some basic mathematics results are used. Essentially, the Fourier series is widely used to analytically describe square waves. The reason for this is that it allows the analytical form of any periodic signal to be written as the sum of an infinite number of sine and/or cosine waveforms, whose frequencies equal the fundamental (frequency of the square wave) and its harmonics (integer multiples).

We are only interested in square wave signals since this is what we get from the input switching circuit. Equation 1 shows the Fourier series of a square waveform of amplitude A.

EQUATION 1:

$$s(t) = \frac{A}{2} + \frac{2}{\pi} A \sum_{k=1,3,5,\ldots} \frac{1}{k} \sin(2\pi k f t)$$

Switch Network Model

Considering the conventions used in Figure 10, the voltage at the output of the switch circuit is a square wave, which is express by Equation 2.

EQUATION 2:

$$v_{sw}(t) = \frac{V_{dc}}{2} + \frac{2}{\pi} V_{dc} \sum_{k=1,3,5,\ldots} \frac{1}{k} \sin(2\pi k f_{sw} t)$$

where,
f_{sw} is the switching frequency of the MOSFETs

This voltage is the sum of a DC level (V_{dc}/2), which is blocked by the tank capacitor (C_r), and an infinite number of sinusoidal waves, whose fundamental is computed from Equation 2, with k = 1, as shown in Equation 3.

EQUATION 3:

$$v_{sw,1}(t) = \frac{2V_{dc}}{\pi} \sin(2\pi f_{sw} t)$$

The peak, average and *rms* values of this sinusoidal voltage are shown in Equation 4.

EQUATION 4:

$$V_{sw,1,pk} = \frac{2V_{dc}}{\pi}$$

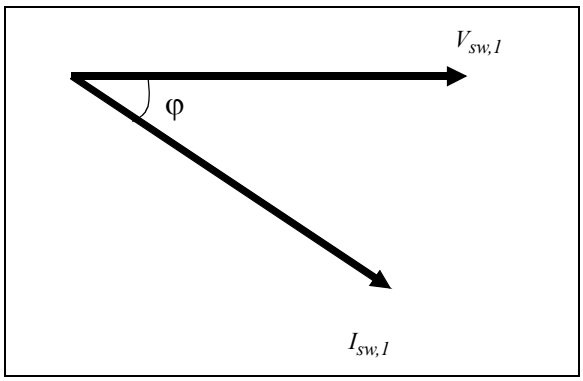
$$V_{sw,1,ave} = 0$$

$$V_{sw,1,rms} = \frac{\sqrt{2}V_{dc}}{\pi}$$

where,
sw = voltage at the output of the switching circuit
1 = consideration of the fundamental term only
pk = peak square value
ave = average square value
rms = root mean square value

As mentioned earlier, the resonant tank, if correctly tuned to the switching frequency, will present a finite impedance to the fundamental frequency and an infinite (in reality, very large) impedance to all other harmonics. The result is that the tank circuit will experience a sinusoidal current. Because of the reactive elements, there will be a phase shift between voltage and current as shown in Figure 11.

FIGURE 11: TANK CIRCUIT CURRENT LAGGING VOLTAGE



Therefore, the resonant tank current can be expressed by Equation 5.

EQUATION 5:

$$i_{t,1} = I_{t,1,pk} \sin(2\pi f_{sw} t - \varphi)$$

where,
t = resonant tank
1 = fundamental value
pk = peak value
φ = phase delay between voltage and current

The DC current drawn from the input voltage generator, when MOSFET Q1 is closed, can be computed as the average value, over one period, of the tank current. The results are shown in Equation 6.

EQUATION 6:

$$I_{dc} = \frac{1}{\pi} I_{t,1,pk} \cos\varphi = \frac{\sqrt{2}}{\pi} I_{t,1,rms} \cos\varphi$$

Equation 3, Equation 5 and Equation 6 allow us to replace the "real" input circuit with the model of Figure 12. The circuit at the left represents the input: the voltage is imposed from the generator (V_{dc}); the current drawn from the source is, as seen, the average (DC) value of the tank current.

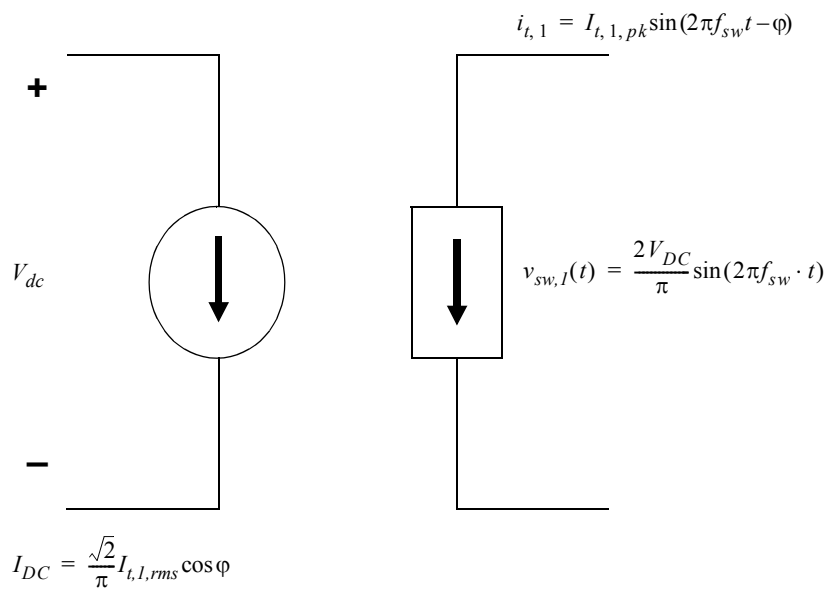
The section on the right represents the equivalent circuit that drives the resonant tank, where only sinusoidal signals at the fundamental frequency are of interest.

We can now also determine the average input power, as shown in Equation 7:

EQUATION 7:

$$P_{dc,ave} = \frac{\sqrt{2}}{2\pi} V_{dc} I_{t,1,rms} \cos\varphi$$

FIGURE 12: INPUT SWITCHING CIRCUIT MODEL



Resonant Tank

The real transformer is replaced by its model, where the magnetizing inductance (L_m) is clearly expressed. Leakage inductance at the primary and secondary are instead neglected (non-essential to this discussion). In the hypothesis previously explained of focusing only on sinusoidal waveforms at the fundamental frequency, it is possible to find the transfer function ($H(s)$) of the resonant tank circuit in Figure 13, where the output circuit has been replaced by an equivalent resistor (R_e), whose value will be computed in the following section.

Considering Figure 14, the input impedance, $Z_{in}(s)$, can be computed, as shown in Equation 8.

EQUATION 8:

$$Z_{in}(s) = Z_s(s) + Z_p(s)$$

The circuit transfer function can be easily computed if we realize that the circuit components can be lumped into a series impedance (Z_s: C_r and L_r) and a parallel impedance (Z_p: L_m, transformer, output load). These detailed computations are shown in Equation 9 through Equation 11.

Respectively, $Z_s(s)$ and $Z_p(s)$ are the impedances of the series and parallel branches, which are expanded in Equation 9 and Equation 10, which results in the calculation shown in Equation 11.

EQUATION 9:

$$Z_s(s) = \frac{1}{sC_r} + sL_r$$

EQUATION 10:

$$Z_p(s) = n^2 R_e \parallel sL_m$$

EQUATION 11:

$$Z_{in}(s) = Z_s(s) + Z_p(s) = \frac{1}{sC_r} + sL_r + (n^2 R_e) \parallel sL_m$$

where, n^2 is the transformer turns ratio, as shown in Figure 15.

FIGURE 13: RESONANT TANK CIRCUIT AND ITS TRANSFER FUNCTION

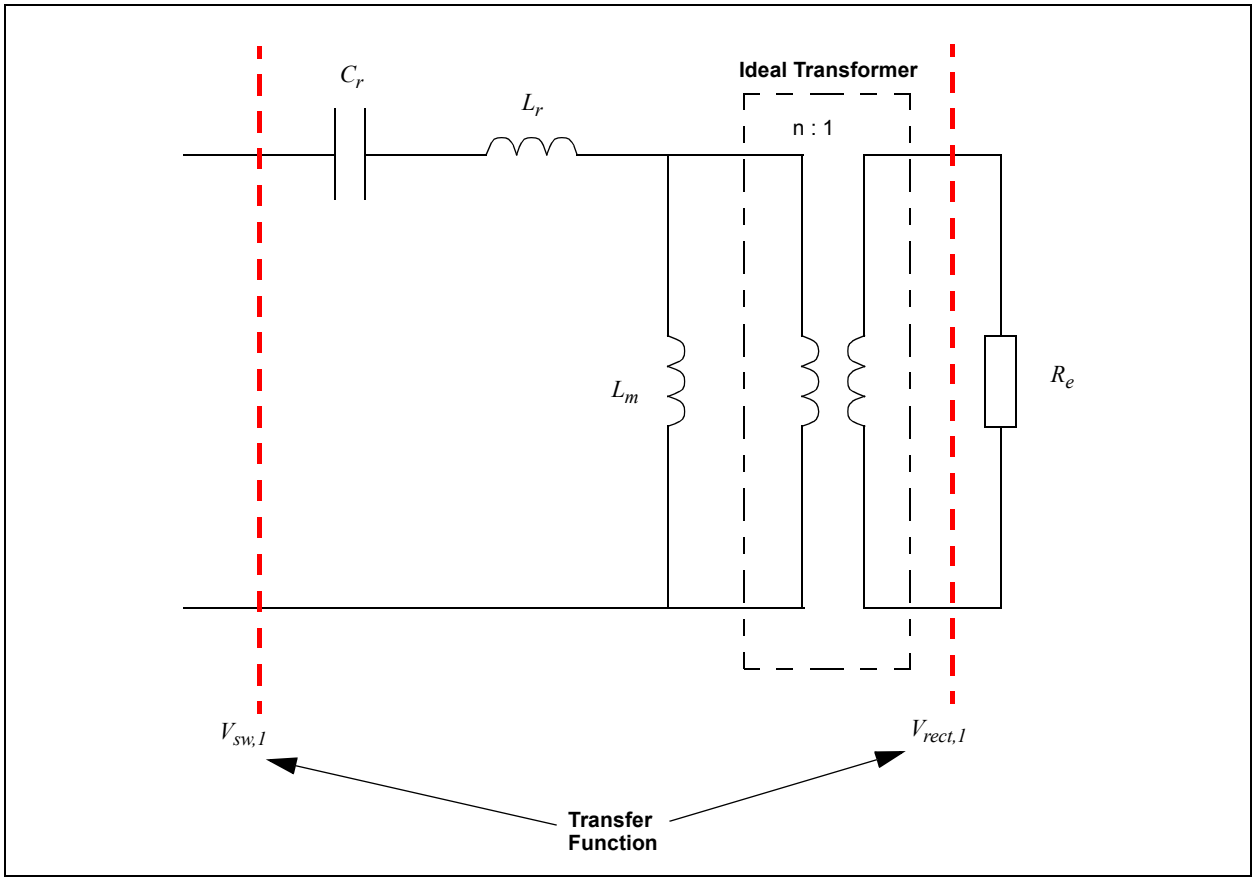


FIGURE 14: RESONANT TANK WITH INPUT IMPEDANCE COMPUTATION

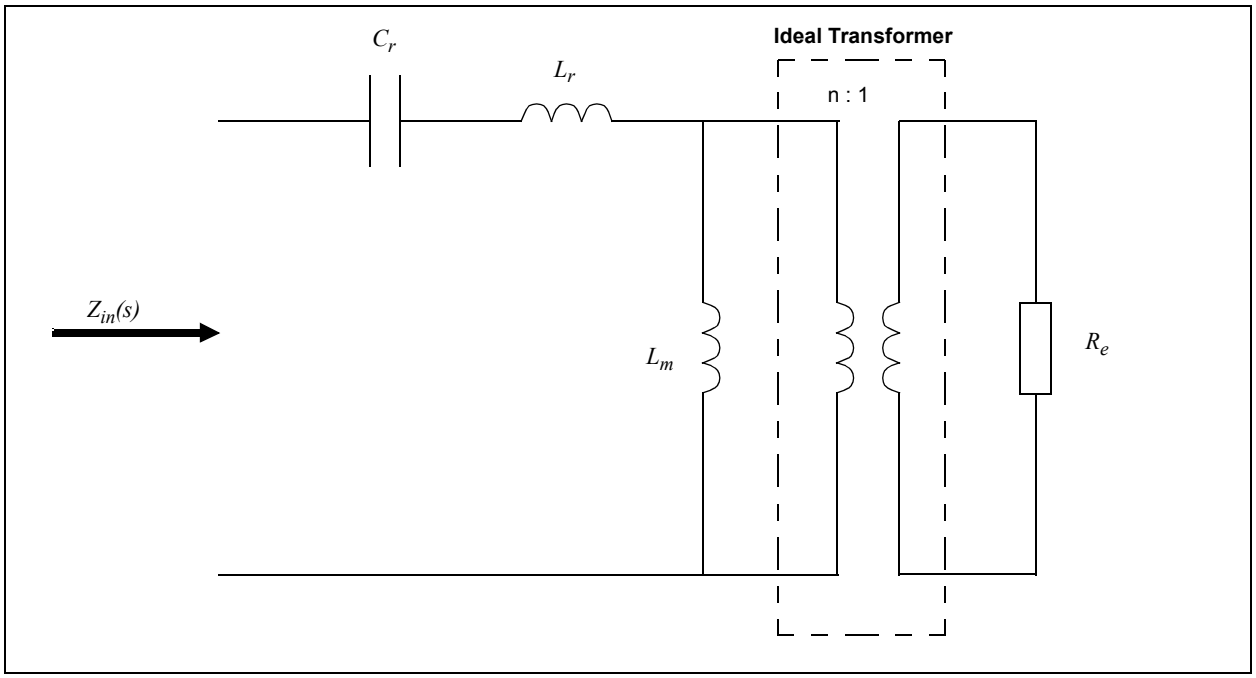
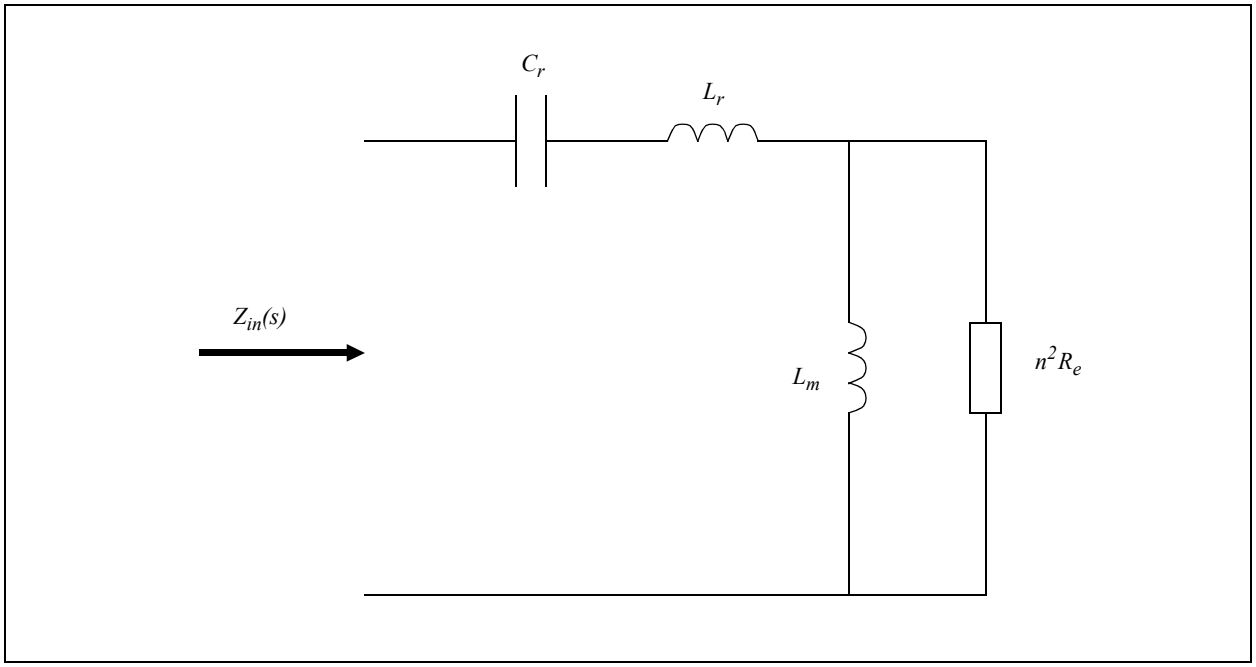
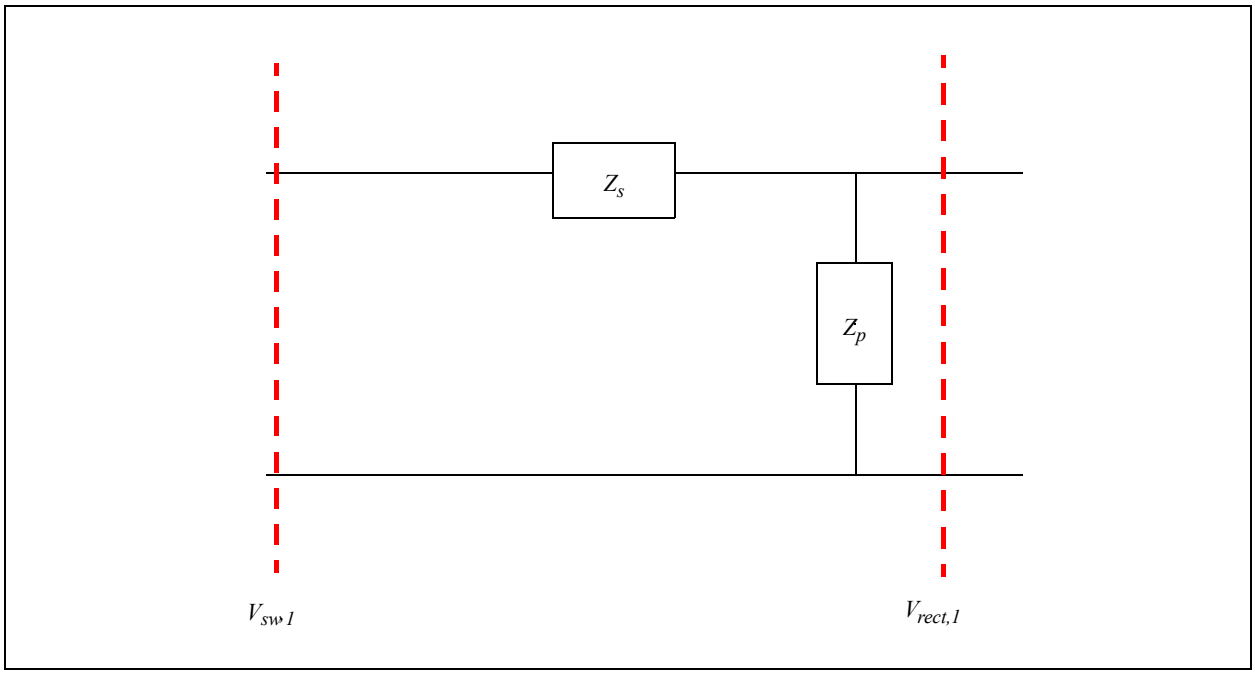


FIGURE 15: RESONANT TANK CIRCUIT AND ITS EQUIVALENT CIRCUIT



The circuit of Figure 13 can now be redrawn as in Figure 16.

FIGURE 16: RESONANT TANK CIRCUIT USED TO COMPUTE THE TRANSFER FUNCTION



Since, in the tank circuit, only the fundamental sinusoidal waveform is of relevant amplitude (all others are attenuated by the tank transfer function), it is possible to define the transfer function at the fundamental frequency, as shown in Equation 12.

EQUATION 12:

$$H(s) = \frac{V_{rect,1,rms}}{V_{sw,1,rms}} = \frac{Z_p}{Z_s + Z_p} = \frac{1}{n}\frac{(n^2 R_e) \| sL_m}{Z_{in}}$$

where,

$V_{rect,1,rms}$ = the rms value of the transformer secondary side voltage.

$V_{sw1,rms}$ = the rms value of the voltage at the input of the tank.

In both cases, the subscript “1” refers to the fact that only the fundamental frequency component is considered. The factor (1/n) is due to the secondary over primary voltage ratio, which is expressed in Equation 13.

EQUATION 13:

$$v_{secondary} = \frac{1}{n} v_{primary}$$

Rectifier Model

Once again, at the transformer secondary, because of the tank circuit, we will have a sinusoidal current ($i_{rect}(t)$) flowing through the transformer itself. Such current will flow alternatively in the two diodes D3 and D4 according to its sign, as shown in Figure 17 and Figure 18.

When examining the circuit, it is clear that this current is responsible for the voltage values at the transformer secondary. In fact, from Figure 17 and Figure 18, the following can be observed:

If current is positive, D3 is conducting and $v_{rect}(t) = V_o$

If current is negative, D4 is conducting and $v_{rect}(t) = -V_o$

FIGURE 17: SECONDARY CIRCUIT WHEN $i_r(t) > 0$

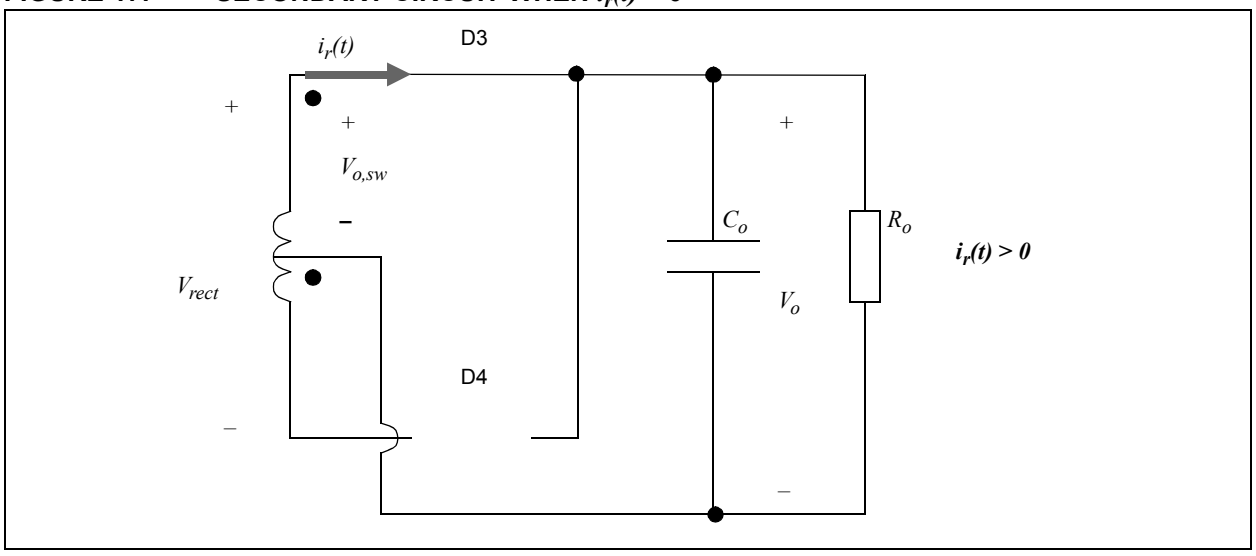
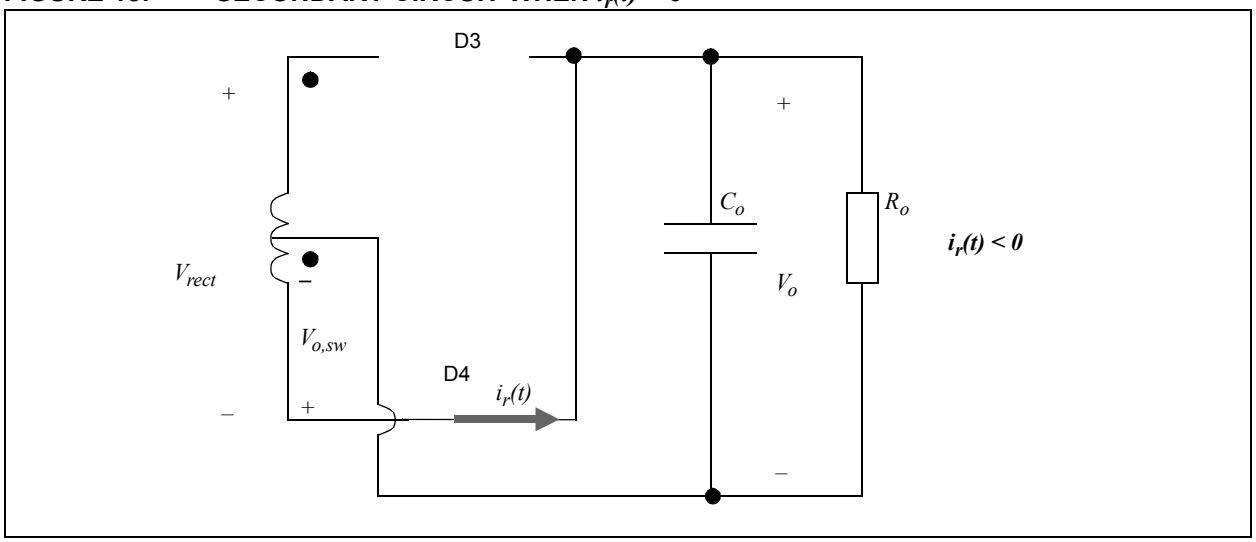


FIGURE 18: SECONDARY CIRCUIT WHEN $i_r(t) < 0$



Considering the Fourier series of this square wave, centered around 0V, its analytical equation can be written (at the rectifier input), as shown in Equation 14.

EQUATION 14:

$$v_{rect}(t) = \frac{4}{\pi} V_o \sum_{k=1,3,5,..} \frac{1}{k} \sin(2\pi k f_{sw} t - \psi)$$

Where,
ψ is the phase lag relative to the input voltage, ($v_{sw}(t)$).

The fundamental component is shown in Equation 15.

EQUATION 15:

$$v_{rect,1}(t) = \frac{4}{\pi} V_o \sin(2\pi f_{sw} t - \psi)$$

The average and *rms* values of this voltage are shown in Equation 16.

EQUATION 16:

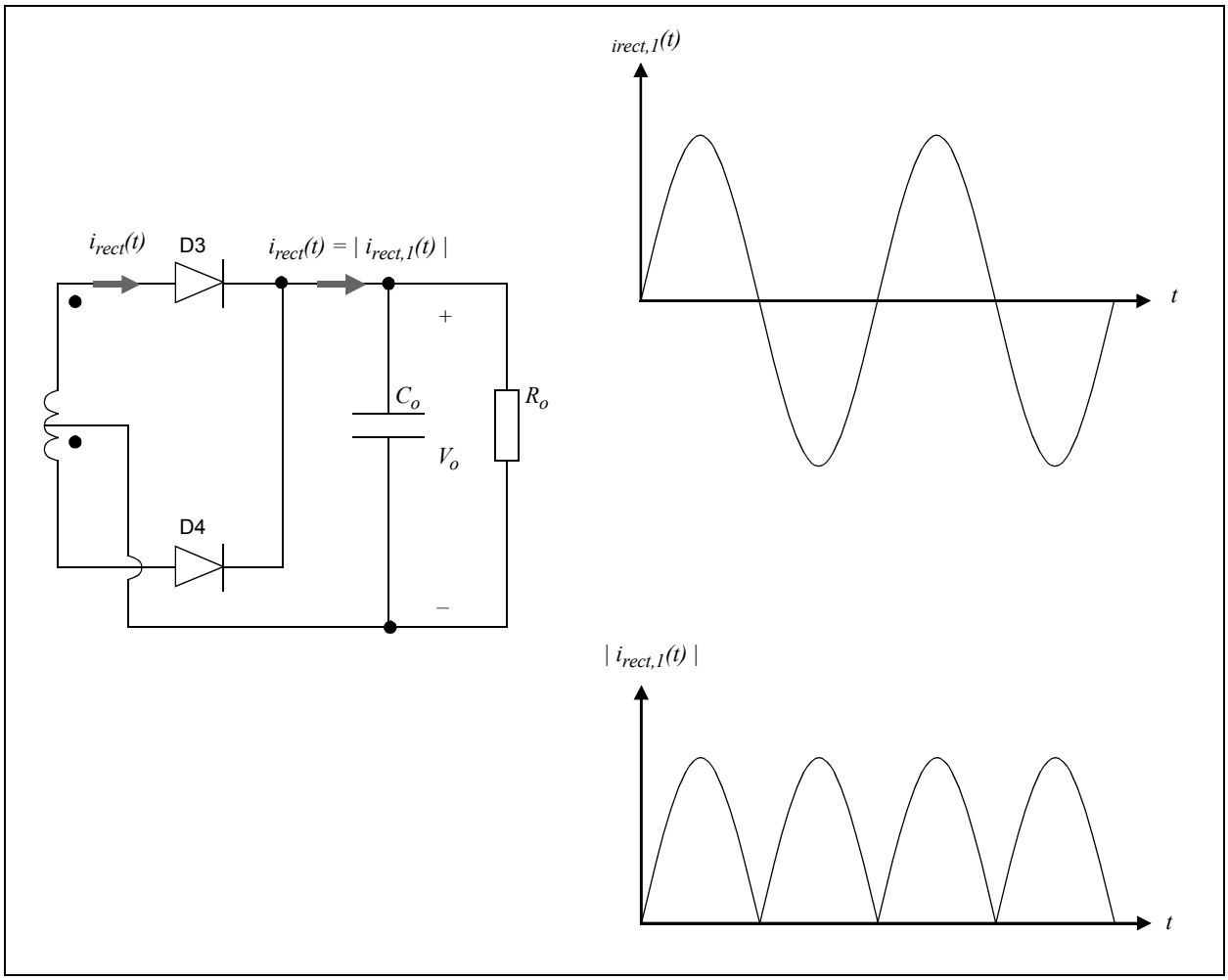
$$V_{rect,1,pk} = \frac{4V_o}{\pi}$$

$$V_{rect,1,ave} = 0$$

$$V_{rect,1,rms} = \frac{2\sqrt{2}}{\pi} V_o$$

As shown in Figure 19, the sinusoidal current $i_{rect,1}(t)$ at the transformer output is rectified by the diodes, so that its value after the diodes is that of equation17.

FIGURE 19: CURRENT AT THE RECTIFIER INPUT



EQUATION 17:

$$i_{rect,1,out}(t) = \left| i_{rect,1}(t) \right|$$

The rectifier input current can be expressed as shown in Equation 18 (only the fundamental frequency).

EQUATION 18:

$$i_{rect,1}(t) = I_{rect,1,pk} \sin(2\pi f_{sw} t - \psi)$$

While the rectifier output current is shown in Equation 19, the average value of such current is shown in Equation 20.

EQUATION 19:

$$i_{rect,1,out} = I_{rect,1,pk} \left| \sin(2\pi f_{sw} t - \psi) \right|$$

EQUATION 20:

$$I_{rect,1,out,ave} = I_o = \frac{2}{\pi} I_{rect,1,pk}$$

where,

I_o is the average (DC) current flowing into the load (resistor R_o, as shown in Figure 20)

Summarizing: at the secondary, a square voltage, whose fundamental term is in Equation 15, and a sinusoidal current (Equation 18 through Equation 20) are present. The important point here is that these two signals are in phase to each other, meaning they have the same relationship between voltage and current in a resistor. Based on this, it is possible to replace the rectifier operation with a resistor of proper value.

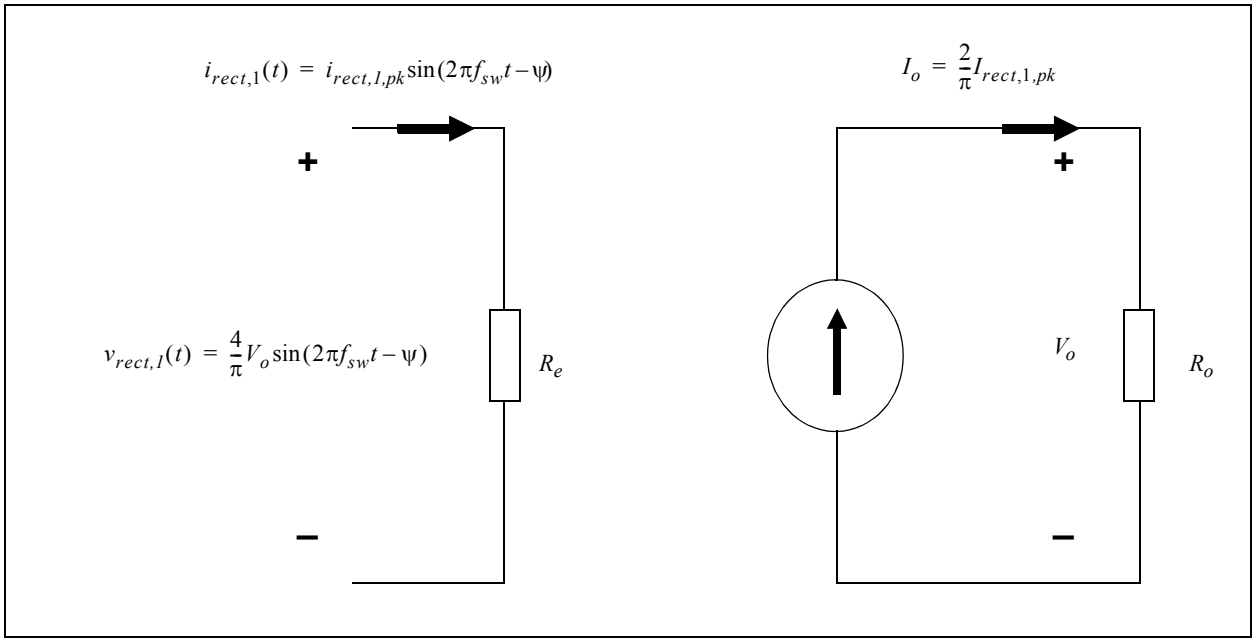
The equivalent resistor value can be computed from Equation 16 and Equation 20 solved against $I_{rect,1,pk}$, as shown in Equation 21.

EQUATION 21:

$$R_e = \frac{v_{rect,1}(t)}{i_{rect,1}(t)} = \frac{4V_o}{\pi}\frac{2}{\pi I_o} = \frac{8}{\pi^2}R_o$$

The rectifier model is shown in Figure 20.

FIGURE 20: RECTIFIER MODEL



Converter Model

At this point, all sections of the converter model of Figure 10 have been identified and their transfer function computed so that it is possible to determine the overall converter transfer function.

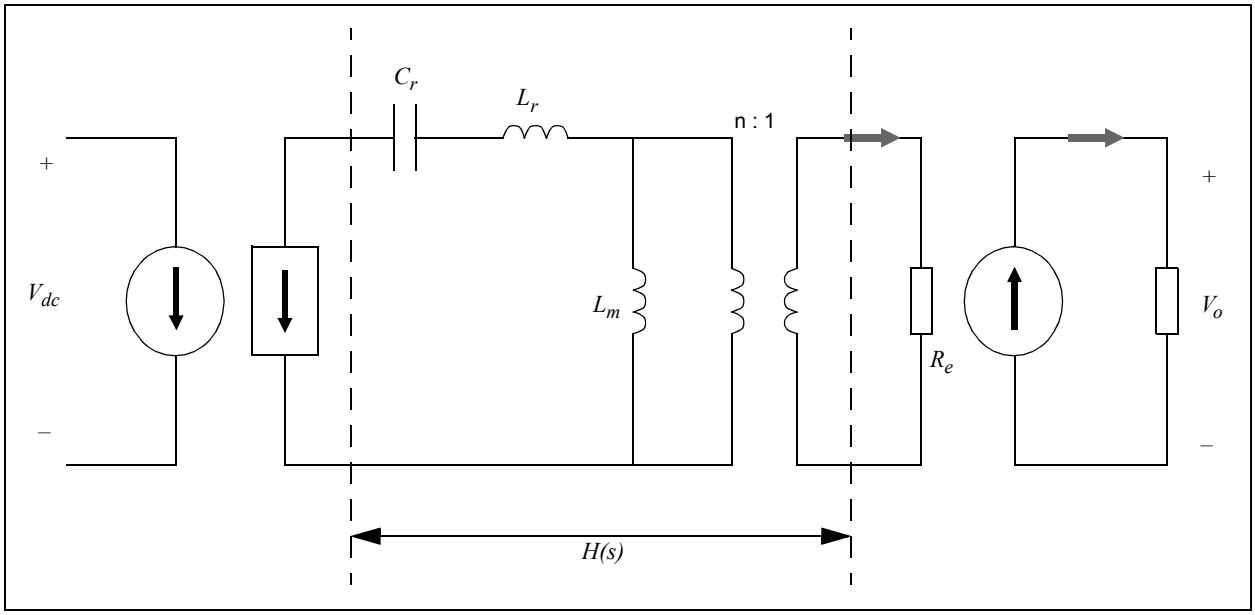
The overall model, obtained by joining together the block diagrams of Figure 12, Figure 13, Figure 14, Figure 15 and Figure 20, is illustrated in Figure 21. Since the circuit elements have been defined considering only fundamental frequency signals are of importance, the model is normally referred to as First Harmonic Approximation (FHA).

The overall I/O relationship, that is the output-to-input voltage ratio (these two voltages are DC values), can be determined by Equation 22 and referring to Figure 21.

Equation 23 introduces the definition of the “voltage conversion ratio”. The results are shown in Equation 24.

As we will analyze in the section **“Voltage Conversion Ratio”**, $M(f_{sw})$ depends on a number of different parameters.

FIGURE 21: OVERALL LLC CONVERTER MODEL



The overall I/O relationship, that is the output-to-input voltage ratio (these two voltages are DC values), can be determined by Equation 22 and referring to Figure 21.

Equation 23 introduces the definition of the “voltage conversion ratio”. The results are shown in Equation 24.

As we will analyze in the section **“Voltage Conversion Ratio”**, $M(f_{sw})$ depends on a number of different parameters.

EQUATION 22:

$$\frac{V_o}{V_{dc}} = \frac{V_o}{V_{rect,1,rms}} \frac{V_{rect,1,rms}}{V_{sw,1,rms}} \frac{V_{sw,1,rms}}{V_{dc}} = \frac{V_o}{\frac{2\sqrt{2}V_o}{\pi}} H(s) \frac{\frac{\sqrt{2}V_{dc}}{\pi}}{V_{dc}} = \frac{1}{2} H(s)$$

EQUATION 23:

$$M(f_{sw}) = n\left|H(s)\right|$$

EQUATION 24:

$$\frac{V_o}{V_{dc}} = \frac{M(f_{sw})}{2n}$$

VOLTAGE CONVERSION RATIO

Before proceeding, a few relationships that will be used going forward must be defined. The LLC circuit has two resonant frequencies, one (f_r) due to the presence of L_r and C_r (see Equation 25) and the second one (see Equation 26) due to the additional presence of L_m. However, when speaking of resonant frequency, f_r will always be referred to from this point forward.

EQUATION 25:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$$

The second resonant frequency is shown in Equation 26.

EQUATION 26:

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}$$

It is useful to define a normalized frequency that is the ratio of the current frequency (f) over the resonance frequency (f_r), which is shown in Equation 27.

EQUATION 27:

$$f_n = \frac{f}{f_r}$$

Going forward, all frequency values are considered to be normalized frequencies.

In addition, it is convenient to define the following: Inductance ratio (see Equation 28), characteristic impedance (see Equation 29), and the quality factor (see Equation 30).

EQUATION 28:

$$\lambda = \frac{L_r}{L_m}$$

EQUATION 29:

$$Z_o = \sqrt{\frac{L_r}{C_r}} = \frac{1}{2\pi f_r C_r}$$

EQUATION 30:

$$Q = \frac{Z_o}{R_e} = \frac{\pi^2 Z_o I_{out}}{8 n^2 V_{out}}$$

Using Equation 12 and Equation 23 it is possible to compute the analytical expression of the voltage transfer ratio. The results are shown in Equation 31.

EQUATION 31:

$$M(f_{sw}) = f(f_n, \lambda, Q)$$

In other words, the transfer ratio is a complex function of the normalized frequency and the tank component values. Also, it is not possible to draw the $M(f_{sw})$ function for the specific design until all of the parameters have been computed. However, it is possible to consider the families of M curves that are generated when considering as single parameters λ and Q.

Figure 22 represents one such curve. In this plot, the f_r resonant frequency is clearly shown. The other resonant frequency (f_{r2}) is responsible for the high peak that is present at the left side (low frequencies). Figure 23 plots the family of curves obtained with Q = 0.2 (fixed) and varying λ from 0.1 to 0.9 in 0.1 steps. Figure 24 plots the curves for a fixed value of λ = 0.2 and varying the quality factor Q from 0.1 to 0.9; again, in steps of 0.1.

FIGURE 22: VOLTAGE CONVERSION RATIO *M(f)*

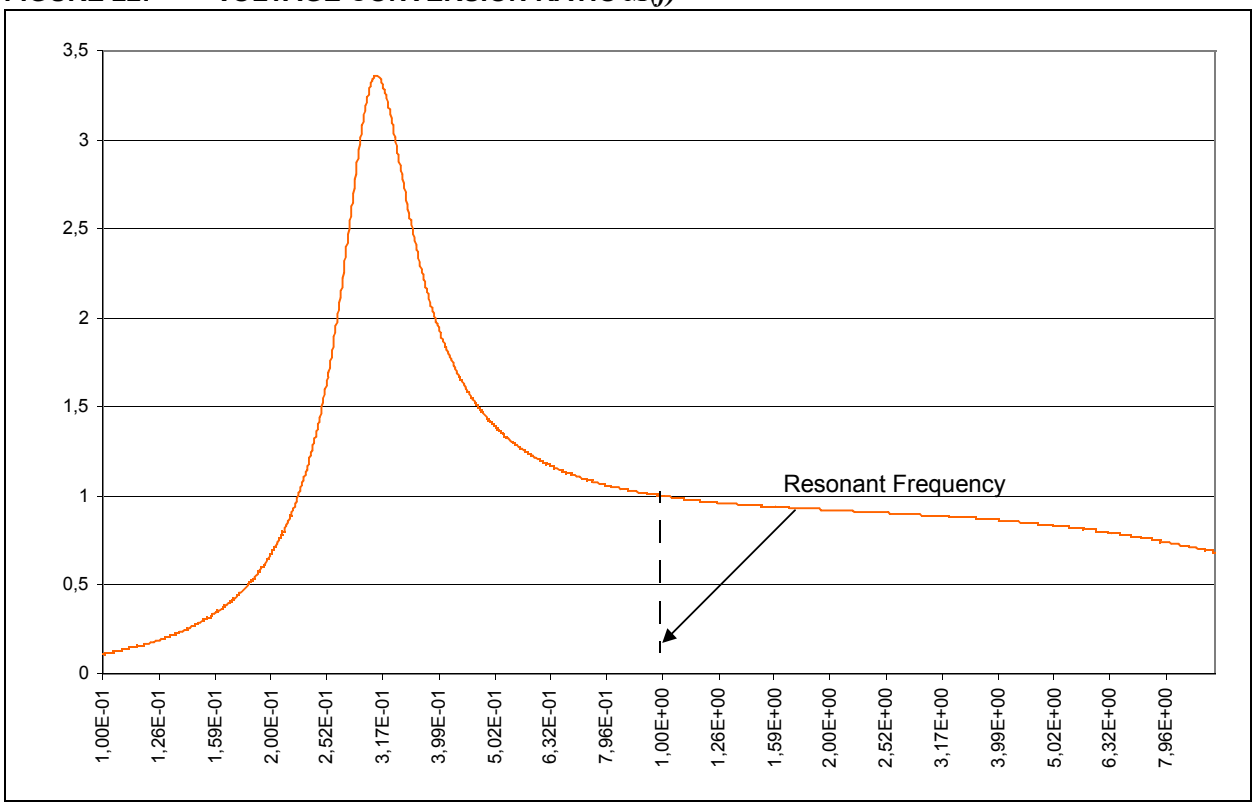


FIGURE 23: VOLTAGE CONVERSION RATIO *M(f)* WITH λ AS A PARAMETER

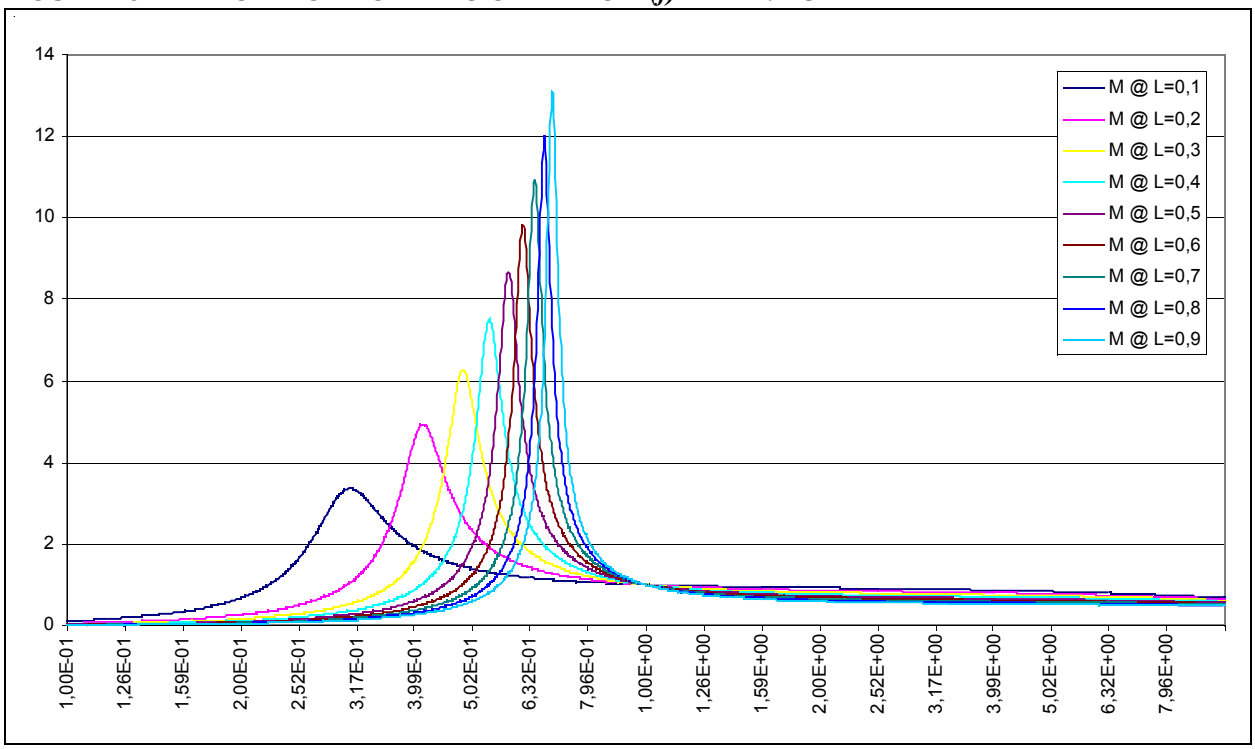
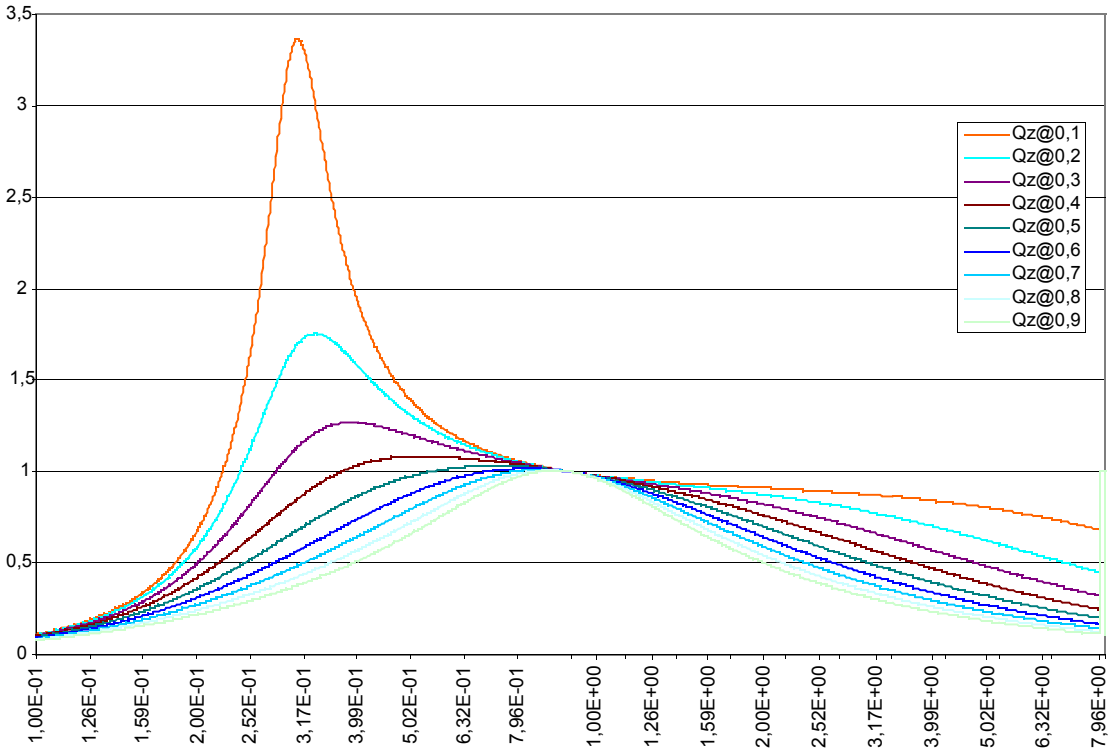


FIGURE 24: VOLTAGE CONVERSION RATIO *M(f)* WITH Q AS A PARAMETER



A couple of comments on these plots. It appears that as λ increases, the curves become more and more sharp, while increasing Q, the curves tend to flatten out.

The converter is designed so that it will operate at resonant frequency at the nominal input voltage. According to Equation 24, it maintains that of Equation 32, which when solved, is shown in Equation 33.

EQUATION 32:

$$M(f_r) = 2n\frac{V_{o,nom}}{V_{in,nom}} = 1$$

EQUATION 33:

$$n = \frac{V_{in,nom}}{2V_{o,nom}}$$

Observing the curves in Figure 23 and Figure 24, a fundamental property appears: in any case all curves always cross each other at the same point corresponding at $f_n = f_r$, that is at resonance; the voltage conversion ratio at this point is 1 (with the suggested turn ratio). This means that such a selection of n will guarantee that at nominal conditions, the correct output voltage will be generated, independently on the specific M curve the system is currently on.

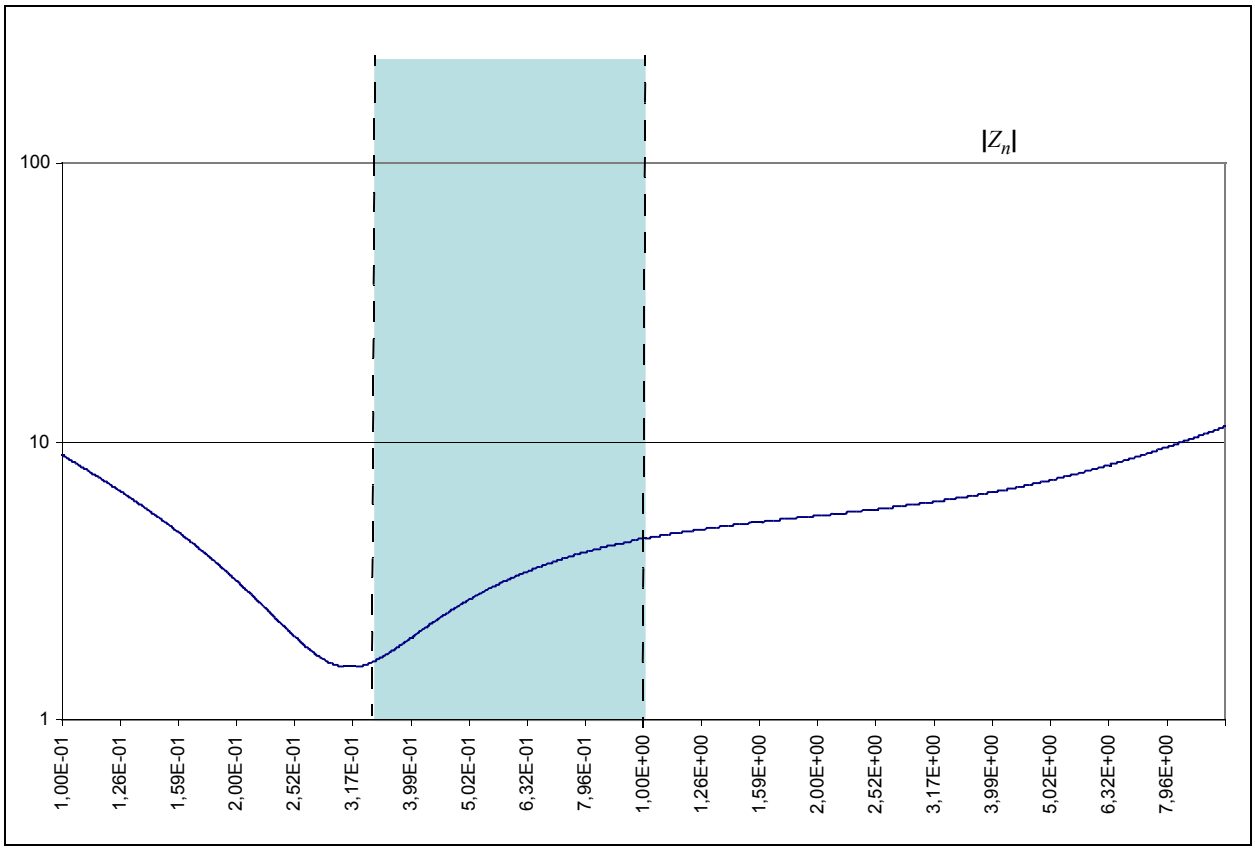
Figure 25 plots the circuit input impedance (Z_{in} defined in Equation 11). In this figure, a portion of the plane has been highlighted; it is the portion of the frequency axis (for $f \le f_n$) where the input impedance presents a positive slope. Remembering that the transfer function of an inductor has the same kind of behavior, we can determine that the LLC circuit is seen by the input circuit and the sinusoidal input voltage waveform as an inductor. This is extremely important to enable the converter to achieve very small (turn-on) switching losses, as shown in subsequent sections. On the contrary, the slope of Z_{in} to the far left of the figure is negative, which means the system has a capacitive behavior. This also means that a point exists, on the Z curve, that defines the border between capacitive and inductive equivalent behavior.

It can be shown that the input impedance Z_{in}, if a complex function, results in Equation 34.

EQUATION 34:

$$Z_{in} = f(f_n, \lambda, Q)$$

FIGURE 25: INPUT IMPEDANCE



As for the voltage gain, it is thus possible to draw a family of curves using λ and/or Q as parameters. For each curve, it is possible to determine a point where the behavior of the converter changes from capacitive to inductive as described previously. All of these points make up a locus, which is represented in Figure 26 by the blue line. In the frequency range below the resonant frequency, that is for $f < f_n$, the area to the right of this curve (shaded regions in Figure 26) is where the converter has inductive behavior. Obviously the operating point must be in this area, for frequencies lower than the resonant frequency.

A second limit of the available operating area in the M plane can be determined reasoning that having a negative Q has no meaning. Thus the lowest value that Q can have is Q = 0. Again, a curve of the gain can be drawn in such a situation. The available area is then shown in Figure 27.

The intersection of the two possible areas is shown in Figure 28.

Two additional limits that can be determined, which depend on the minimum and maximum input voltage. Using Equation 31 with the two extreme voltages, the two following relationships are derived, as shown in Equation 35 and Equation 36, which are plotted in Figure 29.

EQUATION 35:

$$M_{\min}(f) = 2n\frac{V_o}{V_{in,\max}}$$

EQUATION 36:

$$M_{\max}(f) = 2n\frac{V_o}{V_{in,\min}}$$

Considering all of the limitations defined previously, the area (for $f < f_n$) highlighted in Figure 30 is available for the converter operation.

FIGURE 26: LIMIT BETWEEN THE CAPACITIVE AND INDUCTIVE REGIONS AND THE ACCEPTABLE AREA BELOW RESONANCE

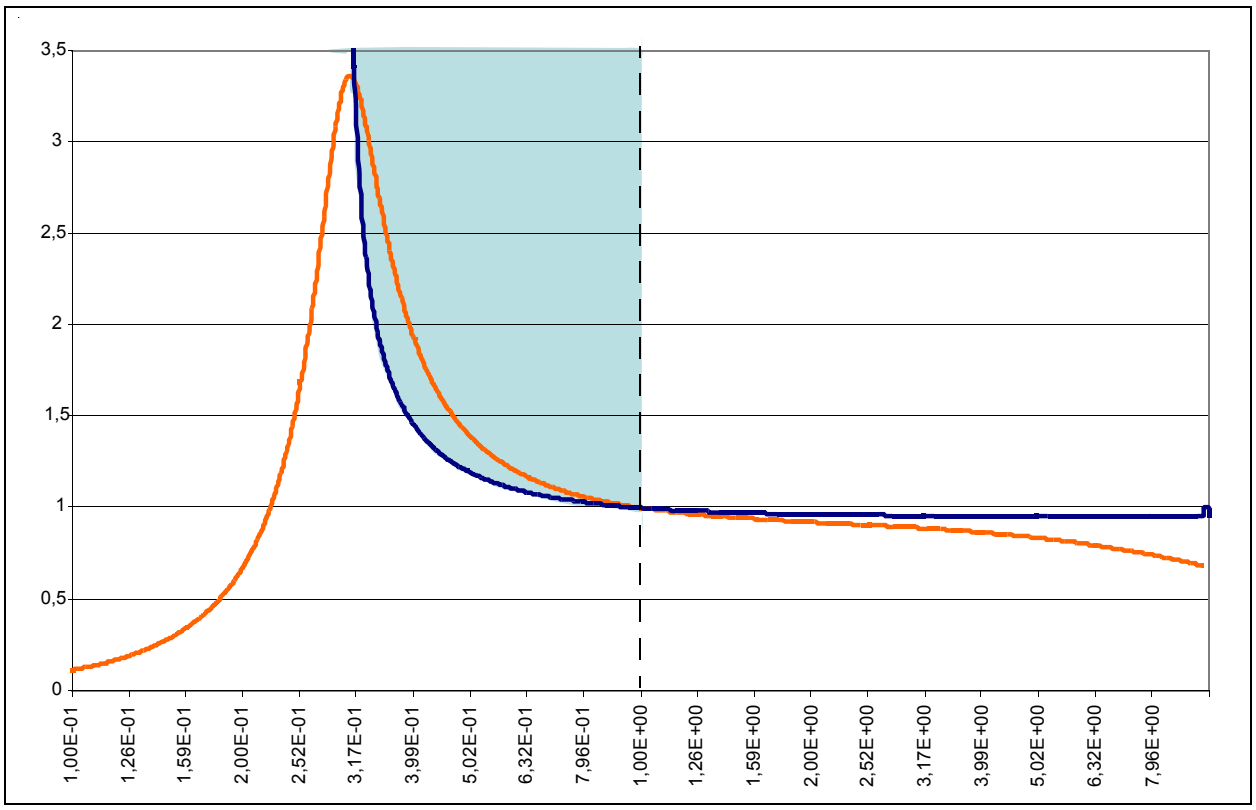


FIGURE 27: ACCEPTABLE AREA BELOW RESONANCE DELIMITED BY Q ≥ 0

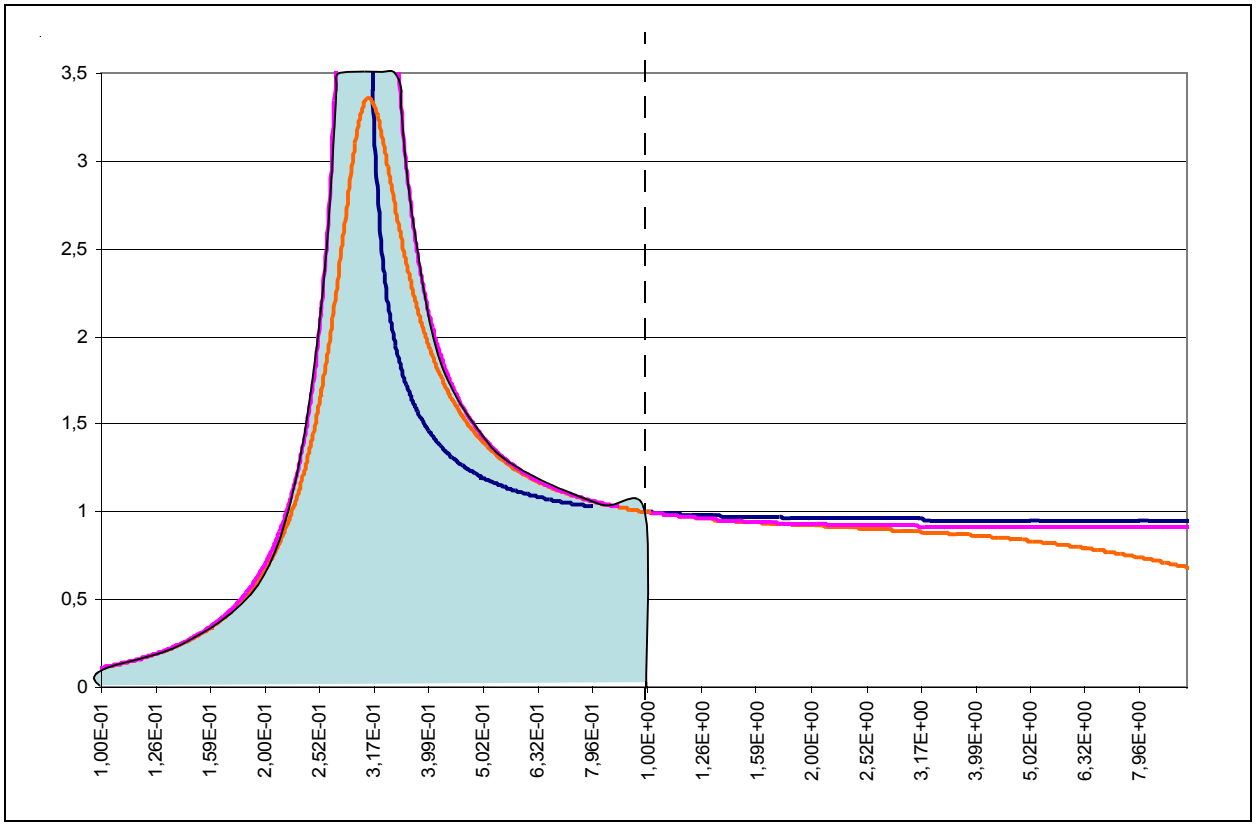


FIGURE 28: AVAILABLE M PLANE AREA WHERE BEHAVIOR IS INDUCTIVE AND Q > 0

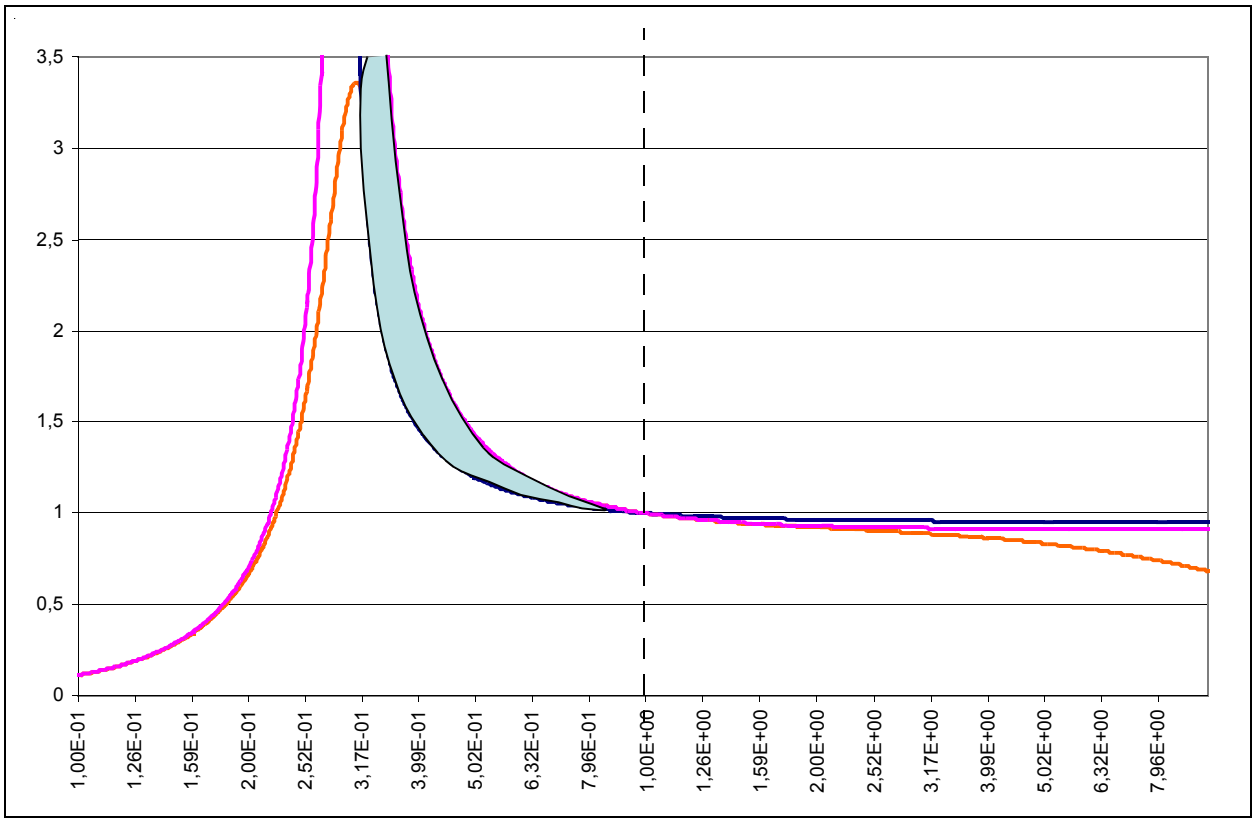


FIGURE 29: MINIMUM AND MAXIMUM ACCEPTABLE GAINS

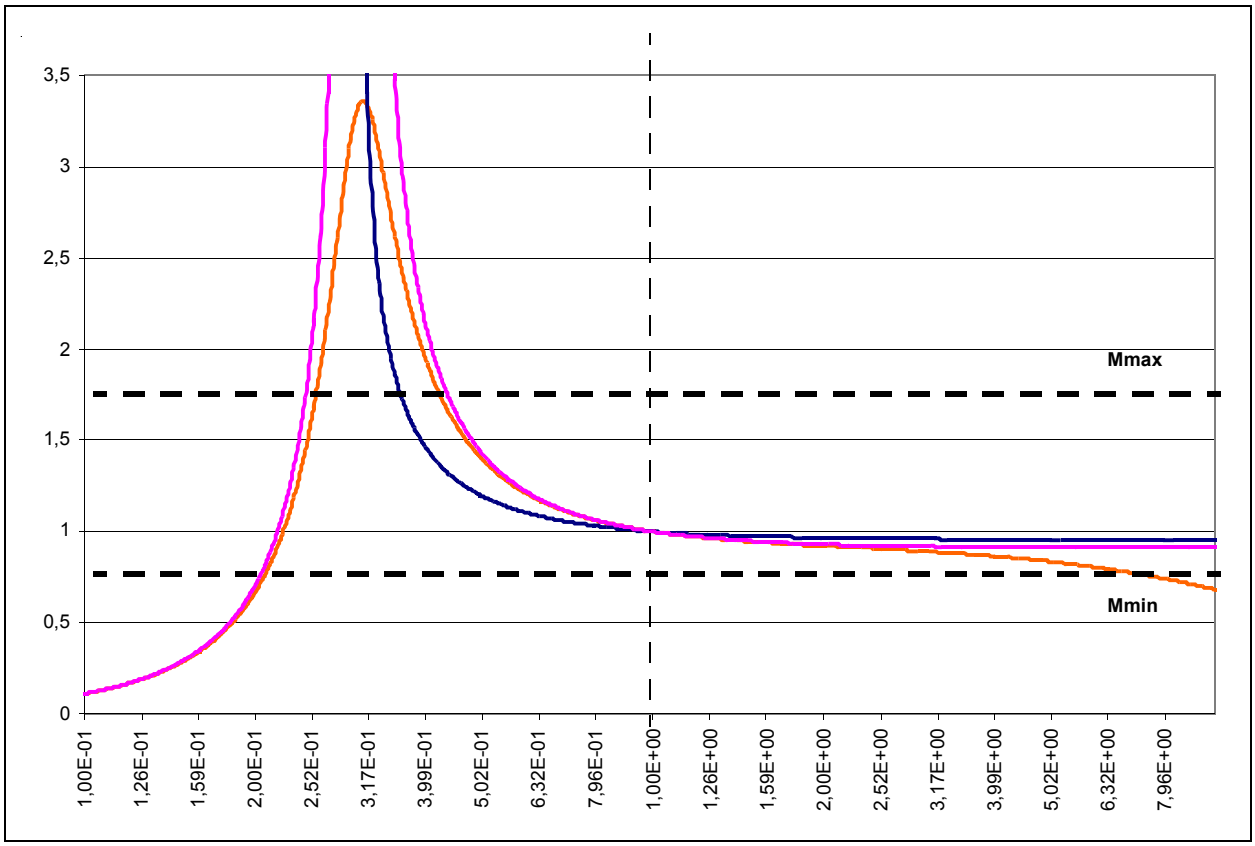
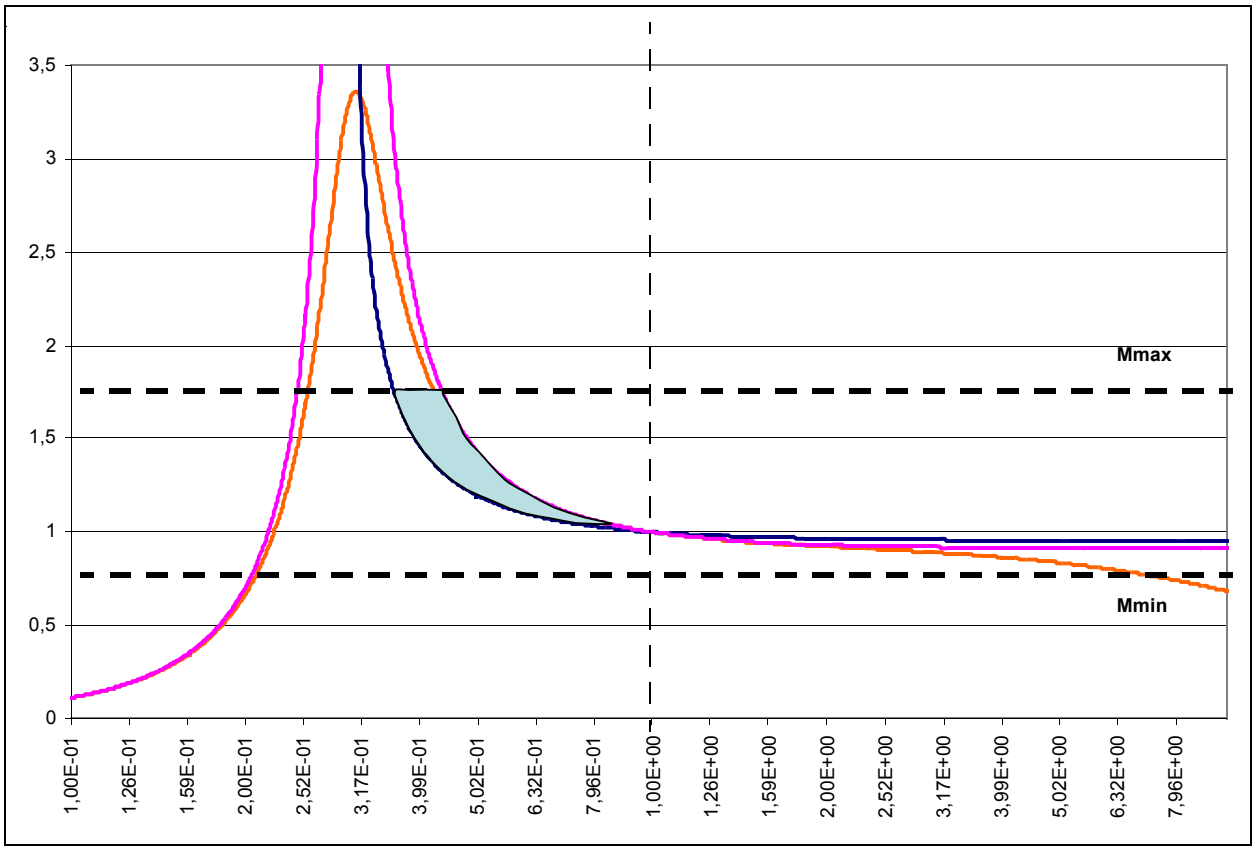


FIGURE 30: OVERALL M PLANE ACCEPTABLE AREA



OPERATION OF THE LLC CONVERTER

Zero Losses at MOSFET Turn-on

Before going into greater detail regarding the operation of the converter at, below, and above resonance, it is useful to consider what happens to the tank circuit when a square voltage waveform is applied. As explained previously, this results in a sinusoidal current waveform. In general terms, there are two possible situations of the relative position in time of the current versus the voltage waveform. If the current leads the voltage the behavior corresponds to that of a capacitor. However, this is of no interest.

Instead, as stated above, we operate the system in an area of its voltage conversion ratio $M(f)$ such that it appears to be inductive to the tank input current: that is, the current lags the voltage. Figure 31 shows the circuit that will be considered in this section, which is only the switching section of the half-bridge. The tank current is defined as positive if it exits the tank (midpoint between the two capacitors). Again D1 and D2, C1 and C2 are the equivalent lumped components of the system.

FIGURE 31: CIRCUIT USED TO INVESTIGATE MOSFET TURN-ON BEHAVIOR

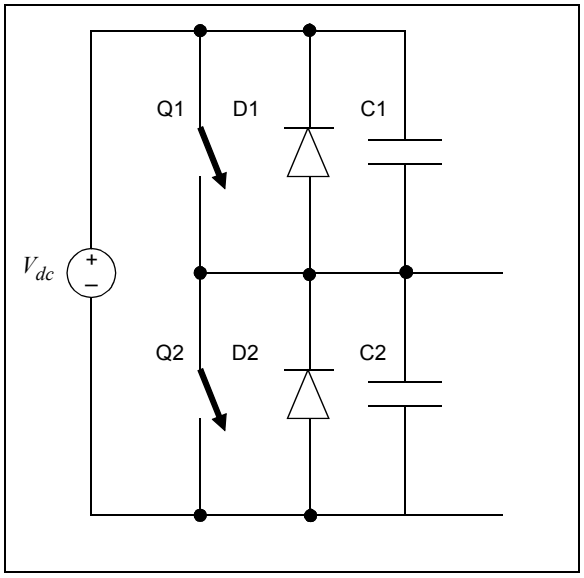


Figure 32 shows the MOSFET gate waveforms and the tank current.

At time t_0 the current is negative, and it enters the circuit as shown in Figure 33. Suppose for a while that the switch has not yet been turned on. The incoming current follows the indicated path through the upper diode D1. This means that the voltage across the switch is very close to zero. The switch can be operated with very small losses. As a consequence, the switch can be operated at any instant in time within the interval t_0 to t_1: the losses will always be very small.

During the interval t_1 to t_2, switch Q1 is closed and the current flows through it (Figure 34).

At time t_2, Q1 is opened. The current is positive and can easily flow through the lower diode D2 (providing that the lower switch is not immediately operated) (Figure 35). Again, the voltage across the lower MOSFET will be close to zero and lossless commutation is possible. In fact, as for Q1, the lower switch can be turned on at any time during this interval. the ideal turn-on of the MOSFET is when there is zero voltage across the drain to the source of the MOSFET.

Then, in interval t_3 to t_4, the lower MOSFET is conducting, as shown in Figure 36.

FIGURE 32: VOLTAGE AND CURRENT WAVEFORMS

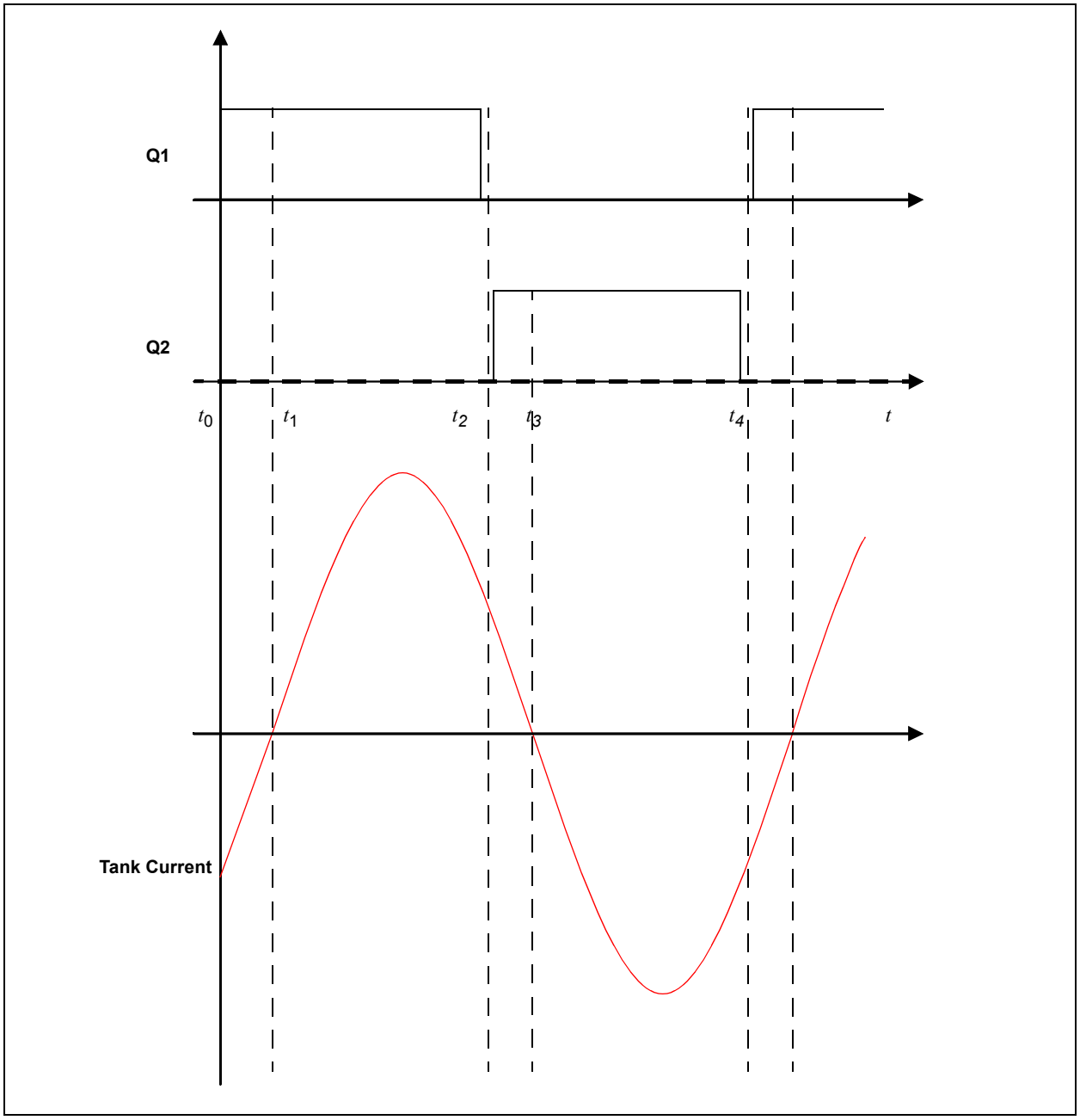


FIGURE 33: TIME INTERVAL t_0 TO t_1: TANK CURRENT CAN FLOW THROUGH DIODE

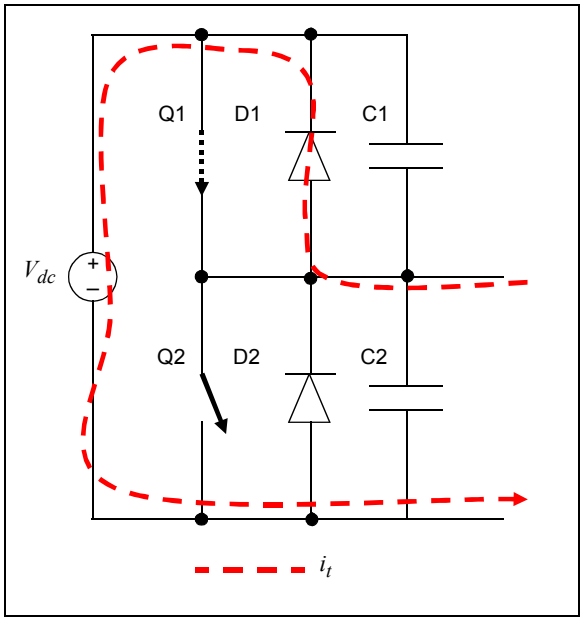


FIGURE 34: TIME INTERVAL t_1 TO t_2: TANK CURRENT FLOWS THROUGH UPPER SWITCH

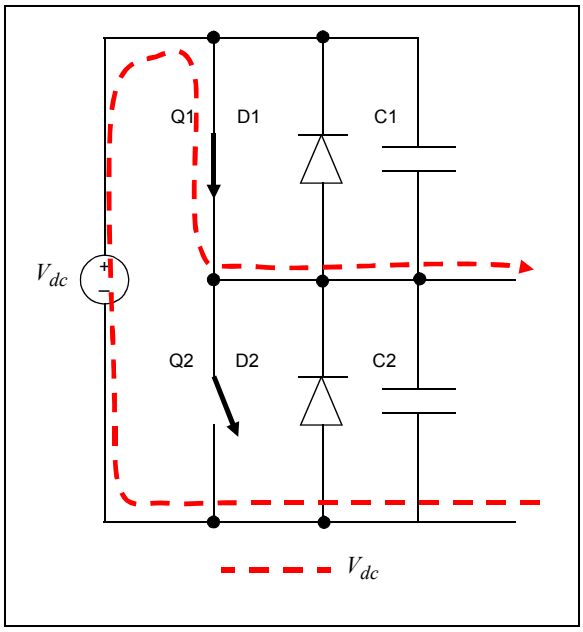


FIGURE 35: TIME INTERVAL t_2 TO t_3: TANK CURRENT CAN FLOW THROUGH DIODE

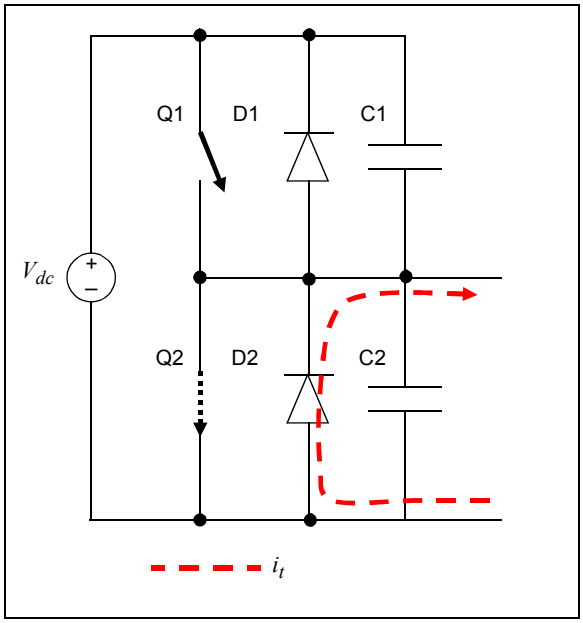
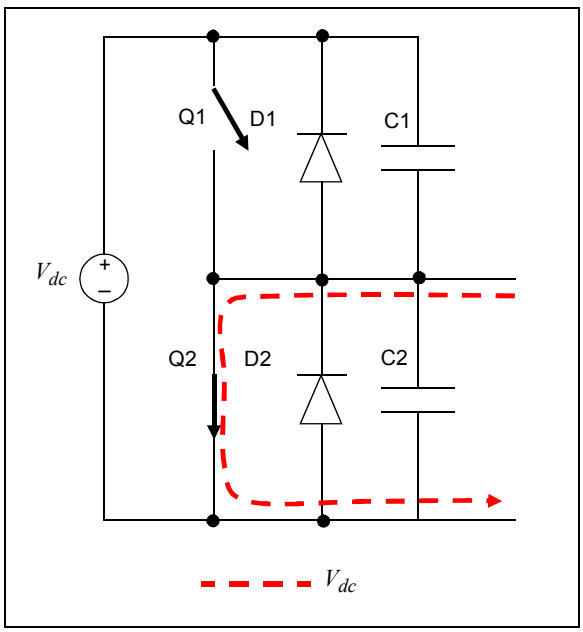


FIGURE 36: TIMER INTERVAL t_3 TO t_4: TANK CURRENT FLOWS THROUGH LOWER SWITCH



Circuit Operation at Resonance

This section describes the operation of the LLC converter at resonance, which is when the MOSFETs are operated at the same frequency as the resonant frequency, as set by the selected components. Refer to the circuit diagrams in Figure 37 through Figure 42 and to the plot of the most important waveforms in Figure 43. Note that, for each MOSFET, the anti-parallel diode (body diode or external diode) and the parasitic C1 and C2 capacitances have been added. This is because they take an active part in the system behavior. Also note that C1 (and C2) lump the MOSFET drain to source capacitance and any other stray capacitance in the circuit. A last note concerns the secondary side. In this discussion diodes are going to be used as a rectifying circuit (while the reference design implements a synchronous rectifier) because this will clarify the circuit operation and will help in determining the requirements to the secondary synchronous MOSFET switching time.

In the following sections analysis will be extended to both above resonance and below resonance.

Figure 43 shows the following signals:

- A: gate signal for upper MOSFET Q1
- B: gate signal for lower MOSFET Q2
- C: currents flowing in the primary side; there are two components: the magnetizing current (dashed, red) and the tank current (solid line, black)
- D: drain to source voltage on upper MOSFET Q1; note that this is also the voltage across cap C1
- E: drain to source voltage on lower MOSFET Q2; note that this is also the voltage across cap C2
- F: secondary side current in diode D3
- G: secondary side current in diode D4

Circuit operation is analyzed in adjacent time intervals.

In general terms the primary current is made up of two components: the magnetizing current ($i_m(t)$) which does not contribute to power transfer to the converter output and the tank current ($i_t(t)$) that is responsible for the power transfer (Figure 37).

$t < t_0$: (Figure 38) Q1 off; Q2 on; D3 off; D4 on

This is the starting condition for the analysis. Q2 is closed and will be switched opened right at time t_0. The voltage drop on the upper cap C1 is V_{dc}.

$t_0 < t < t_1$: (Figure 39) Q1 off; Q2 off (dead time); D3 off; D4 off

Since both switches are open, no energy is supplied by V_{dc} to the circuit. The only current flowing into the primary is the magnetizing current, which remains constant ($i_m(t)$) during this time interval. This current splits between the two MOSFET caps, discharging C1 and charging C2. One key point here is that the magnetizing current must be big enough to complete the caps charge/discharge operations before the end of the dead time. The designer must select the components and dead time duration to fulfill this requirement. At t_1, the voltage on C2 will be slightly bigger than V_{dc} and the voltage on C1 will be slightly negative, which will allow D1 to start conducting.

At the secondary both diodes D3 and D4 are open, and the output cap C_o supplies energy to the output to maintain the voltage V_o.

$t_1 < t < t_2$ (Figure 40) Q1 off→on; Q2 off; D3 off→on; D4 off

As anticipated above, diode D1 starts conducting. The voltage drop on it is very close to zero. MOSFET Q_1 can be closed at any time during this interval: the voltage drop on it is almost zero, so that the turn-on losses are pretty close to zero. Zero Voltage Switching (ZVS) is obtained. While only D_1 only is conducting, the primary current is again the magnetizing current, which does not participate in energy transfer. But as soon as Q1 is closed, the input generator V_{dc} supplies the power to be transferred to the output. Note that during this time interval, the tank current is negative, meaning it flows into V_{dc}.

$t_2 < t < t_3$ (Figure 41) Q1 on; Q2 off; D3 on; D4 off

This is the first half period during which power transfer takes place. As can be seen from the waveform plots, both components of the primary current are significative. The magnetizing current is generated by the secondary voltage (V_o) reflected back to the primary. This voltage is directly across L_m, so that the magnetizing current is calculated, as shown in Equation 37, which shows a linear behavior.

EQUATION 37:

$$i_m(t) = i_m(t_1) + \frac{nV_o}{L_m}t$$

ΔI in Figure 43 (waveform C), clarifies the amount of current that is effectively available for energy transfer.

The tank current is expressed by Equation 38.

EQUATION 38:

$$i_t(t) = \sqrt{2} I_{P,rms} \sin(2\pi f_r t + \varphi)$$

Note that at resonance, at time t_3, the tank current exactly equals the magnetizing current. This, then, is the current flowing into Q1 when it opens. This current should be as small as possible to have low turn off switching losses. Unfortunately two conflicting requirements on the magnetizing current are involved. The first one (see the interval t_0 to t_1 description) requires it to be large enough to charge/discharge the parasitic capacitances within the dead time duration. Because of Equation 37, this means having a small value of L_m. The second one is to have $i_m(t_3)$ as small as possible to reduce losses (which means a large value of L_m). Some kind of trade-off must be performed by the designer. One possible approach is to select a rather large value of L_m giving preference to the fulfillment of the ZVS requirement.

$t_3 < t < t_4$: (Figure 42) Q1 off; Q2 off (dead time); D3 off; D4 off

The circuit behavior is complementary to the previous dead time interval. Again, the only current flowing into the primary is the magnetizing current, which remains essentially constant. This current splits to charge C1 and at the same time discharge C2. During this period, the voltage $v_{ds1}(t)$ grows to slightly above V_{dc} and at the same time the voltage on C2 falls to slightly less than 0V. In a symmetrical way compared to the previous dead time interval, this will enable D2 to start conducting.

The circuit operation from t_4 to t_7 is the reverse of the first half cycle.

A final note on Figure 43. Signals F and G represent the secondary current; its amplitude is shown graphically with the vertical blue lines.

FIGURE 37: LLC CIRCUIT WITH MAGNETIZING AND TANK CURRENTS SHOWN

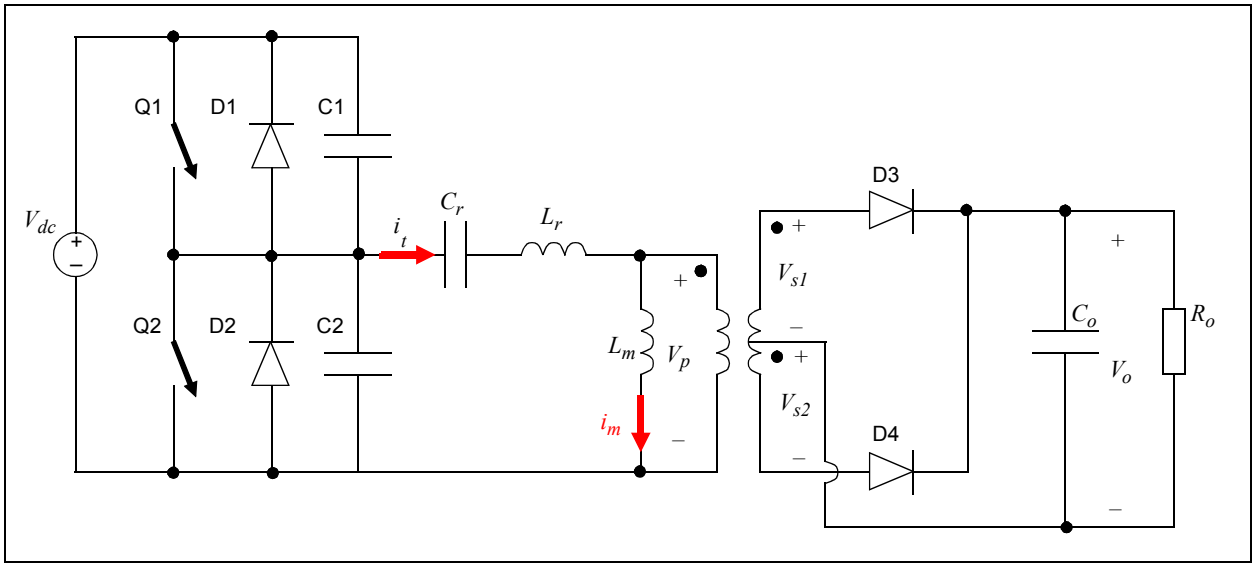


FIGURE 38: LLC CIRCUIT AT TIME INTERVAL $t < t_0$

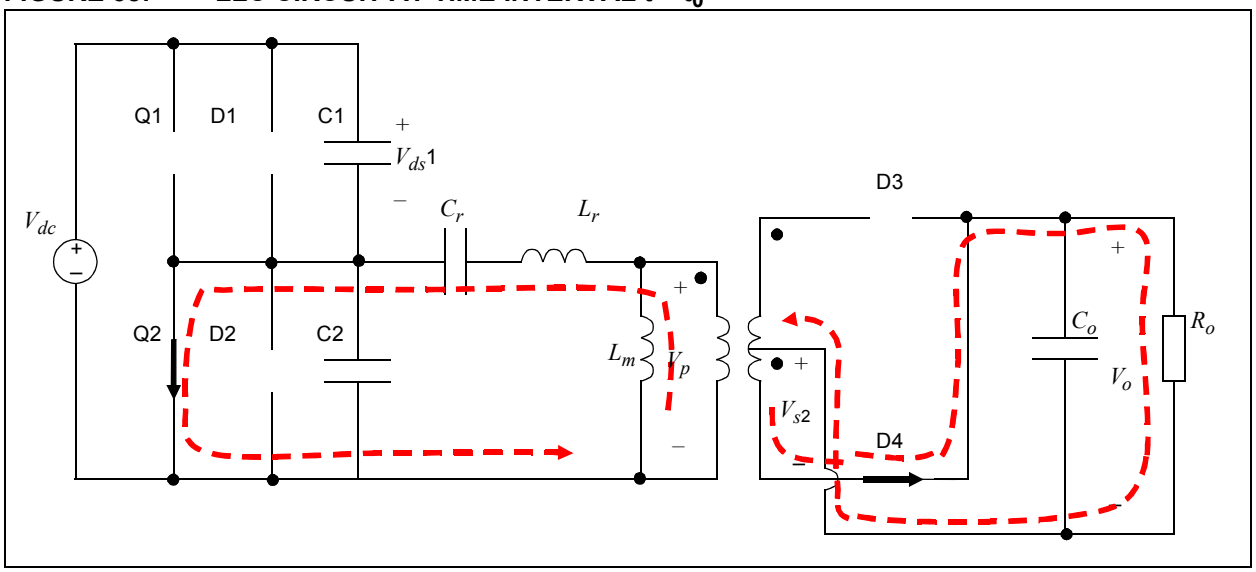


FIGURE 39: LLC CIRCUIT AT TIME INTERVAL t_0 TO t_1

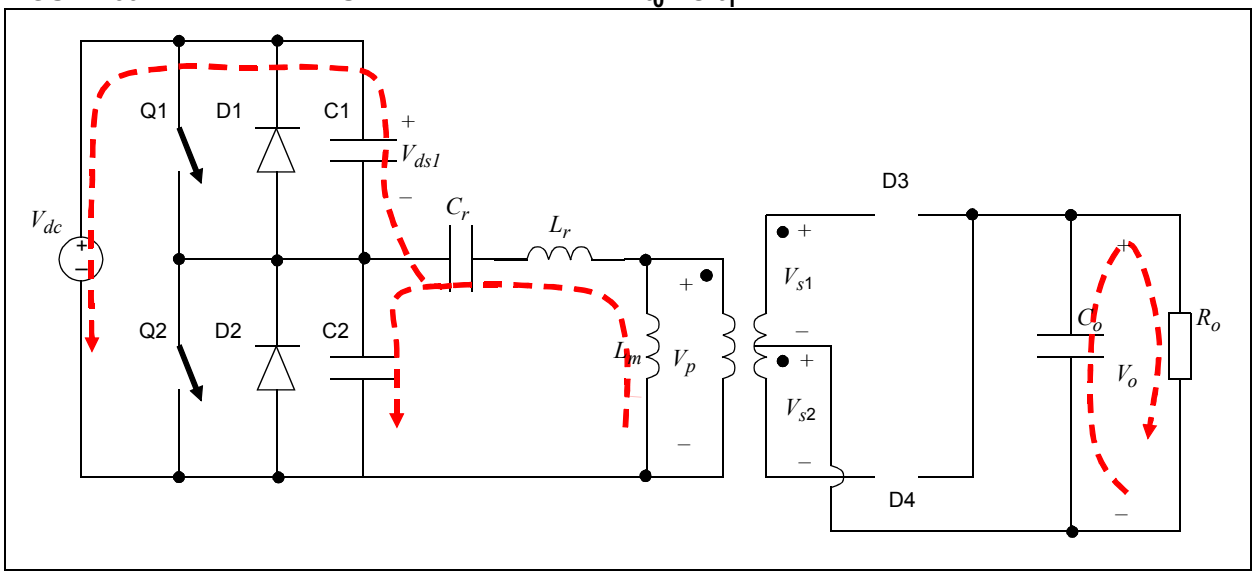


FIGURE 40: LLC CIRCUIT AT TIME INTERVAL t_1 TO t_2

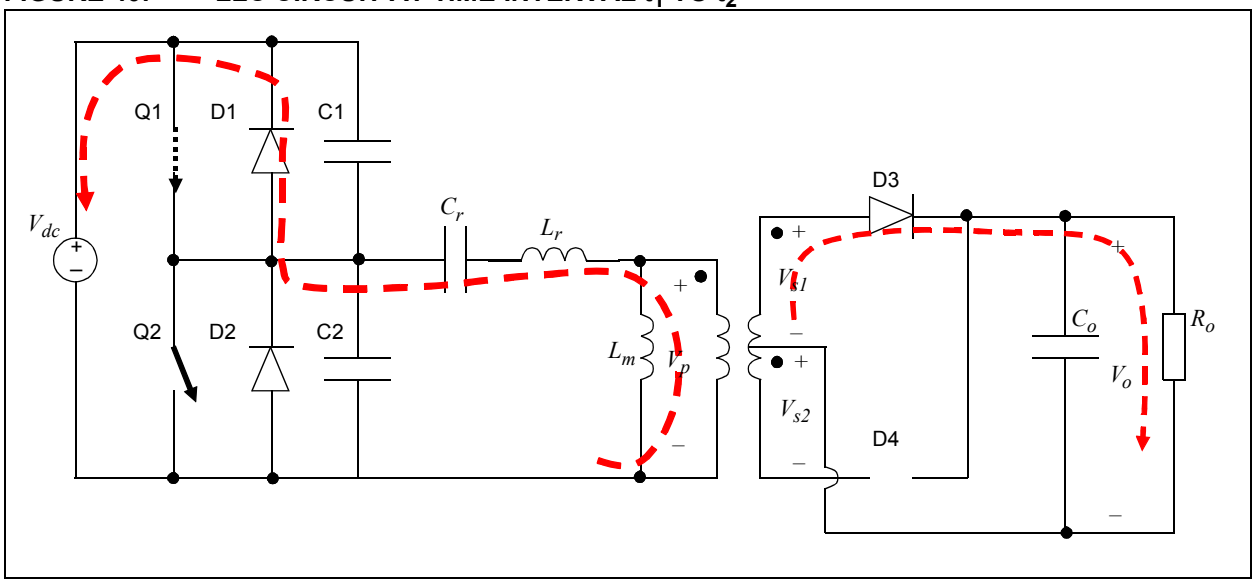


FIGURE 41: LLC CIRCUIT AT TIME INTERVAL t_2 TO t_3

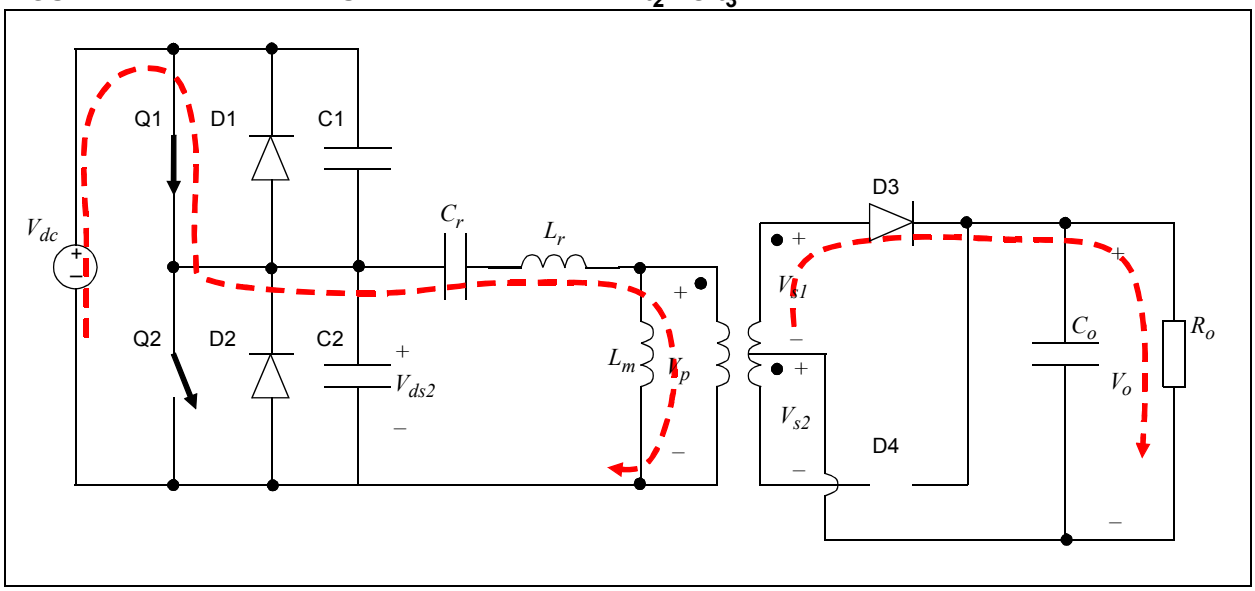


FIGURE 42: LLC CIRCUIT AT TIME INTERVAL t_3 TO t_4

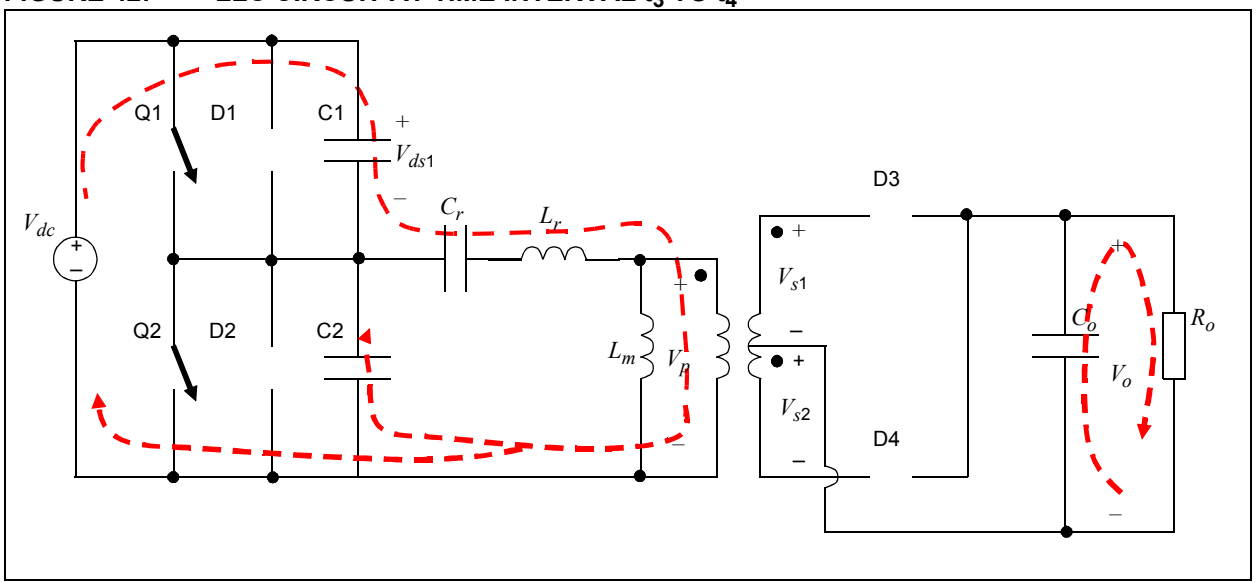
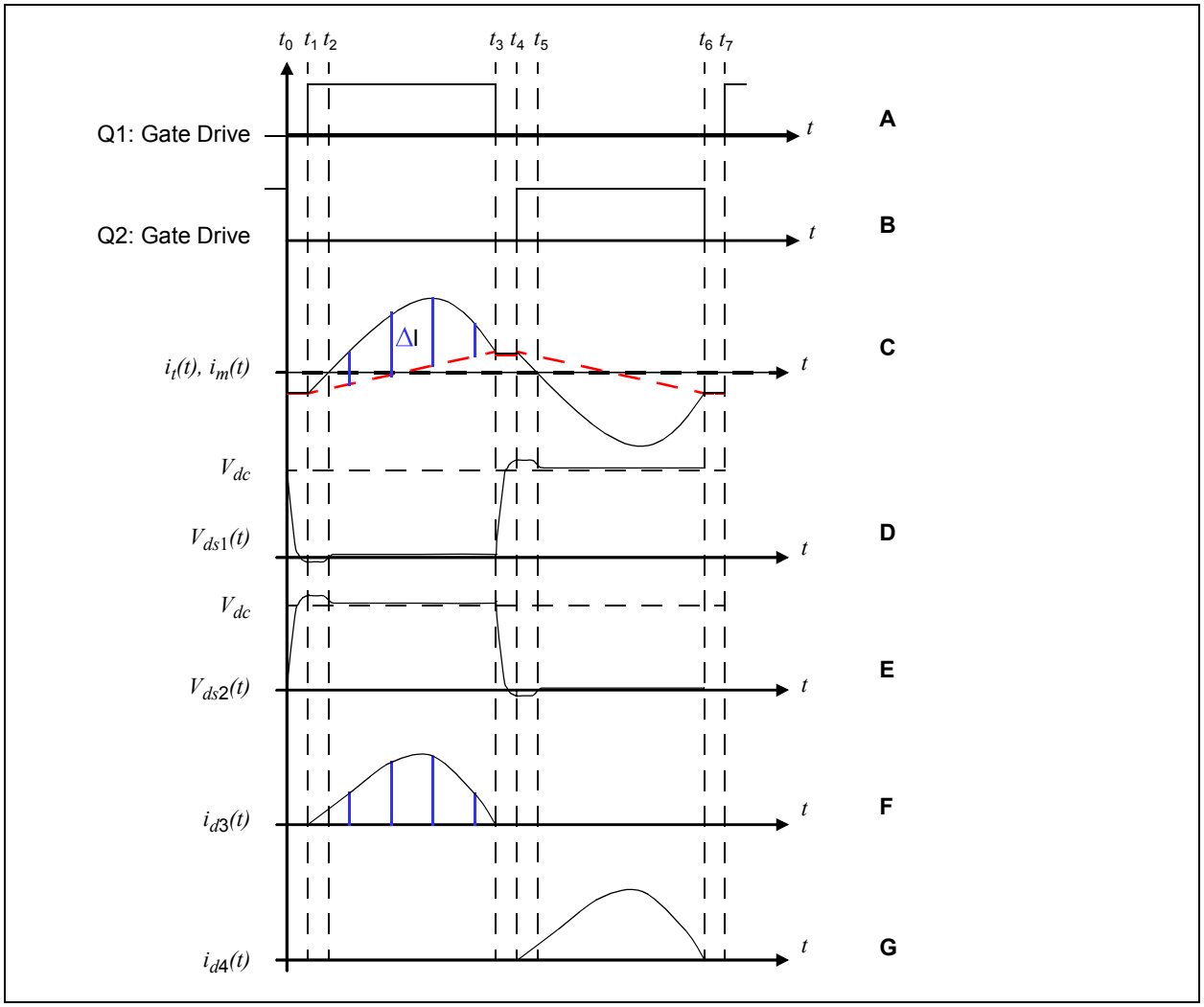


FIGURE 43: RELEVANT LLC WAVEFORMS



Circuit Operation Below Resonance

Circuit operation below resonance is calculated by Equation 39.

EQUATION 39:

$$f_{sw} < f_r \Rightarrow T_{sw} > T_r$$

Essentially, the circuit behavior is similar to that at resonance. However, there are some significative differences that directly influence the secondary side switching behavior. Figure 44 shows the relevant waveforms and should be compared to Figure 43.

Since the tank fundamental sine wave has a shorter period compared to the switching period, the tank current will equal the magnetizing current before the half period ends. This is highlighted in Figure 44. From that point on, the current flowing in the primary is the magnetizing current only.

It is important to note that when using diodes at the secondary, they will stop conducting at the right time (as soon as the current goes to zero). However, in a synchronous implementation, diodes are replaced by MOSFETs and their gate must be driven correctly. The designer must find a strategy to determine the exact time when the secondary MOSFETs are to be turned off. A number of different techniques have been developed, usually requiring some kind of indirect current sensing (that is, for example, measuring the voltage drop across the MOSFETs themselves).

Circuit Operation Above Resonance

Circuit operation above resonance is calculated by Equation 40.

EQUATION 40:

$$f_{sw} > f_r \Rightarrow T_{sw} < T_r$$

The circuit behavior is somehow reversed compared to the operation below resonance. Refer to Figure 45. Since the resonant period is longer that the switching period, at the end of the switching half period, the tank current is higher than the magnetizing current. During the dead time the tank current falls rapidly to the value that the magnetizing current has, so that a new half cycle can start.

It should be clear that above resonance the synchronous switches can be turned on and off at the same time as the primary switches. This makes their control very easy.

From the preceding discussion is should be clear that the secondary MOSFET's control depends on the relative value of the switching and resonant frequencies. The firmware manages this issue.

FIGURE 44: CIRCUIT BEHAVIOR BELOW RESONANCE

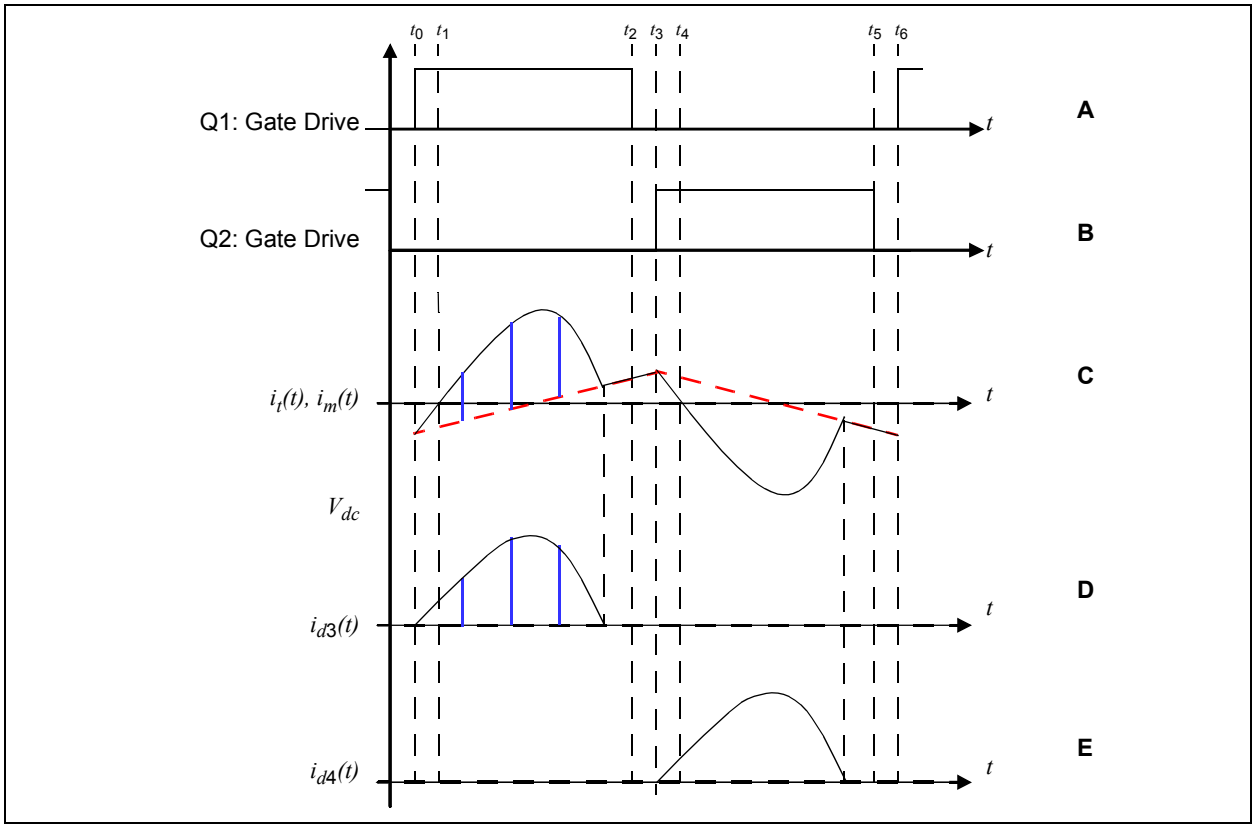
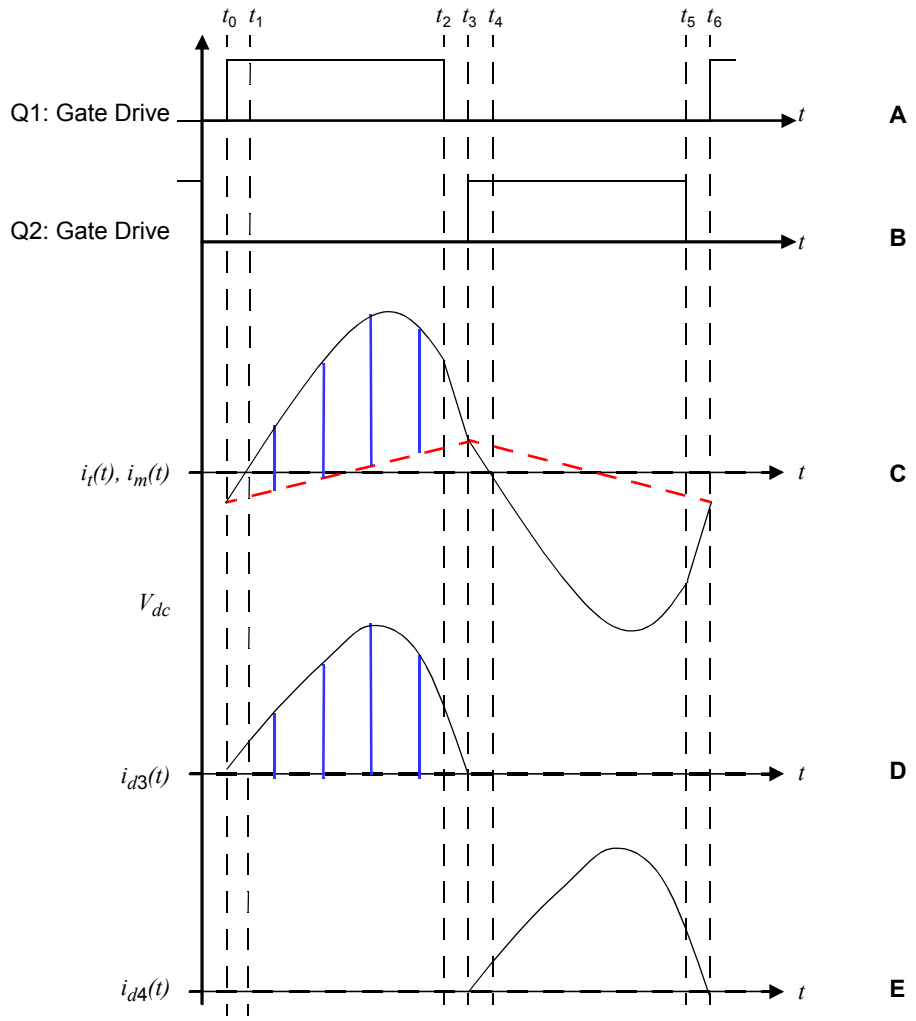


FIGURE 45: CIRCUIT BEHAVIOR ABOVE RESONANCE



SYNCHRONOUS RECTIFICATION

As previously discussed, the secondary side has been designed using a synchronous rectifier, instead of using diodes. The reason for this choice has been to reduce conduction losses at the secondary. The power dissipated on a diode has two contributions: the losses due to the forward resistance (R_f) and the losses due to the diode forward voltage. Therefore, the total diode loss can be computed, as shown in Equation 41.

EQUATION 41:

$$P_{loss,diode} = V_F I_{D,ave} + R_F I^2_{D,rms}$$

Where,

V_f is the diode forward voltage

$I_{d,ave}$ and $I_{d,rms}$ are respectively the average and *rms* forward diode currents

R_f is the diode forward resistance (usually in the range of a few tens of mOhms)

If the diode is replaced by a MOSFET acting as a switch, the losses are depicted by Equation 42.

EQUATION 42:

$$P_{loss,MOSFET} = P_{conduction} + P_{switching}$$

Where,

$P_{conduction}$ are the conduction losses, or in other terms:

$$P_{conduction} = I^2{}_{MOSFET,rms}\ R_{DS,on}$$

and $P_{switching}$ are the switching losses.

The interesting thing is that in the LLC converter, the secondary switches are always operated while the current flowing through them is zero. Refer to Figure 43 for curves G and H, and Figure 44 and Figure 45 for curves D and E. As already stated previously, only at a switching frequency below resonance could the option exist to turn off the secondary switches with a non-zero current. It is the responsibility of the designer to find the correct strategy to guarantee that such an event does not occur.

As far as the possible topology, the designer can choose between some very common topologies:

- Full wave rectifier, diode bridge
- Full wave rectifier, center tapped

The solution used in the reference design is the latter. Usually the center tap is connected to the secondary ground; however, in the reference design it has been connected to the positive output. The reason for this is that, as can be seen in the schematic, such a topology allows the sources of both MOSFETs to be connected to ground. This makes the driver circuit much easier, since it is not required to have any kind of bootstrap circuit.

The traditional approach would have required a bootstrap circuit since the n-channel MOSFET needs a gate voltage higher than the source voltage to operate. However, when conducting, the source and drain voltages would essentially be the same. Since in such a situation the gate to source voltage (V_{gs}) cannot be greater than the threshold voltage (V_{th}), as the MOSFET would never operate properly.

The full-wave diode bridge is common in applications that have a high output voltage and a low output current

REFERENCE DESIGN HARDWARE OVERVIEW

The LLC reference design can be logically divided into two sections: the converter itself and the auxiliary power supply. The converter is then split into a primary section and a secondary section; the isolation between the two sections is obtained through the resonant transformer. The dsPIC DSC, controlling all power transfer and supervision operations, is located on the secondary side. This enables easy implementation of power management communication and eases supply and grounding connections. The nominal switching frequency (and thus resonant frequency) has been selected at 200 kHz, to be a reasonable trade-off between high speed and small passive components from one side and the possibility to implement sophisticated control loops and auxiliary functions on the other.

Figure 46 presents the high level block diagram of the LLC converter.

Figure 47 shows a high level representation of the complete circuit, where:

- high voltage connections are highlighted with black bold line
- the 12V tracks to supply power to the components are drawn in blue
- the 3.3 V track is drawn in green

A Schottky diode separates the 12V generated by the flyback circuit from the 12V generated by the LLC converter.

FIGURE 46: HIGH-LEVEL LLC CONVERTER BLOCK DIAGRAM

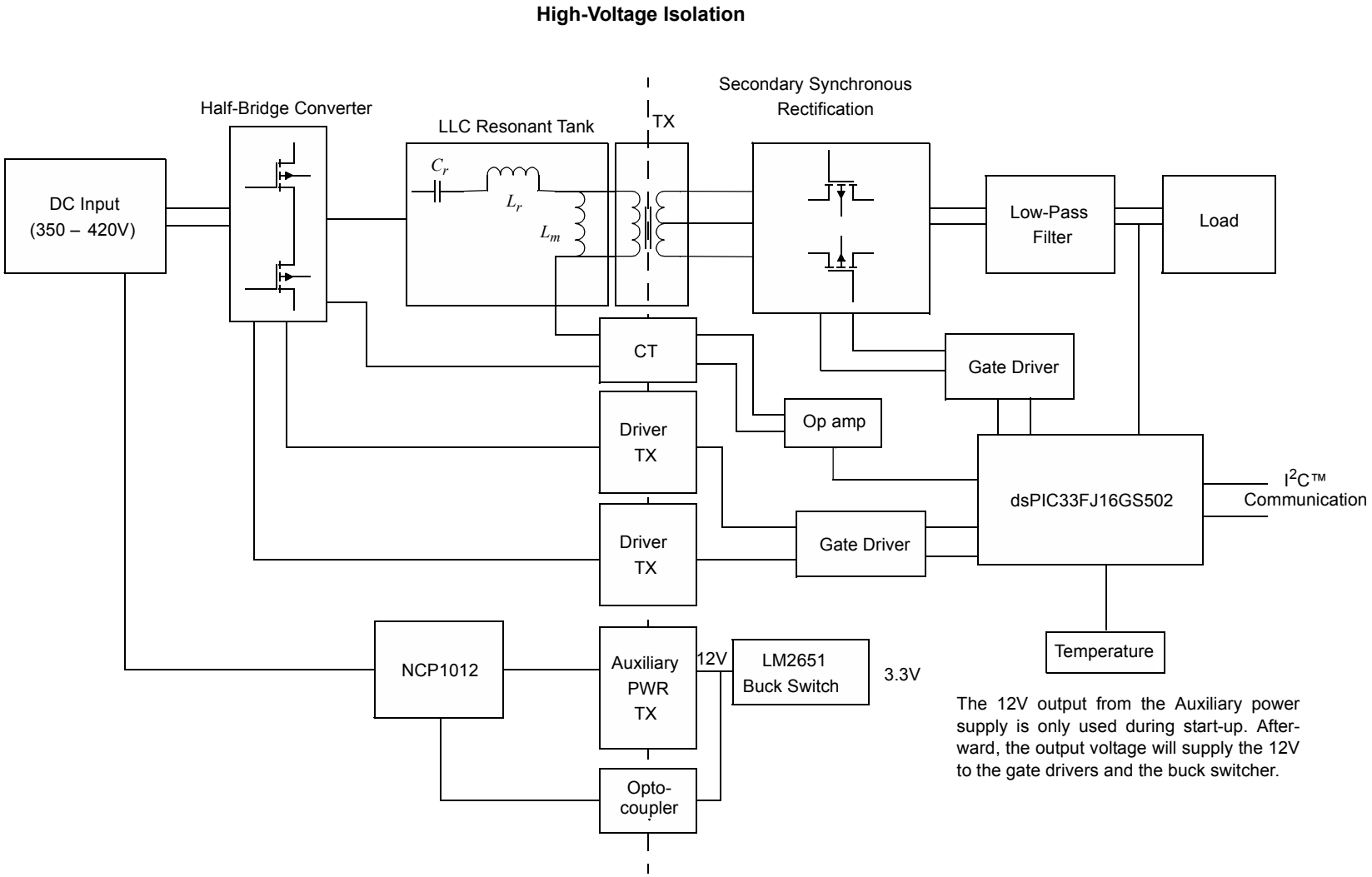
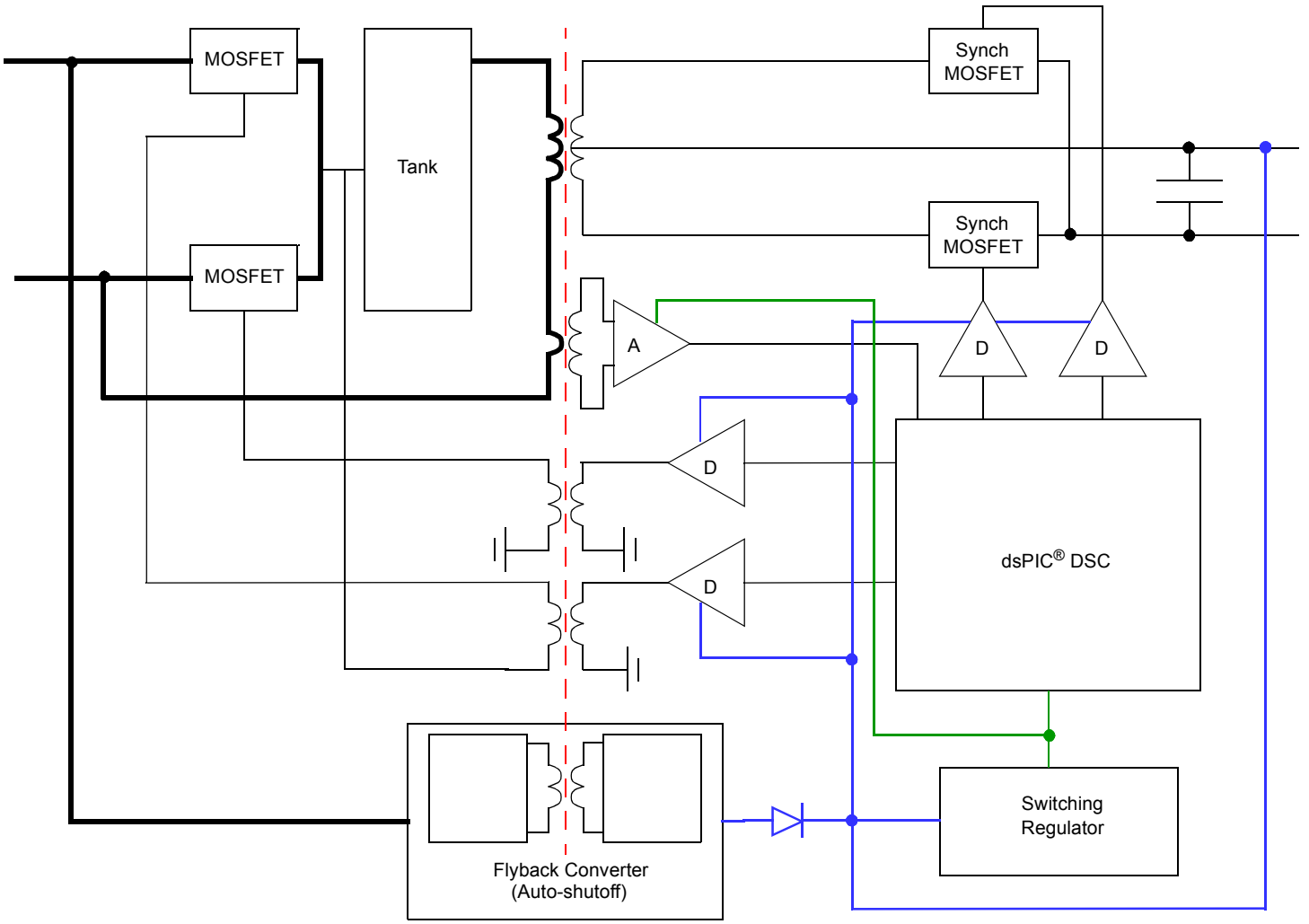


FIGURE 47: HIGH-LEVEL LLC CONVERTER BLOCK DIAGRAM (D: MOSFET DRIVER; A: AMPLIFIER)



Half-Bridge MOSFETs

The operation of the two MOSFETs is designed to alternatively connect the tank circuit input to the input high rail (400 V_{dc} nominal) and to ground. Positive dead time is inserted on each commutation edge to prevent shoot-through. With this operation, the half-bridge MOSFETs are not subjected to any particular turn-on stress. Since the maximum input voltage is defined as 450 V_{dc}, a safe selection of these parts would be choosing MOSFETs with a breakdown voltage in the range of 600-700 V_{dc}.

A gate to source resistor of 10 kΩ is added to both MOSFETs to prevent accidental MOSFET turn-on due to noise. Series resistors are added to control the rate at which the MOSFETs turn ON or OFF.

As explained in previous sections, the current flowing into the MOSFETs is the magnetizing current and the tank current. A rough evaluation of the tank current is described in the following paragraphs.

The output power is 200W. Considering a converter efficiency of 95%, the resulting input power is shown in Equation 43.

EQUATION 43:

$$P_{in} = P_{out} / 0.95 = 200 / .95 = 210W$$

The maximum average input power is shown in Equation 44.

EQUATION 44:

$$P_{in} = V_{rms} I_{rms} = V_{in,\min} \frac{I_{pk,\max}}{\sqrt{2}}$$

Equation 45 shows the input current.

EQUATION 45:

$$I_{pk,\max} = \frac{\sqrt{2} P_{in}}{V_{in,\min}} = \frac{\sqrt{2}\, 210W}{350V} = 0.85A$$

Taking some margins we can set I_{pk} = 2 A.

Input capacitance C_{ISS} (or better total gate capacitance) is an important parameter for the definition of the driver: the larger the capacitance the more drive current required to charge/discharge this capacitance. See additional details in the **"Hardware Drivers"** section.

Output capacitance is of interest also, because as explained earlier, this capacitance must be charged to V_{in} or discharged to zero during dead time to achieve zero voltage switching. Output capacitance is listed in the MOSFETs data sheet as C_{OSS}; however this value should be increased to take care of the stray capacitance that should be lumped into it.

TABLE 3: INPUT MOSFET SUMMARY

Parameter	Value
Breakdown voltage	650 V
Continuous current	9A @ 25°C
$R_{DSon,\ max}$	385 mOhm
Input capacitance (C_{ISS})	790 pF typical
Output capacitance (C_{OSS})	38 pF typical
Total Gate Charge (Q_g)	17 nC typical

Tank Circuit

Three elements must be determined in the design of the tank circuit: L_m, L_r, C_r. There are a number of equations that relate these values (refer to Equation 25 to Equation 30) to each other and to the desired converter performances. Usually, the system has more variables or parameters than equations, so the designer is forced to take some decisions based on experience or common sense. This is the reason why a wide number of different techniques can be used in the selection of the components.

One of them is to examine the plots of the voltage ratio $M(f_{sw})$, consider the limitations and available areas in its plane that have been identified previously, and select a suitable value of the λ and Q parameters.

EQUATION 46:

$$n = \frac{400}{2 \bullet 12} = 16.667$$

EQUATION 47:

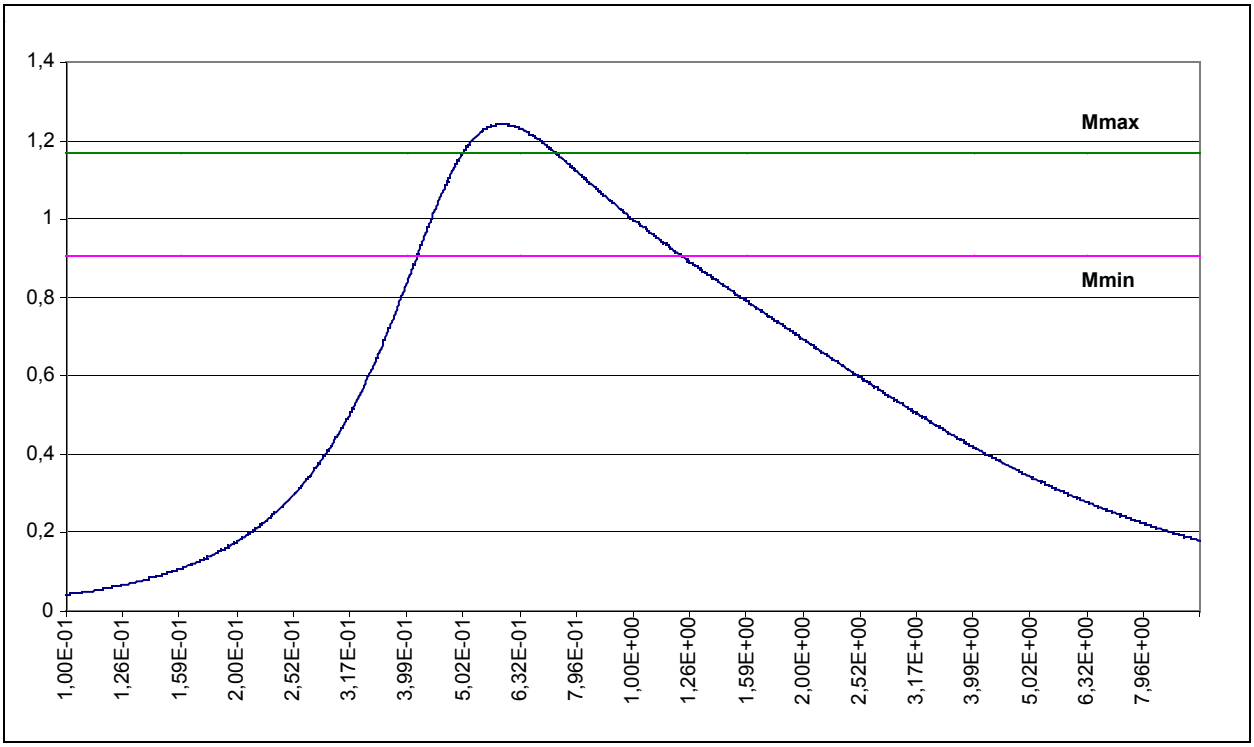
$$M_{\min}(f) = 2n \frac{V_o}{V_{in,\max}} = 2 \bullet 16.667 \bullet \frac{12}{450} = 0.889$$

EQUATION 48:

$$M_{\max}(f) = 2n \frac{V_o}{V_{in,\min}} = 2 \bullet 16.667 \bullet \frac{12}{350} = 1.143$$

See Figure 48 for the two values (Mmin and Mmax) that have just been determined

FIGURE 48: VOLTAGE CONVERSION RATIO (*M(f)*) AND GAIN LIMITS IMPLEMENTED IN THE REFERENCE DESIGN



In the implementation of the reference design, the λ and Q parameters have been selected as: λ = 0.25 and Q = 0.5.

The rationale behind the choice of such values is that the corresponding voltage gain plot supports the required max gain also permitting some margin (around 10%).

Using equations Equation 29 and Equation 30, C_r can be computed as:

EQUATION 49:

$$C_r = \frac{\pi I_{out}}{16 f_r Q n^2 V_{out}} = 10nF^*$$

*For the reference design, a value of 9.4nF was selected.

EQUATION 50:

$$L_r = \frac{1}{4\pi^2 f_r^2 C_r} = 67\mu H$$

EQUATION 51:

$$L_m = \frac{L_r}{\lambda} = 270\mu H$$

From the analysis of the plot in Figure 48, some additional information can be derived. First, the minimum operating switching frequency is determined by the intersection of the *M(f)* plot and the Mmax plot. The resulting value is 155 kHz.

Similarly, the maximum switching frequency is determined as the intersection of the *M(f)* plot and the Mmin plot. The resulting value is 220 kHz.

Some additional notes on the implementation of L_m and L_r. As already stated, they are both realized by the transformer. In a real transformer the total magnetizing inductance is given by the sum of L_m and L_r. This can be easily proved with two experimental tests. The first test consists of measuring the primary inductance with the secondary open: in this case, the measure gives the L_m + L_r value. The second test consists, again, of measuring the primary inductance – this time with the secondary short-circuited. The measured value is now the leakage inductance.

Figure 49 shows the model of a transformer, taking into account the leakage inductance at the primary and secondary, the winding resistance and the equivalent core resistance; these two terms are useful in determining the transformer losses. All secondary related terms have been moved to the primary to determine the relationship between these inductance values and the L_m and L_r inductance as needed by the resonant converter. In Figure 50, all inductances have been lumped together to simplify the model. The model in Figure 53 is preferred, since L_r and L_m are measurable parameters.

- R_1: primary winding resistance
- L_{li}: primary winding leakage inductance
- L_m: magnetizing inductance
- R_m: resistance modeling core losses (equals v_m^2/R_m)
- L'_{l2}: secondary winding leakage inductance reflected to the primary. $L'_{l2} = n^2 L_{l2}$, with L_{l2} being the secondary winding leakage inductance
- R'_2: secondary winding resistance reflected to the primary, $R'_2 = n^2 R_2$, with R_2 being the secondary winding resistance

FIGURE 49: TRANSFORMER MODEL TAKING INTO ACCOUNT LEAKAGE INDUCTANCES AND RESISTANCES

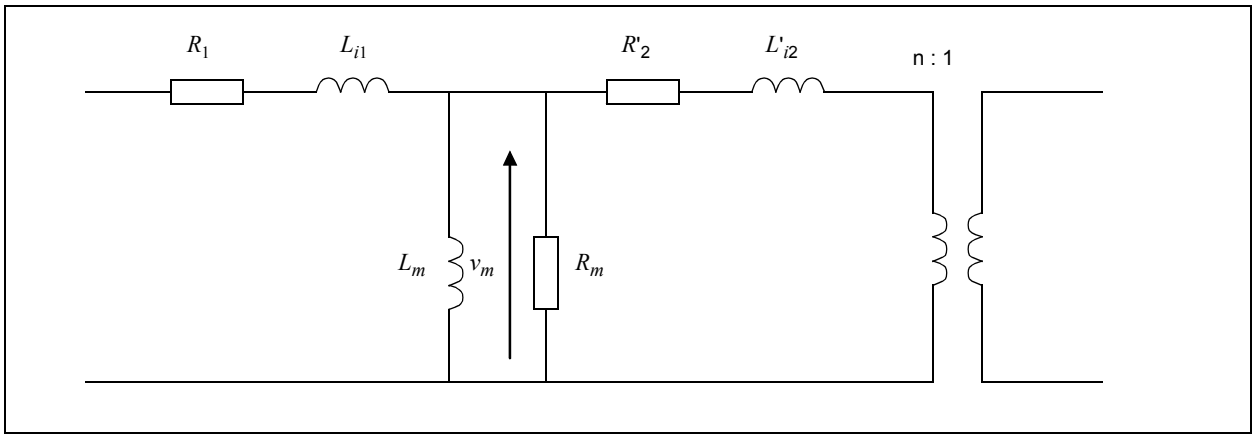
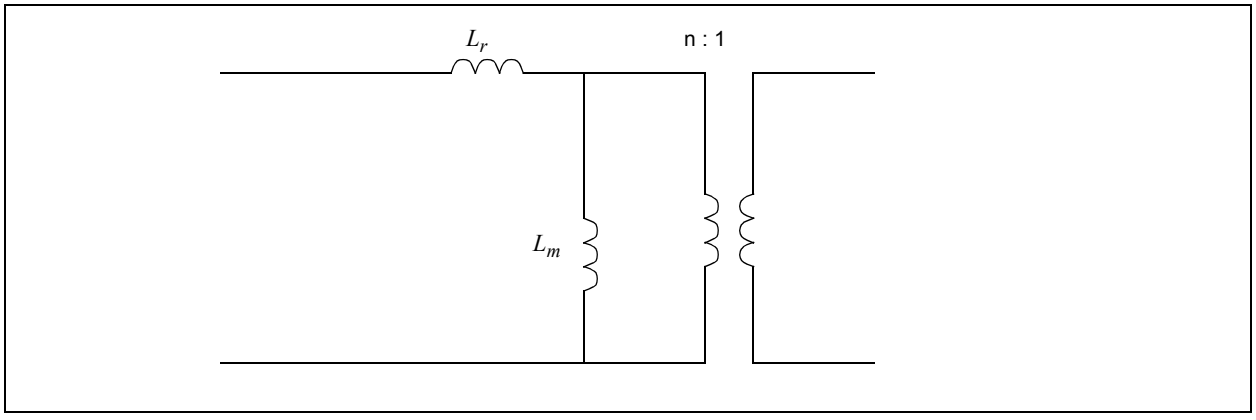


FIGURE 50: TRANSFORMER MODEL TAKING INTO ACCOUNT INDUCTANCES ONLY



According to Figure 49, the total leakage inductance at the primary terminals is calculated in Equation 52.

EQUATION 52:

$$L_{pri} = L_m + L_r = L_m + L_{l1} + \left(L_m \| n^2 L_{l2}\right)$$

L_{pri} can be easily determined, measuring the primary inductance with the secondary windings open. The results are shown in Equation 53.

EQUATION 53:

$$L_{pri}(\text{measured}) = 330\mu H$$

The resonant inductance as shown in Equation 53 is calculated in Equation 54.

EQUATION 54:

$$L_r(\text{measured}) = 62\mu H$$

The results of these two calculations are shown in Equation 55.

EQUATION 55:

$$L_m = L_{pri} - L_r = 330\mu H - 62\mu H = 268\mu H$$

It is possible to define a gain of the transformer, as shown in Equation 56.

EQUATION 56:

$$G_{transformer} = \sqrt{\frac{L_m + L_r}{L_m}} = \sqrt{\frac{330\mu H}{268\mu H}} = 1.11$$

Equation 57 shows the transformer winding ratio.

EQUATION 57:

$$n = 16.667 \cdot 1.11 = 18.5$$

The resulting transformer will then have 56 turns at the primary and three at each secondary.

The transformer bobbin is ETD34 and the core material is 3C90. The expected losses are approximately 2W. As the turns ratio is 18.667, there are three turns on the secondary and 56 turns on the primary. Litz wire has been used on the secondary (three parallel wires of 40 gauge, 175 strands) as well as the primary (two parallel wires of 40 gauge 10 strands). The gap is approximately 2 mm.

With this transformer an external inductor to boost the leakage inductance of the transformer may be needed.

In summary, the components values and parameters limits are shown in Table 4.

TABLE 4: TANK CIRCUIT SUMMARY

Parameter	Value
C_r	9.4 nF
L_r	62 µH
L_m	268 µH
Q	0.42
Resonant Frequency	210 kHz

Hardware Drivers

Drivers are required for the main switches because of the high voltage involved and the required commutation speed.

A driver is selected according to its current sourcing capability. The reason is that the gate of a MOSFET presents a high capacitance value. This capacitance has to be charged/discharged in a time that is essentially dependent on the rise and fall times of the MOSFET itself. Designers have to find a driver that is capable of supplying all the required current to allow the MOSFET to have a fast transition. However, while a fast rise and fall time enables reducing switching losses, it will at the same time increase EMI and may introduce high frequency ringing due to lead and circuit inductances.

As soon as the rise/fall time have been defined, the required peak current can be computed from the basic equation of a capacitor, as shown in Equation 58.

EQUATION 58:

$$T_{rise}\ (or\ T_{fall}) = \frac{V\,C}{I}$$

Where,

V is the gate voltage

C is the gate capacitance

The value of C is determined by the gate to source capacitance (C_{GS}) plus the gate to drain capacitance (C_{GD}) due to Miller effect. So it is not correct to evaluate C as the C_{ISS} parameter that can be found in MOSFET data sheet. Instead the value of C can be computed looking at the total gate charge (Q_g) which is another parameter in MOSFET data sheets and applying the simple relation between charge and capacitance, as shown in Equation 59.

EQUATION 59:

$$C = Q_g / V_{GS}$$

This is the value of C that must be used in the previous equation.

The value of Q_g is not a constant, obviously. It should not be a surprise that Q_g depends on the V_{gs} voltage. The MOSFET data sheet should have a graph like Figure 51, where the effective Q_g at the correct V_{gs} and V_{ds} value can be determined.

Two different resistors have been used at the driver's output to enable different paths for the current during the rising and falling edges. This changes the rise/fall times of MOSFET.

The driver's output signals are conveyed to the primary side MOSFET through a couple of signal transformers. DC blocking capacitors are added to prevent saturation of the drive transformers. The capacitors remove the DC off set and at a 50% duty cycle produce a gate voltage of ~6V.

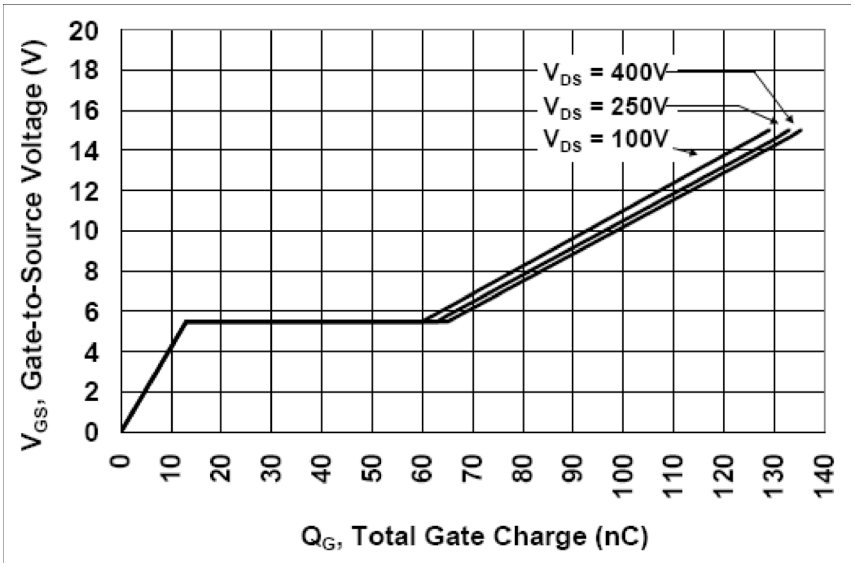
Current Transformer

A current transformer is used to acquire the current flowing into the primary side. The knowledge of this value, as explained, enables knowledge of the secondary side current also. The selection of the CT has been challenging because of the requirement of 4000V isolation. The turn ratio is 1:50.

Primary Voltage Measurement

The primary side voltage is detected at the common point of the two switches. A high voltage cap is used to cross the galvanic isolation barrier; at the secondary side, a resistor voltage divider reduces the voltage amplitude within the dsPIC DSC analog voltage input range.

FIGURE 51: TYPICAL MOSFET TOTAL GATE CHARGE VS. *Vgs*



Synchronous Rectifier

The output of the transformer is a sinusoidal waveform. A synchronous rectifier circuit is added to rectify the sinusoidal waveform to create a DC voltage. The synchronous rectifier is implemented with MOSFET switches. As explained in a previous section, the correct choice of the instant in time when to turn-off these MOSFETs enables (very) low switching losses. Conduction losses then remain as the main source of power consumption. This leads to the selection of very low $R_{DS,on}$ MOSFETs.

The turn-on time is not an issue since the MOSFETs follow the primary switched turn-on timing.

TABLE 5: SYNCH RECTIFIER MOSFETs

Parameter	Value
Breakdown voltage	30V
Continuous current	85A
$R_{DSon,\ max}$	5.8 mOhm
Input capacitance (C_{ISS})	2150 pF
Output capacitance (C_{OSS})	480 pF
Total Gate Charge (Q_g)	15 nC typical

Output Filter

The inductor is 4.7 µH with a DCR of 1.5 mOhms. The capacitor is 330 µF.

Current Amplifier

A non-inverting op amp with a gain of 2 is used to buffer and amplify the primary current signal acquired by the current transformer. Diodes on the input create a full wave rectifier circuit; diodes are also added on the output to protect the circuit and following stages from high voltage transients.

Auxiliary Power Supply - Flyback

During the normal system operation, the controller, analog parts and drivers derive their supply from the main converter output; a stand-alone high efficiency synchronous switching regulator chip is used to derive the 3.3V from the converter 12V nominal output.

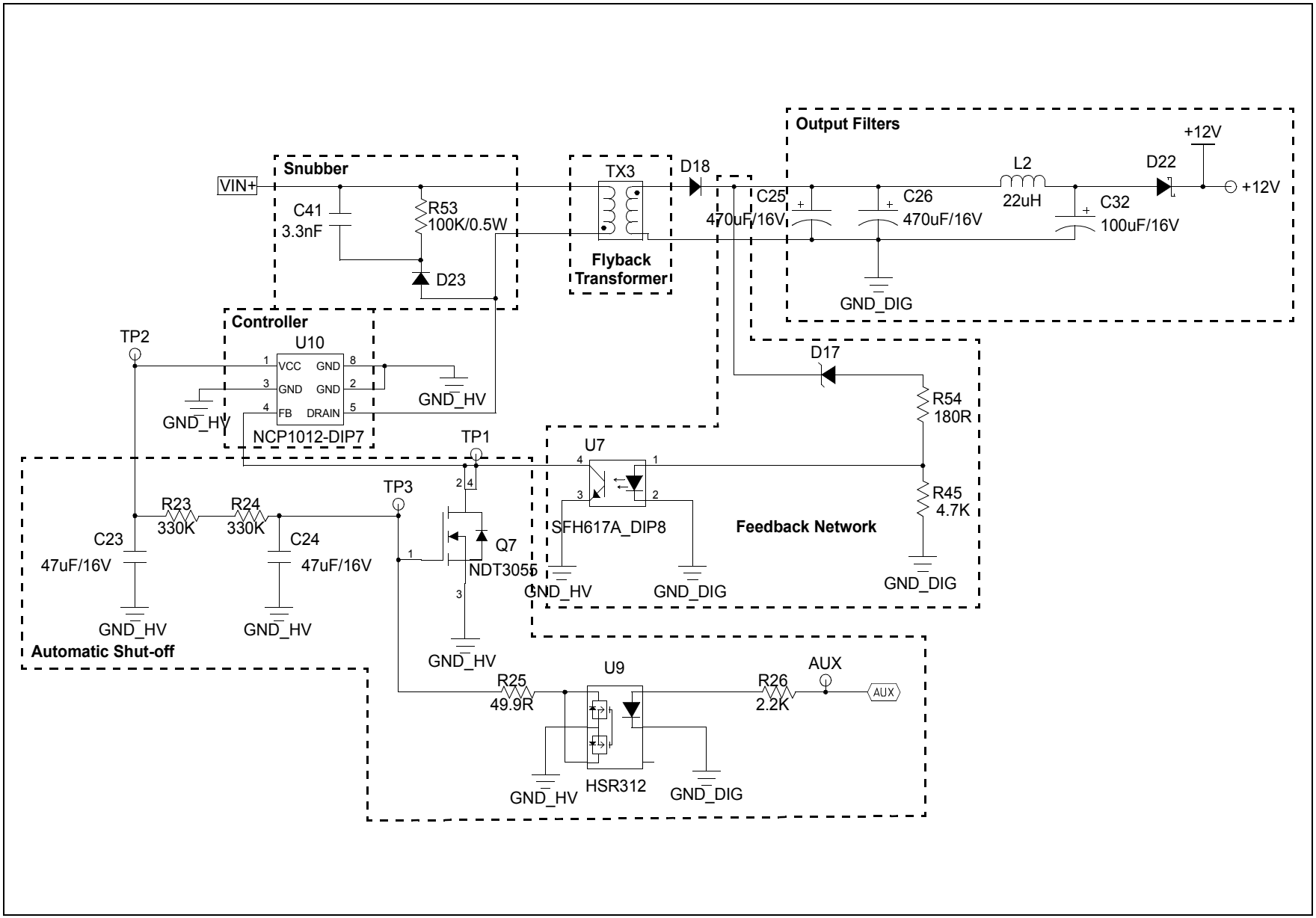
There are, however, two situations where the 12V output voltage is not available, that is at start-up and if any faults occur, with the consequence of a fast PWM shutdown operated by the dsPIC DSC to prevent serious damages. The auxiliary power supply must cope with these problems.

An additional fundamental requirement is to minimize the power consumption of the flyback converter. This had two consequences:

- Selection of the high efficiency 3.3V regulator
- Implementation of a circuit that is capable of auto-shut off when the main converter is up and running

Figure 52 shows details of the flyback circuit. The description in the sections that follow refer to this figure.

FIGURE 52: FLYBACK CIRCUIT



CONTROLLER

An NCP1012 device from ON Semiconductor® has been selected for the following reasons:

- Monolithic chip (almost everything needed is embedded in it)
- Can withstand high input voltages (up to 700 V_{dc})
- Can derive its own power supply from this high voltage rail
- Fixed frequency controller (100 kHz has been selected), implementing current-mode control
- Permits an easy implementation of the control loop, through the connection of its feedback input pin to an optocoupler, driven by the output voltage
- Can be easily switched OFF
- Implements internal protection strategies (short-circuit protection)

FLYBACK TRANSFORMER

The transformer design specifications derive from the power rating and the controller requirements.

The turns ratio is computed considering the flyback behavior at the instant in time when the flyback MOSFET opens. Applying Kirchoff's voltage law at the flyback primary side, the voltage on the switch can be computed as the sum of the input voltage (V_{in}), the output voltage (nV_o) reflected back to the primary and some additional headroom (V_x) which takes in consideration the voltage overshoot that appears at transients. This overshoot voltage, if not taken care of, is destructive. To control it a snubber circuit is added. The total voltage on the switch, as explained previously is shown in Equation 60.

EQUATION 60:

$$V_{sw} = V_{in} + nV_o + kV_x$$

Where, k is some value greater than 1

To prevent problems, this voltage must of course be less than the component rated breakdown voltage (700V). Solving this relationship on (n), the turn ratio is determined to be n = 15.

The transformer inductance value is selected in order to keep the system in discontinuous mode operation; this is required by the chip. According to the ON Semiconductor device data sheet, the inductance can be computed as shown in Equation 61.

EQUATION 61:

$$L = \frac{D_{\max} V_{in\min}}{f_{sw} I_{\max}} = 7.6uH$$

Where,

D_{max} = 0.5 is the max allowable duty cycle

V_{inmin} is the minimum input voltage (340V)

f_{sw} is the chip switching frequency

I_{max} is max peak current that is requested from the chip (using some guard band, this has been set at 225 mA).

For the transformer design, a number of considerations must be met:

- **Core material:** essentially depends on the switching frequency. Manufacturers provide plots that relate the material performances and frequency. These plots allow the selection of the correct material. Manufacturers very often also provide some additional guidance on the best fitting material, according to the kind of application the transformer is intended for. The material used in the flyback transformer is N87 (from the EPCOS Ferrites and Accessories catalog).
- **Core size:** essentially depends on the core losses and core temperature increase the designer can accept, in relation to the overall design economy. A standard core (E20/16/6 from EPCOS) has been chosen.
- **Number of turns:** Although very often the magnetics in a flyback converter is called an "inductor", in reality it is manufactured as a transformer. This means that the data we currently have (inductance value and turn ratio) are not enough to fully define the component.

  To proceed further, a core with a standard center gap has been selected in order to use an off-the-shelf part. Manufacturer can produce customer specific gaps, but of course this increases the cost and lead time of transformers. The introduction of a gap changes the transformer characteristics. In order to make things easy, manufacturers supply a parameter (AL) that tells how many nanoHenrys are obtained on the specific core plus gap for a one turn winding. In this design, based on the particular device available from the manufacturer, AL is close to 100 nH, so that the primary number of turns is computed as 272. From this value, and the turn ratio computed above, we also have the number of secondary turns (19).

- **Wire size:** Having selected the core size and the gap value (from the EPCOS data sheet, 5 10^{-2} cm), the maximum magnetic flux B in the core can be computed as a function of the primary turn ratio and max allowable current, resulting in B_{max} = 70 mT. The transformer manufacturer allows then, usually with a diagram, to determine the core losses corresponding to such a flux intensity.

  The selection of the wires is based on the assumption that the specific (per volume unit) core losses equal the specific losses in wires. This is a compromise that usually allows to keep the transformer temperature increase within reasonable values. Since the wire specific losses are function of the wire size, it should be clear that this allows to determine the AWG for both primary (AWG = 33) and secondary wires (AWG = 20).

SNUBBER

As already introduced previously, the snubber at the primary is needed to control (limit) the voltage overshoots that appear during switching, in such a way to guarantee that the total voltage on the MOSFET is always below its breakdown value. Here a max tolerable overshoot (on top of the input voltage plus output voltage reflected back to the primary) of about 60V has been computed (with some additional headroom). The additional voltage is due to the leakage inductance in series with the transformer primary.

Knowledge (or at least estimation) of the transformer leakage inductance allows to proceed with computations. The snubber operates in such a way that when the voltage increases too much, getting close to the switch breakdown voltage, the energy stored in the leakage inductance (that generates the voltage increase) is dissipated, through the diode, into the snubber resistors

FEEDBACK NETWORK

The flyback output needs to be regulated at 12V. A zener diode with V_z = 11V does not allow any current to flow in the feedback path until the output grows above 11V. From that point on, the zener current is set with the two resistors to be around 300 µA. Using Kirchoff's current and voltage laws and the selected optocoupler input characteristic, it is possible to determine the two resistor values (R1 = 4.7 kOhm, R2 = 280 Ohm).

The optocoupler output can be considered a current generator whose value is proportional to the converter output voltage. This current develops a voltage drop on a resistor internal to the ON Semiconductor; this voltage feedback is finally detected and used internally to the On Semiconductor chip, to control the peak current value flowing into the flyback primary winding.

AUTO SHUT-OFF CIRCUIT

As already stated, one of the main design targets of the auxiliary power circuit is to reduce its power when not effectively needed, that is when the main (LLC) converter is up and running. The power consumed by the auxiliary circuit during this time is completely wasted and can be a relatively important percentage of the overall power. In this case, it would be approximately 1 to 1.5% of the rated system power.

To solve this problem, the aux power supply circuit has been designed in such a way that, after a preset time from when the system is powered-up, it turns off, shorting the ON chip feedback input to ground. The delay time (during which the flyback circuit is running) may be set via the two resistors (R23 and R24). The nominal value of this delay, with the selected resistors, is approximately two seconds.

While this solves the problem of shutting off the flyback converter during normal converter operation, it poses a serious problem in the event of a fault. In this case, the dsPIC DSC shuts down the PWM controlling the LLC converter, the output voltage drops to zero and, consequently, the dsPIC DSC is not powered any more. The system shuts down (completely) but would not be capable to start again.

To solve this problem some kind of feedback from the dsPIC DSC device is needed. The dsPIC DSC must essentially "communicate" to the auxiliary power supply circuit that it is going to shut down the LLC converter. The AUX signal is used for this. In the event of a fault, while managing the fault itself, the dsPIC DSC drives high the AUX pin. This signal, crossing the isolation barrier via an optocoupler, restarts the flyback controller operation, discharging capacitor C24.

As a result, the dsPIC DSC is powered and active even if the LLC converter, for any reason, cannot be started again. One important possible advantage from this is that the dsPIC DSC can, for example, communicate the fault condition and the impossibility of restoring the converter functionality to the outside world.

Auxiliary Power Supply – Synchronous Buck Converter

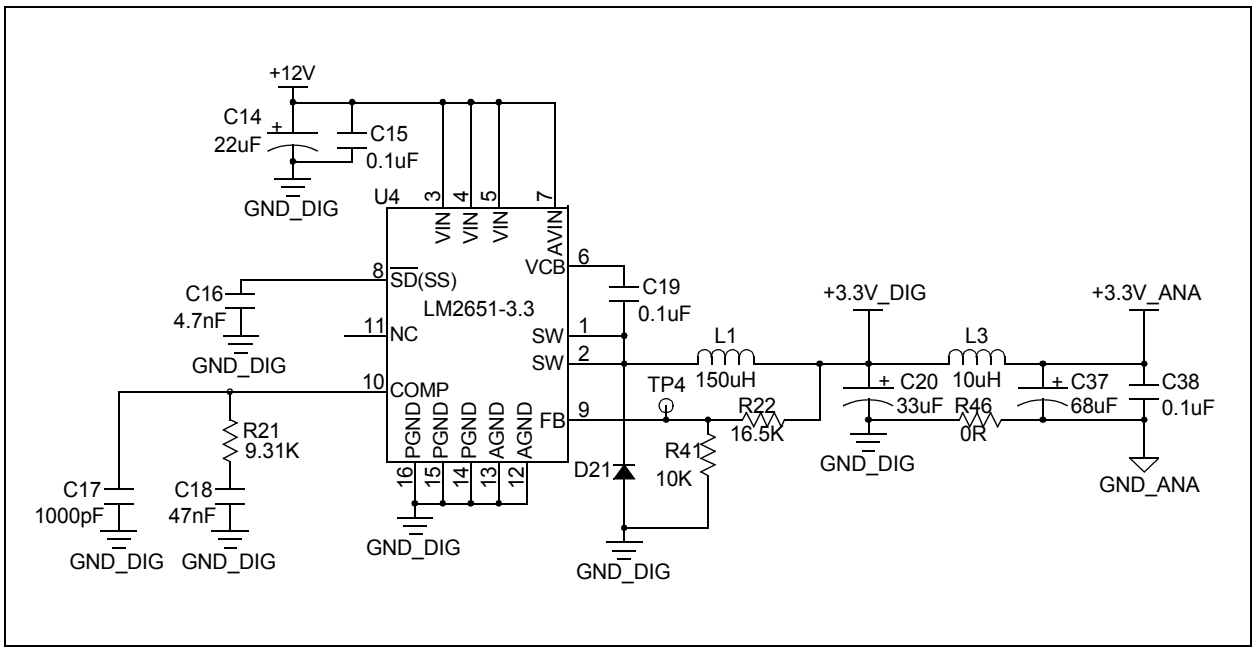
Referring to Figure 53, this circuit is intended to supply the dsPIC DSC with a 3.3V DC voltage, derived from the 12V input (either from the flyback or the main LLC converter). The LM2651 device from National Semiconductor™ has been selected because of its high efficiency. The measured efficiency is approximately 89% at 75% of the nominal current. The switching frequency is 300 kHz, which allows the use of small passive components. The circuit design is pretty straight forward, since only a few components must be added.

Some attention must be paid to the design of the compensation circuit. In fact, the chip presents an open loop transfer function having two poles: one (f_{p1}) at low frequency, the second one (f_{p2}) at a high frequency and one zero (f_z) in between. The compensation network, consisting in R21, C17 and C18, connected to the COMP pin of the chip, adds two poles (f_{cp1}, f_{cp2}) and one zero (f_{cz}) so that:

- the first compensation pole (f_{cp1}) is at very low frequency, about 1/10 of the low frequency chip pole (f_{cp2})
- the compensation zero has the same frequency of the first chip pole (f_{p1})
- the second compensation pole (f_{cp2}) is at the same frequency of the chip zero (f_z).

The overall result is a loop transfer function with a -20 dB per decade from very low to very high frequencies. Such a function guarantees a stable circuit.

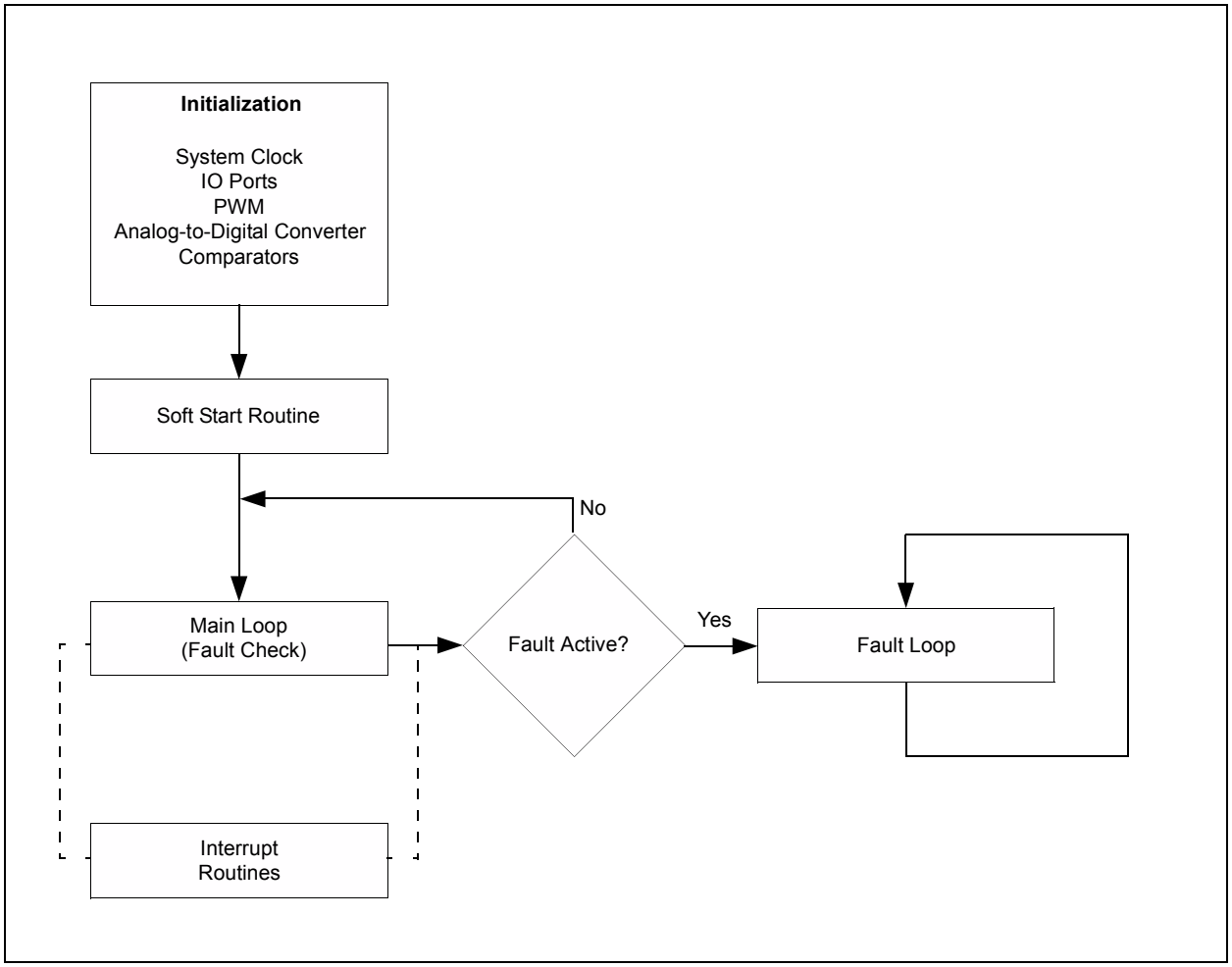
FIGURE 53: AUXILIARY HIGH-EFFICIENCY BUCK REGULATOR



REFERENCE DESIGN FIRMWARE OVERVIEW

Figure 54 introduces the fundamental firmware block diagram of the LLC Converter Reference Design.

FIGURE 54: HIGH-LEVEL FIRMWARE BLOCK DIAGRAM



Initialization

In this section of the code, all of the main system operations and peripherals are initialized.

Since the LLC half-bridge converter is frequency controlled, an external oscillator is used to provide the clock to the system in order to obtain a small tolerance over the entire operating temperature range. The external 7.37 MHz crystal is supplied to the internal oscillator circuit; from this the system PLL and the auxiliary PLL clocks are derived for the system and the PWM and ADC peripherals respectively. The auxiliary clock has an internal 16x PLL, which produces a clock frequency of 118 MHz for the PWM and ADC Peripherals. The system clock PLL provides a clock frequency of 40 MHz.

The LLC Reference Design uses two PWM channels. One channel drives the primary half-bridge MOSFETs, and the other channel the secondary synchronous rectifier MOSFETs.

The Table 6 summarizes the initial modes of operation of the two PWM channels.

TABLE 6: INITIAL PWM MODES

Operating Mode	Primary PWM Push-pull	Secondary PWM Push-pull
Dead Time	Disabled (included into the duty cycle value)	Disabled (included into the duty cycle value)
Duty	1/2 the period – dead time value	1/2 the period – dead time value
ADC Trigger	Generated every fourth PWM period	Generated every fourth PWM period

The ADC channels are used as summarized by Table 7.

TABLE 7: ADC CHANNELS

ADC Channel	Signal	Comment
AN0	IOUT_FB	The current transformer outputs, connected in series to the main transformer, are filtered and amplified by U2.
AN1	VOUT_FB	A resistor divider network is used to sense the output voltage.
AN2	VIN_FB	It is measured at the secondary, using a high voltage capacitor to cross the isolation barrier.
AN3	TEMP_FB	Temperature is detected using the MCHP9700 (U8) temperature sensor. The sensor is located close to the output synch MOSFETs.

Comparator 1 shares the same input pin as ADC channel 0. This means that the output current is also monitored with the comparator to determine overcurrent events.

Before starting the system operation, a check is performed on the input voltage to check that its value is within the specified range.

Soft-Start Routine

The unit, when powered up, operates at a at very high frequency (around 300 kHz). The duty cycle is manually controlled to ramp-up the converter's output voltage from 0V to approximately 10V, depending on the input voltage. From this point on, the duty is fixed at 50% minus dead time and the frequency is instead reduced down to the nominal value (205 kHz @ 400V input).

Interrupts Management

A number of interrupts are serviced:

- ADC Pair 0 interrupt

  The output voltage is acquired and is passed to the routine that implements the PI control. The output of the PI processing is the new frequency value, or, more precisely, is the value of the PTPER register. During normal operation the updated frequency value is checked to be within specified limits.

  The output synchronous rectifier PWM channel is also updated, keeping into consideration the fact that the operating frequency is higher or lower than the resonant frequency.

  During soft start, the system is operated at fixed frequency, and the PI compensator is disabled; however, the output voltage is still monitored by the ADC. The tank current will also be measured in this ADC interrupt.

- ADC Pair 1 interrupt

  This interrupt is used to acquire the input voltage and for temperature sensing.

- Timer 1 interrupt

  This interrupt is used to compute delays. The timer interrupt occurs every 100 µs.

- Comparator 1 interrupt

  This interrupt is used to detect overcurrent events (faults).

Fault Management

A number of different signals originating faults are considered. One of the main problems in managing faults is to avoid stopping the operation of the unit immediately, as soon as a fault signal is received. The reason for this is to avoid having a fast response to possible glitches and noise.

Fault condition is continuously tested in the main loop. In effect, this is the only operation which is performed (in background) by the main code.

Each fault signal is tested a number of times, a counter is incremented at each cycle if the fault is always present and only when the counter has reached some specific value, the firmware considers that a real fault condition has occurred. See Table 8 for details. As soon as the system enters a fault status, the fault LED will be switched on and off a number of times that corresponds to the fault status; this provides visual representation of which fault occurred.

TABLE 8: FAULT STATUS

Fault Event	Counter Value to Start Fault Status	LED Number of ON/OFF Cycles
Input Undervoltage	250	1
Input Overvoltage	250	1
Overcurrent (Comparator)	—	2
Overcurrent (ADC)	250	2
Output Overvoltage	250	3
Output Undervoltage	250	4
Temperature	250	5
Soft-start	—	6

APPENDIX A: SOURCE CODE

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APPENDIX B: ELECTRICAL TEST RESULTS AND OPERATIONAL WAVEFORMS

This appendix provides information on the test results for the 200W LLC Resonant Converter Reference Design, as well as a few operational waveforms.

The following equipment was used to test the LLC Resonant Converter:

- DC source > 450V, 3A
- Electronic DC load > 12V, 20A
- Four-channel oscilloscope (100 MHz or higher)
- High-bandwidth current probes and differential probes
- 6 half digit multimeters
- Efficiency boards (only for measuring efficiency)

B.1 SOFT-START AND OVERSHOOT

The LLC Resonant Converter implements a duty cycle/frequency controlled soft-start routine to ramp the output voltage up to 12V, thereby eliminating in-rush current and output voltage overshoot at start-up.

At start-up, the switching frequency is set to 300 kHz to provide minimal gain from the resonant tank. The duty cycle is manually controlled to bring the output voltage up to approximately 10V depending on the input voltage. Afterward, the switching frequency is reduced until the output voltage is close to the desired reference voltage (12V). From this point on, the frequency is controlled using a PI compensator; however, in order to eliminate any overshoot the integral error is calculated providing history to the control loop.

Figure B-1 and Figure B-2 demonstrate the converter's soft-start with and without load.

FIGURE B-1: NO LOAD SOFT-START, INPUT VOLTAGE: ~400 VDC

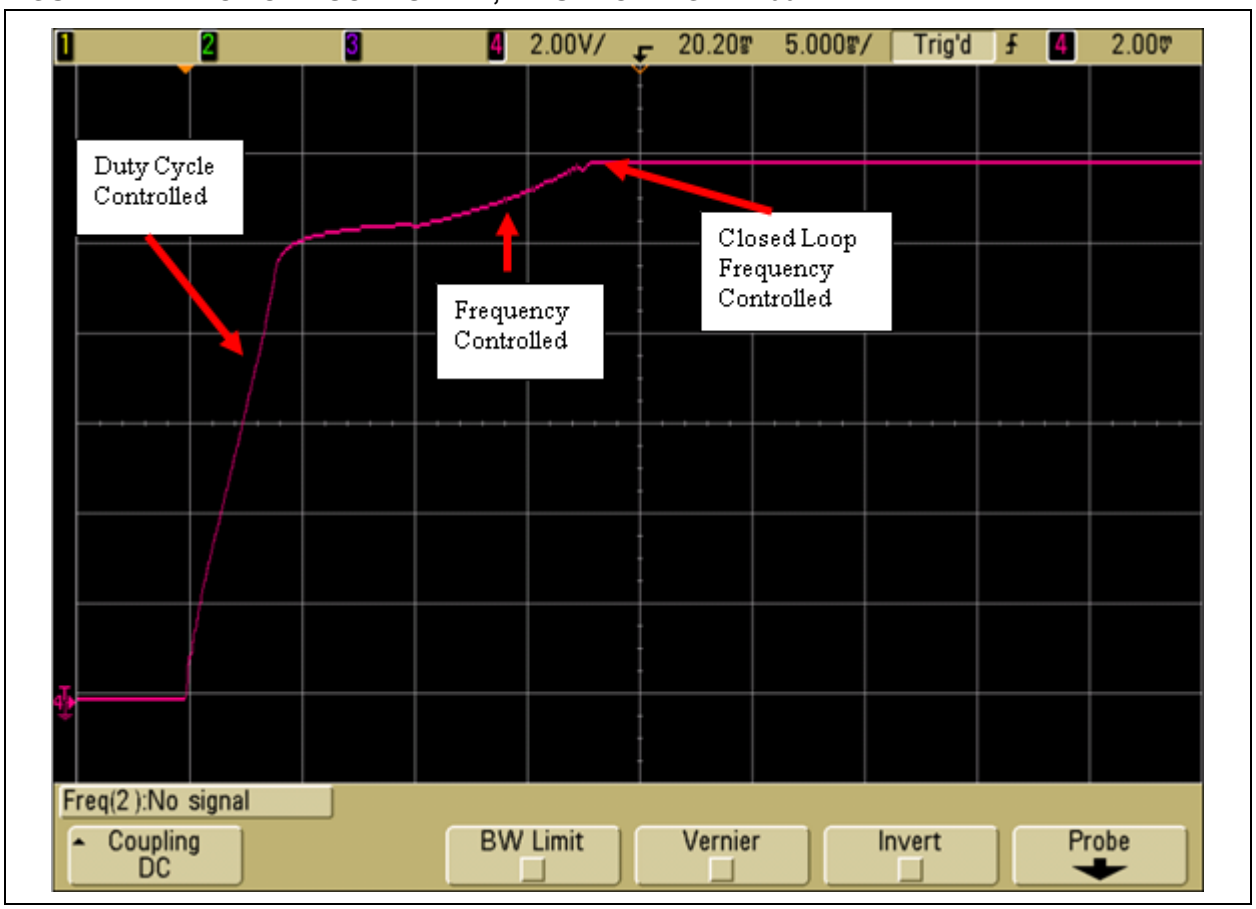
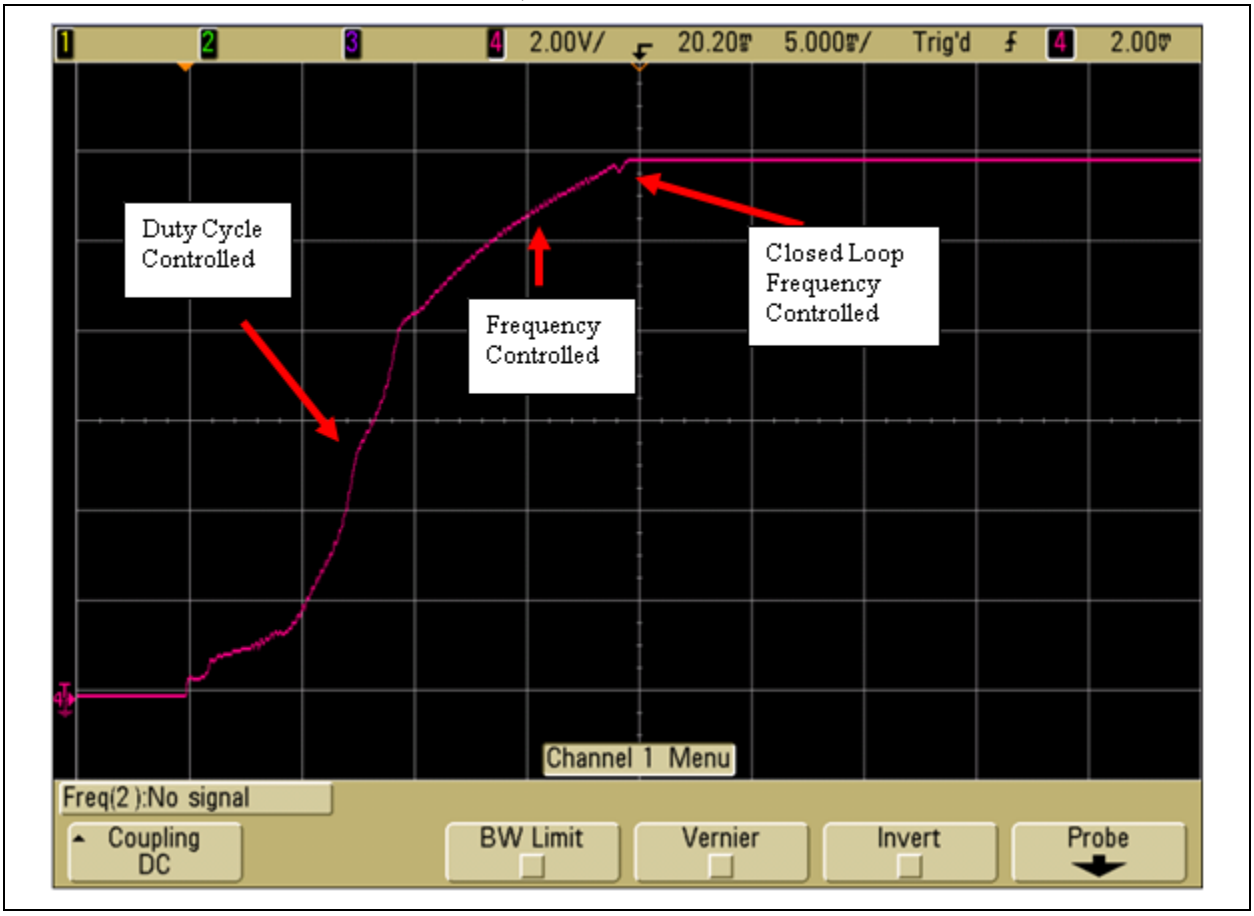


FIGURE B-2: FULL LOAD SOFT-START, INPUT VOLTAGE: ~400 VDC

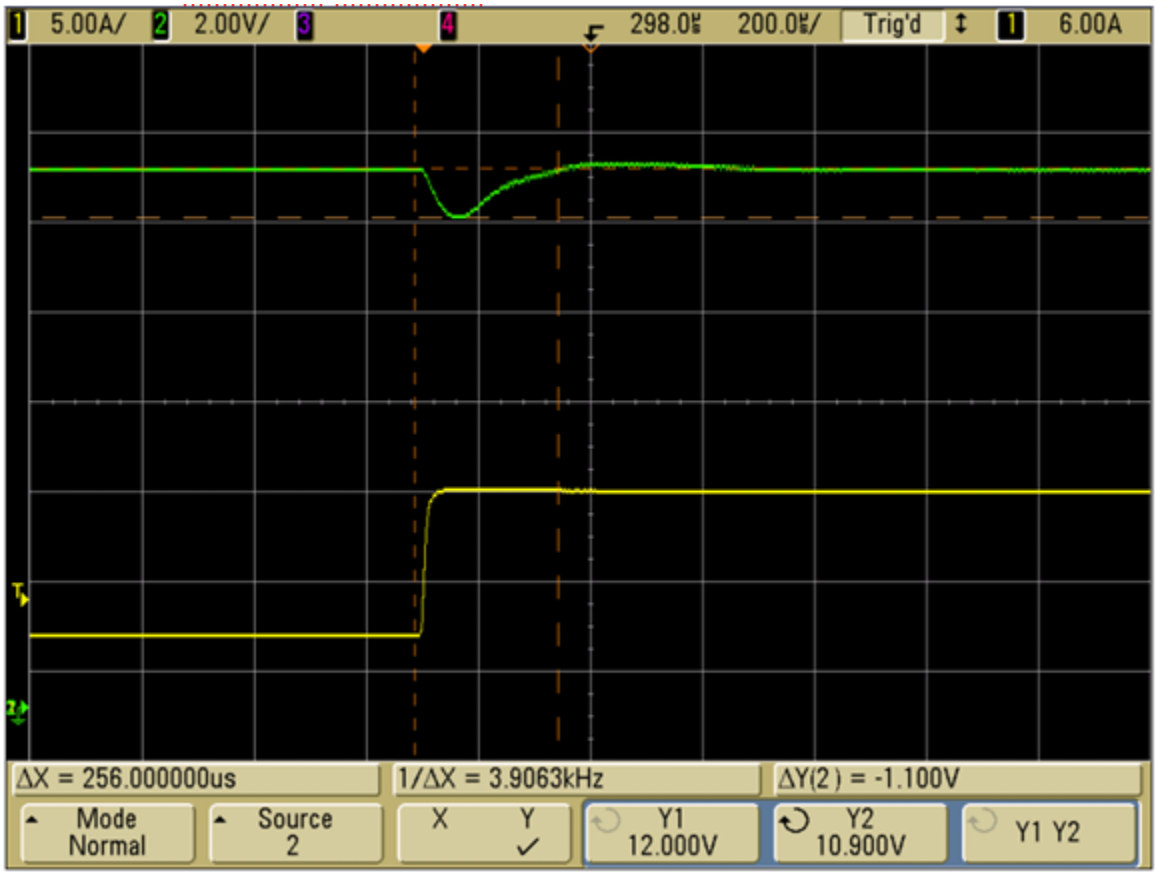


B.2 DYNAMIC LOAD RESPONSE

When measuring the dynamic load response the undershoot/overshoot voltage and settling time of the output voltage are captured when a load step change is performed on the output.

Figure B-3 and Figure B-4 demonstrate the dynamic load response of the system with a load step change of 25%-75% and 75%-25% with a slew rate of 1A/µs.

FIGURE B-3: TRANSIENT RESPONSE 25%-75% (4A-12A), INPUT VOLTAGE: ~400 VDC

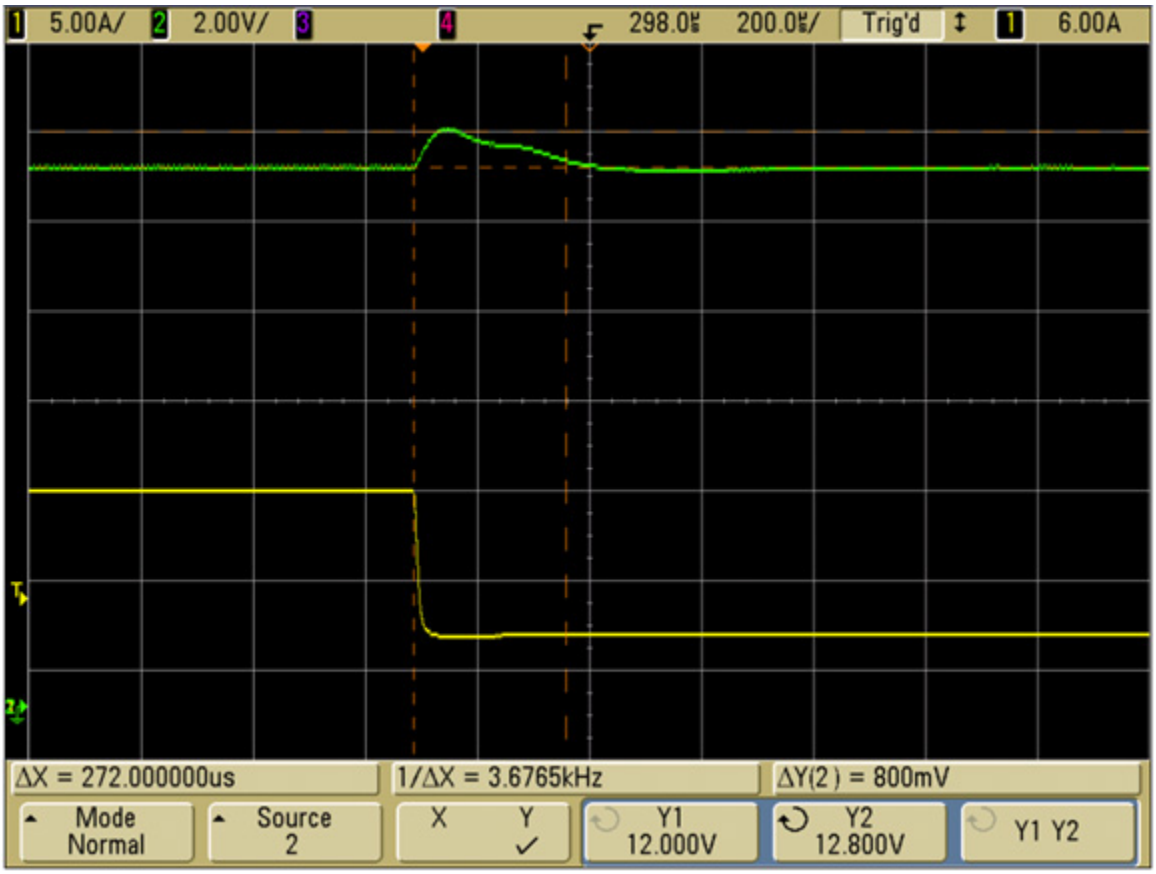


Legend:

Green = Output voltage

Yellow = Output load current

FIGURE B-4: TRANSIENT RESPONSE 75%-25% (12A-4A), INPUT VOLTAGE: ~400 VDC



Legend:

Green = Output voltage

Yellow = Output load current

B.3 OUTPUT VOLTAGE RIPPLE

Output voltage ripple is measured across the output capacitors with the shortest possible probe ground lead. Figure B-5 and Figure B-6 show the output voltage ripple of the LLC Resonant Converter.

FIGURE B-5: OUTPUT VOLTAGE RIPPLE, I_{OUT}: 17A, INPUT VOLTAGE: ~400 V_{DC}

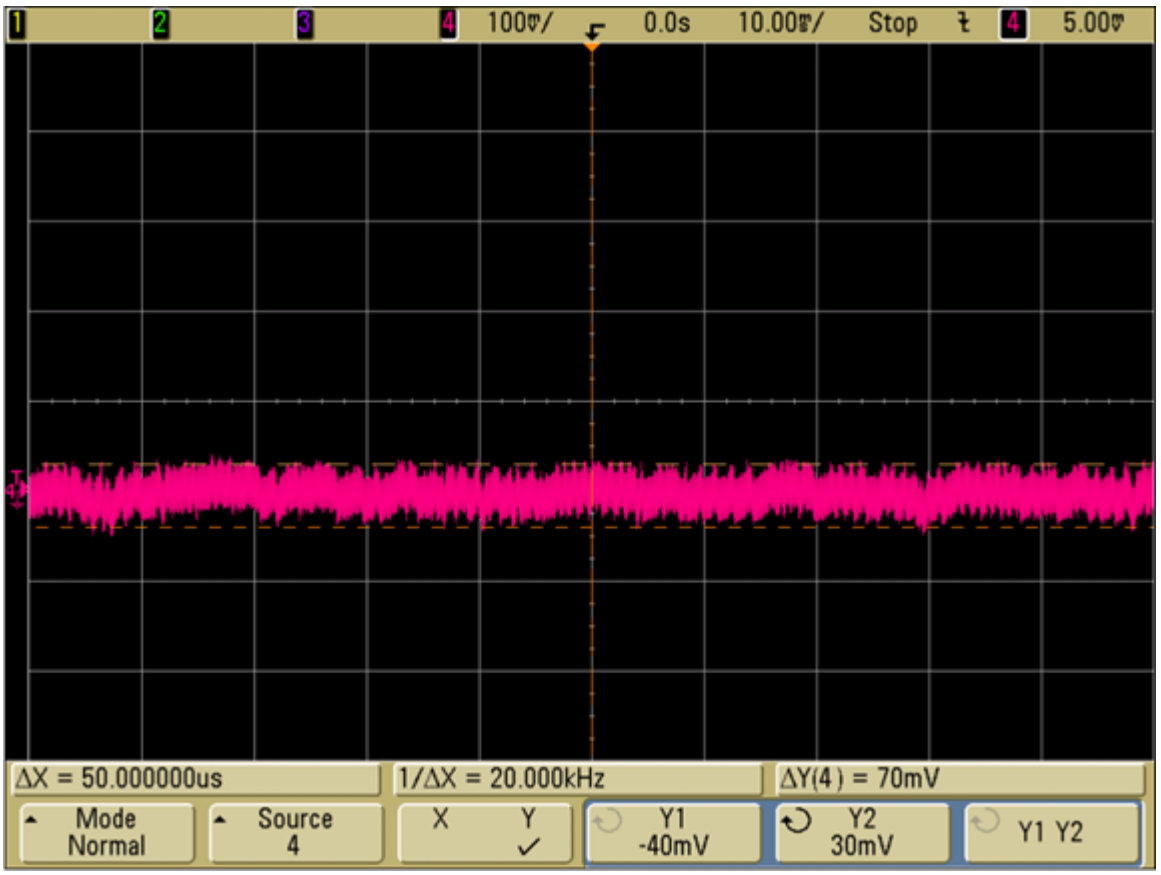
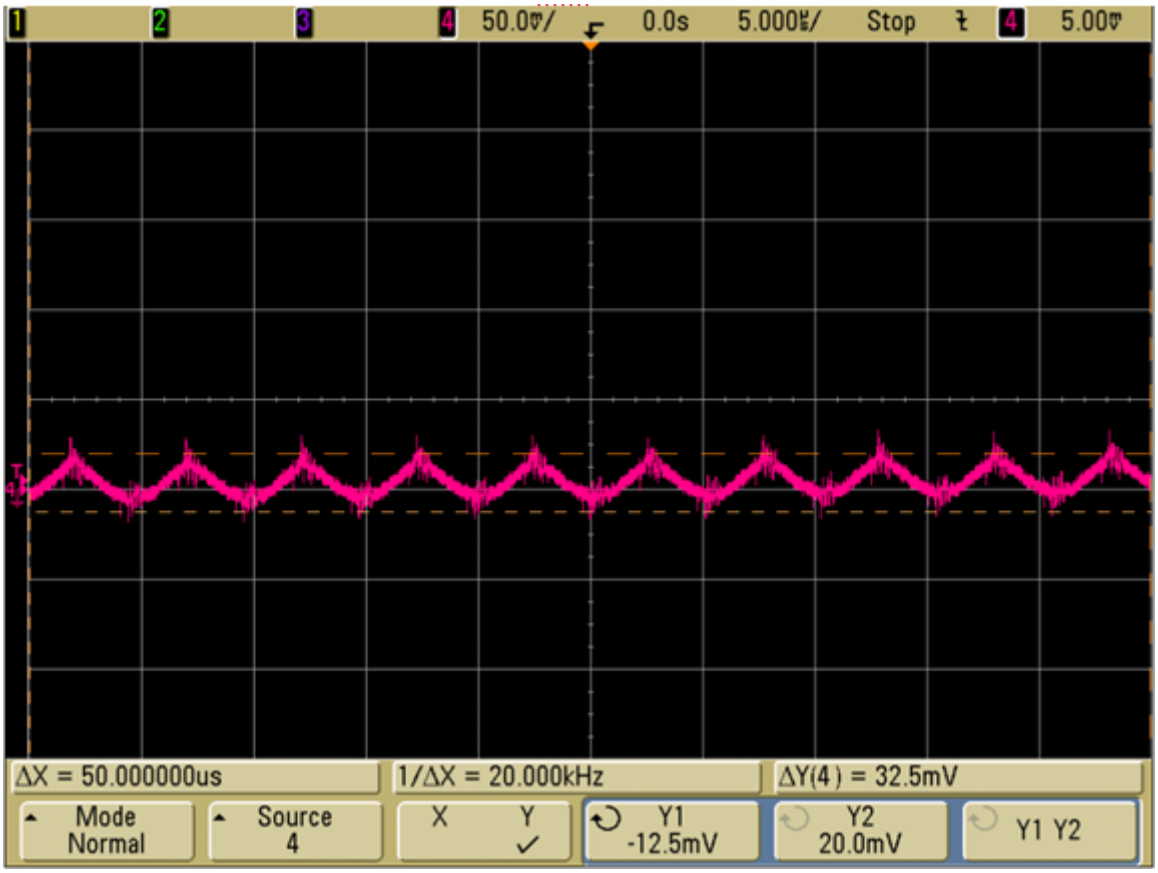


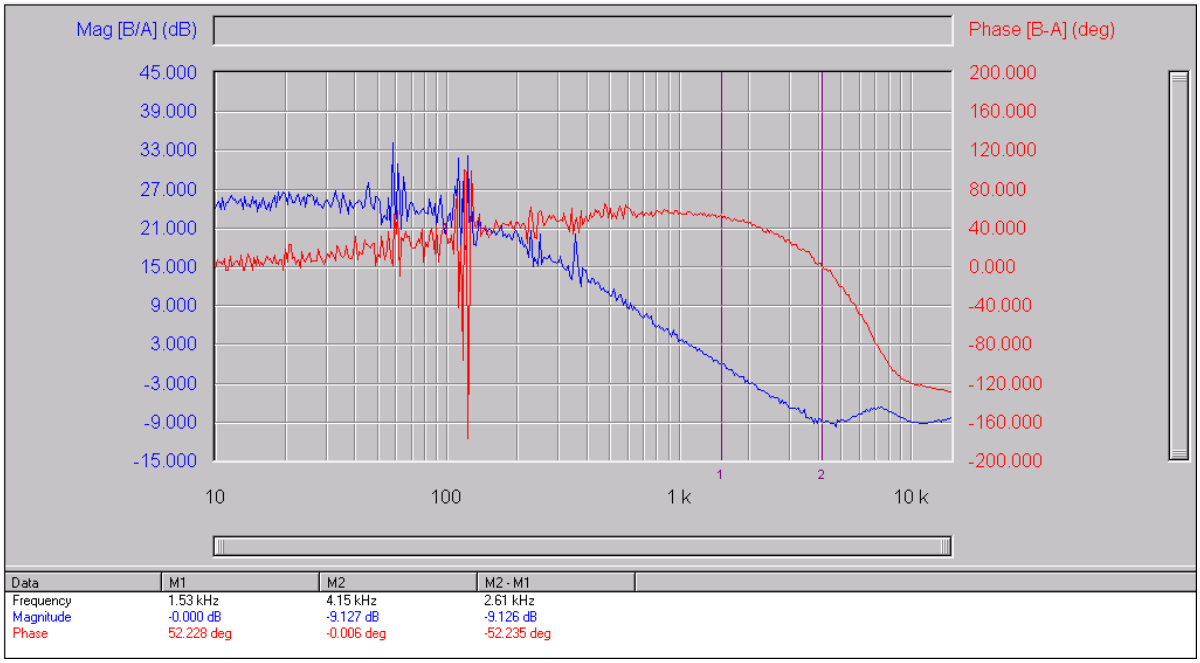
FIGURE B-6: OUTPUT VOLTAGE RIPPLE, I_{OUT}: 17A, INPUT VOLTAGE: ~400 V_{DC}



B.4 Phase and Gain Margin

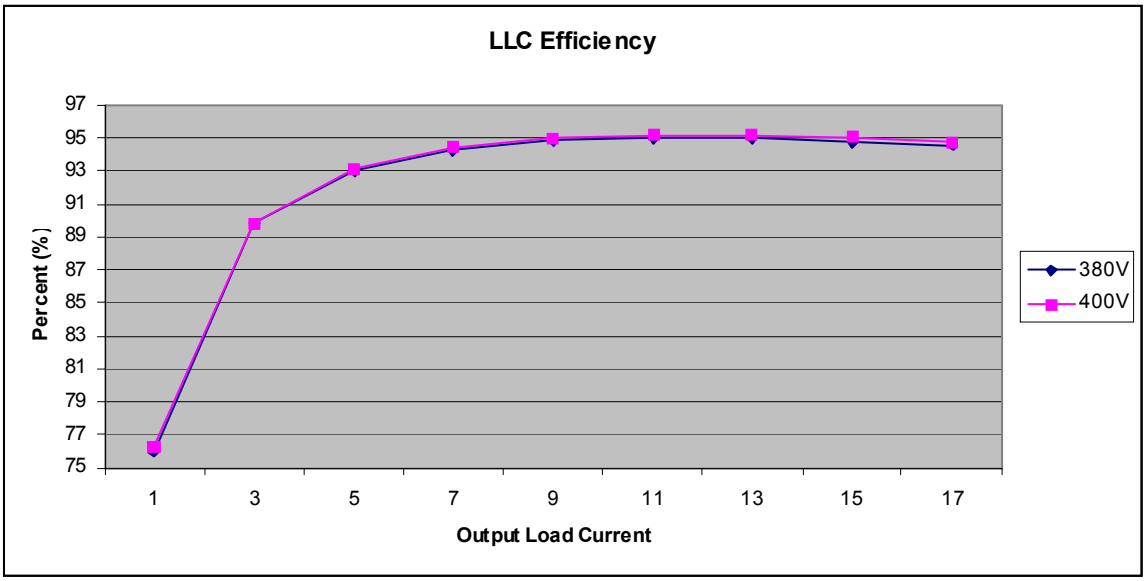
Figure B-7 shows the closed loop performance of the LLC Resonant Converter at nominal input voltage (400Vdc) and half load.

FIGURE B-7: PHASE AND GAIN MARGIN (VIN: 400 VDC, IOUT: 8.5A)



B.5 EFFICIENCY

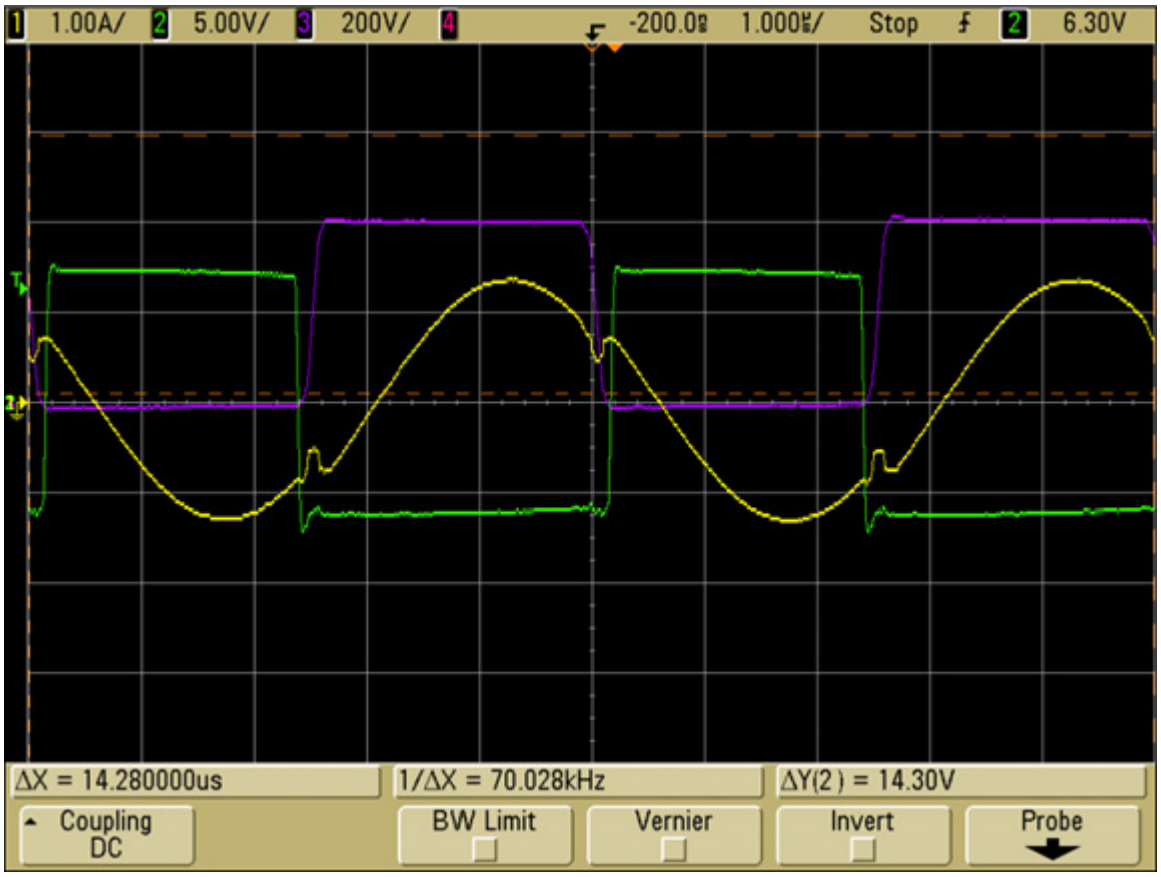
FIGURE B-8: LLC EFFICIENCY @ 380 VDC AND 400 VDC



B.6 Zero Voltage Switching

Due to the phase shift between the resonant tank current and voltage the half-bridge MOSFETs are able to switch without any turn on losses. Figure B-9 and Figure B-10 demonstrate zero voltage switching on the low-side MOSFET.

FIGURE B-9: ZVS, IOUT: 8.5A INPUT VOLTAGE: ~400 VDC



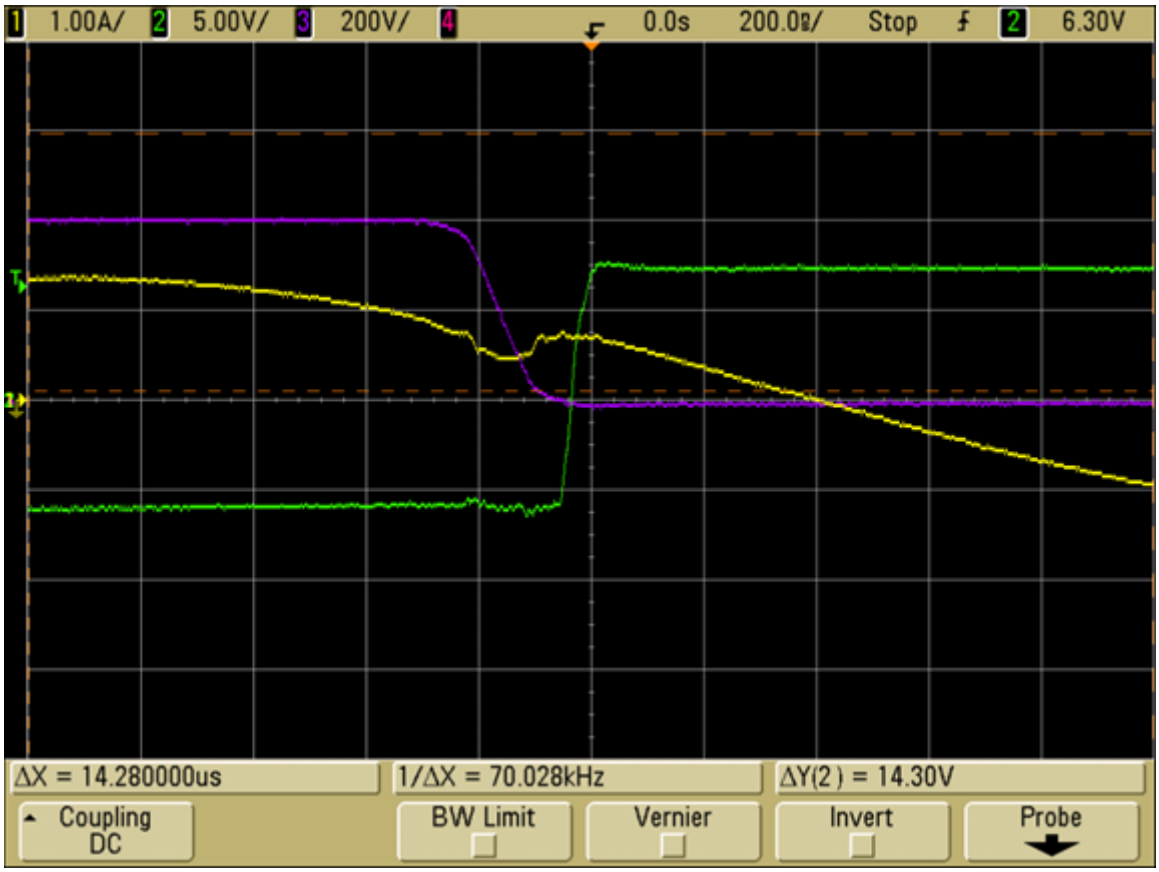
Legend:

Green = MOSFET gate-to-source

Violet = MOSFET drain-to-source

Yellow = Resonant tank current

FIGURE B-10: ZVS, I_{OUT}: 8.5A, INPUT VOLTAGE: ~400 V_{DC}



Legend:

Green = MOSFET gate-to-source

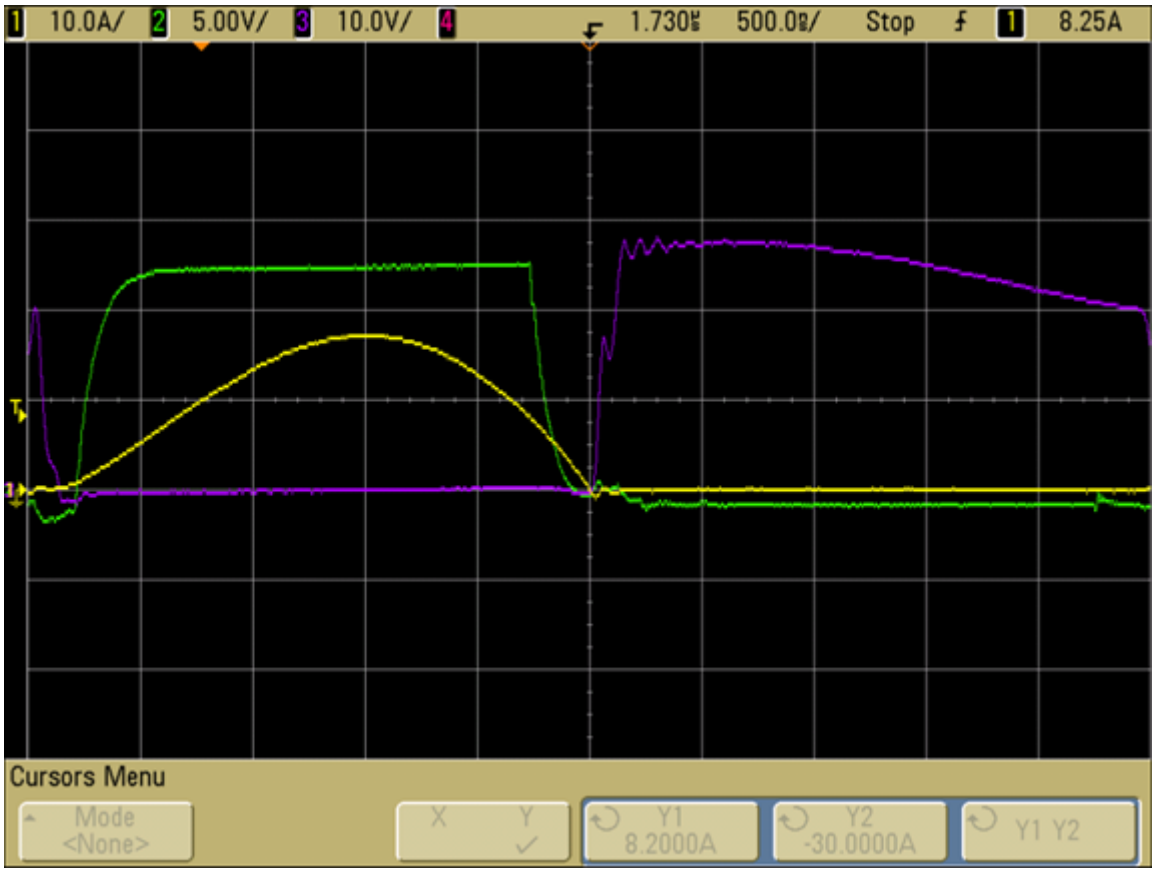
Violet = MOSFET drain-to-source

Yellow = Resonant tank current

B.7 Zero Current Switching

Figure B-11 demonstrates zero current switching on the secondary rectifier. As the MOSFET current becomes zero the MOSFETs Drain-to-Source Voltage begins to rise. This eliminates any turn-off loses.

FIGURE B-11: ZCS, IOUT: 8.5A, INPUT VOLTAGE: ~400 VDC



Legend:

Green = MOSFET gate-to-source

Violet = MOSFET drain-to-source

Yellow = MOSFET current

B.8 Resonant Tank Current

Figure B-12 and Figure B-13 show the resonant tank current at no load as well as full load near the resonant frequency.

FIGURE B-12: RESONANT TANK CURRENT: NO LOAD

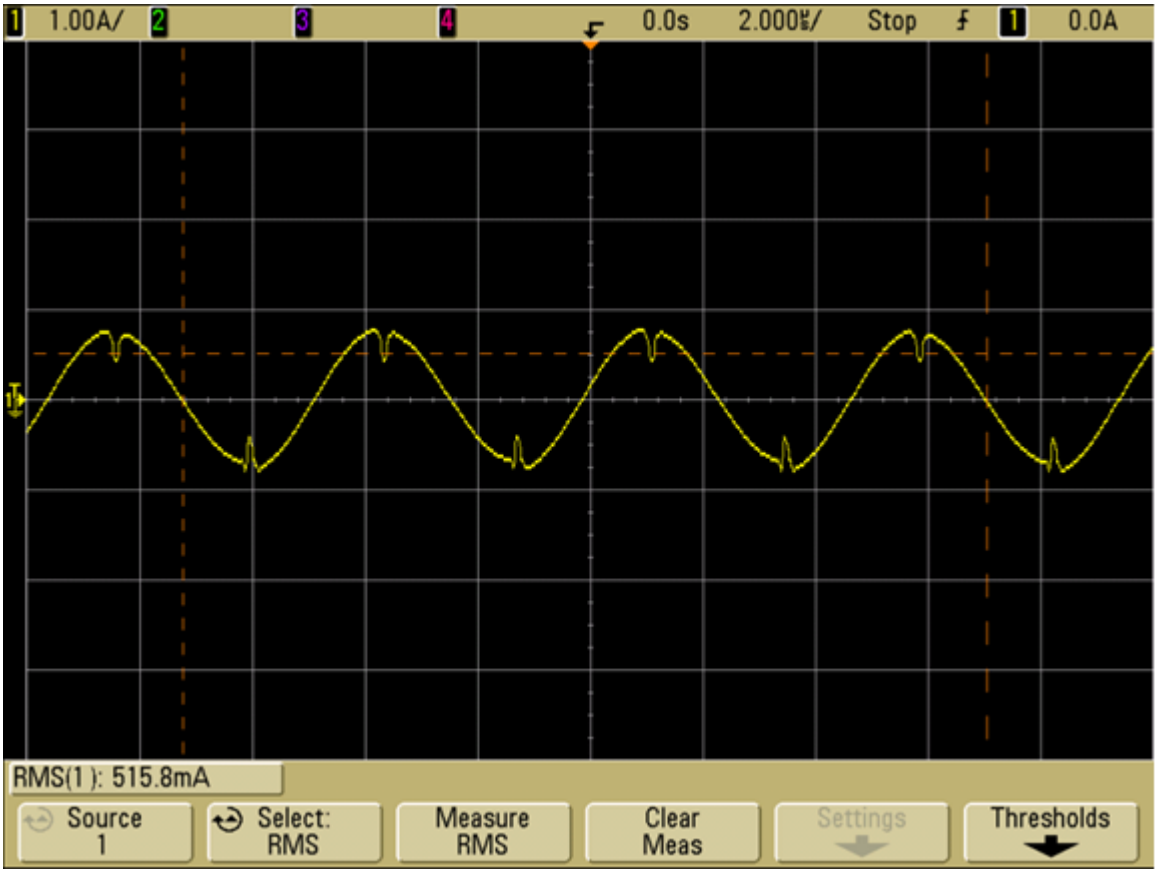
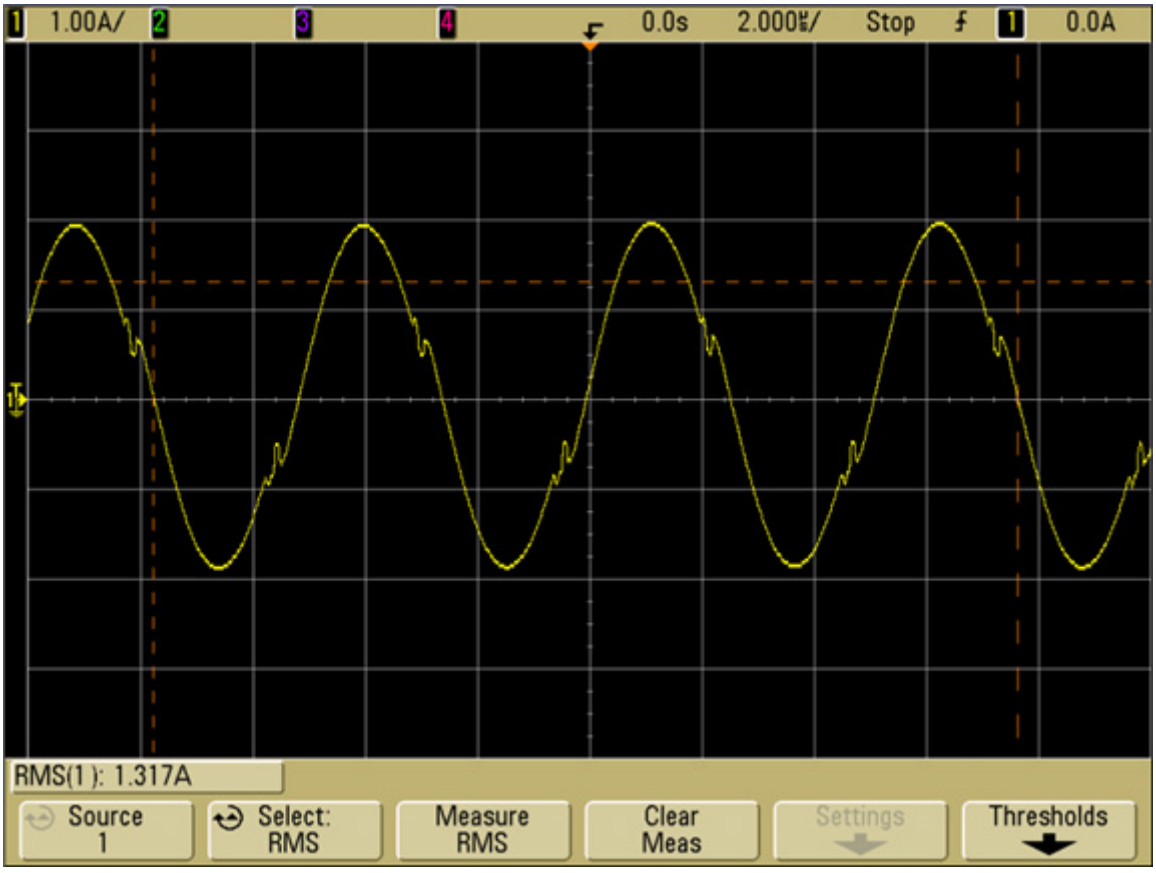


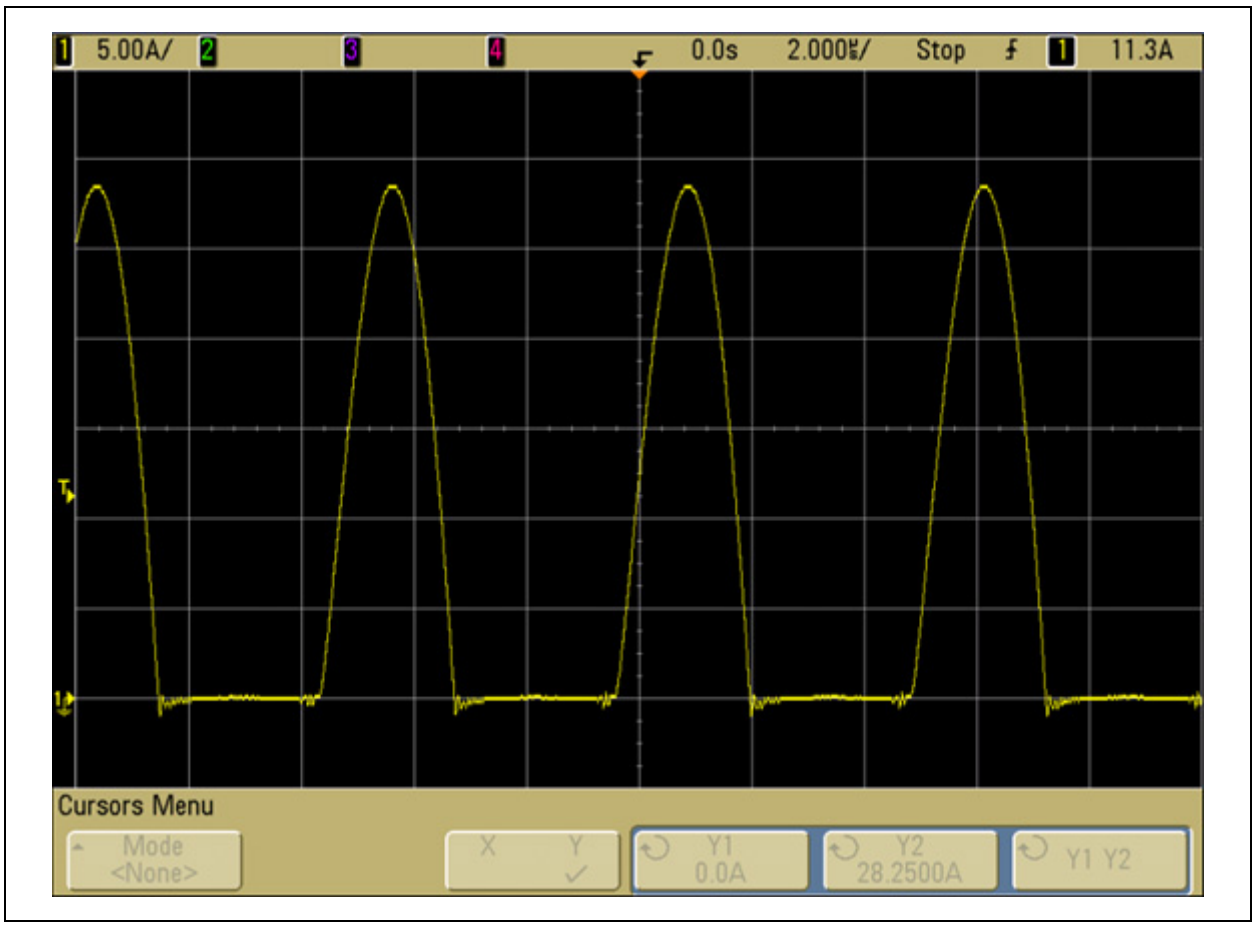
FIGURE B-13: RESONANT TANK CURRENT IOUT: 17A



B.9 Secondary Currents

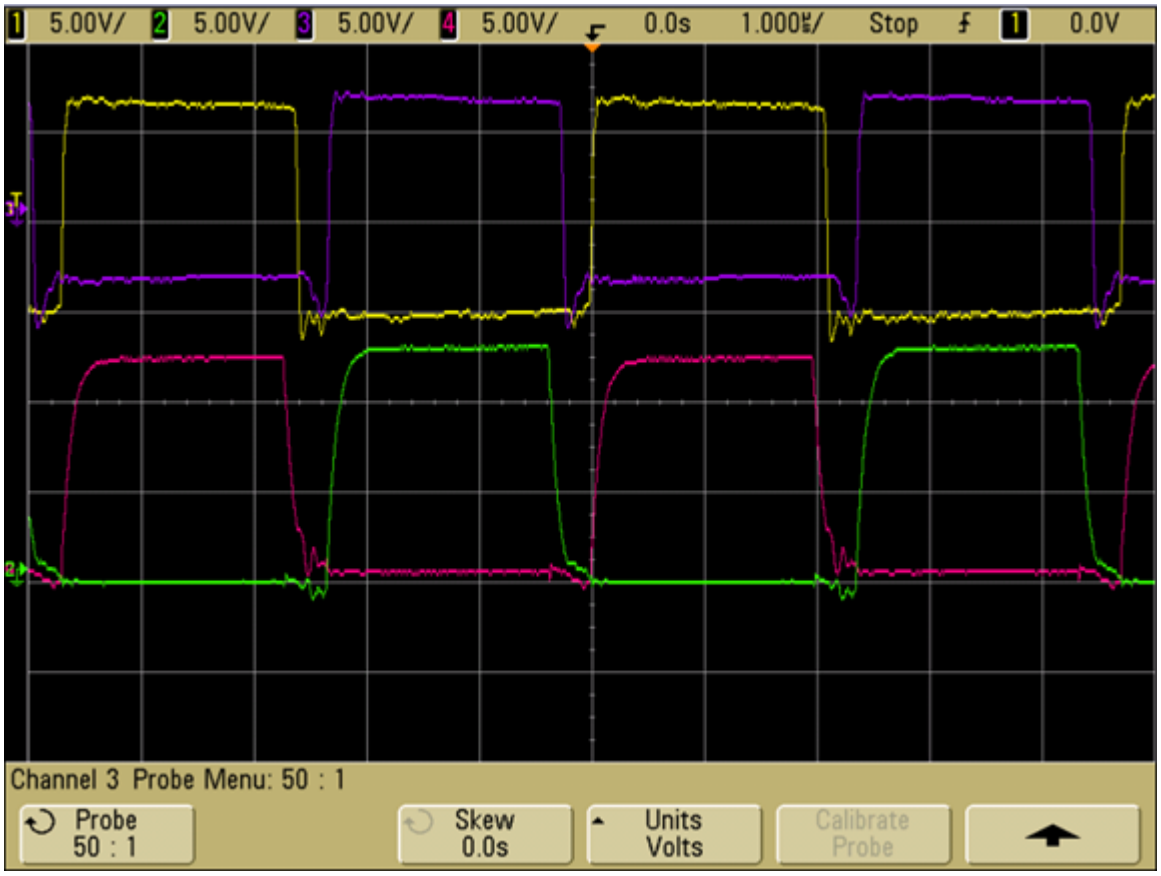
Figure B-14 shows the secondary MOSFET current at full load.

FIGURE B-14: SECONDARY MOSFET CURRENT IOUT: 17A



B.10 MOSFET Gate Signals

FIGURE B-15: PWM GATE DRIVE WAVEFORMS

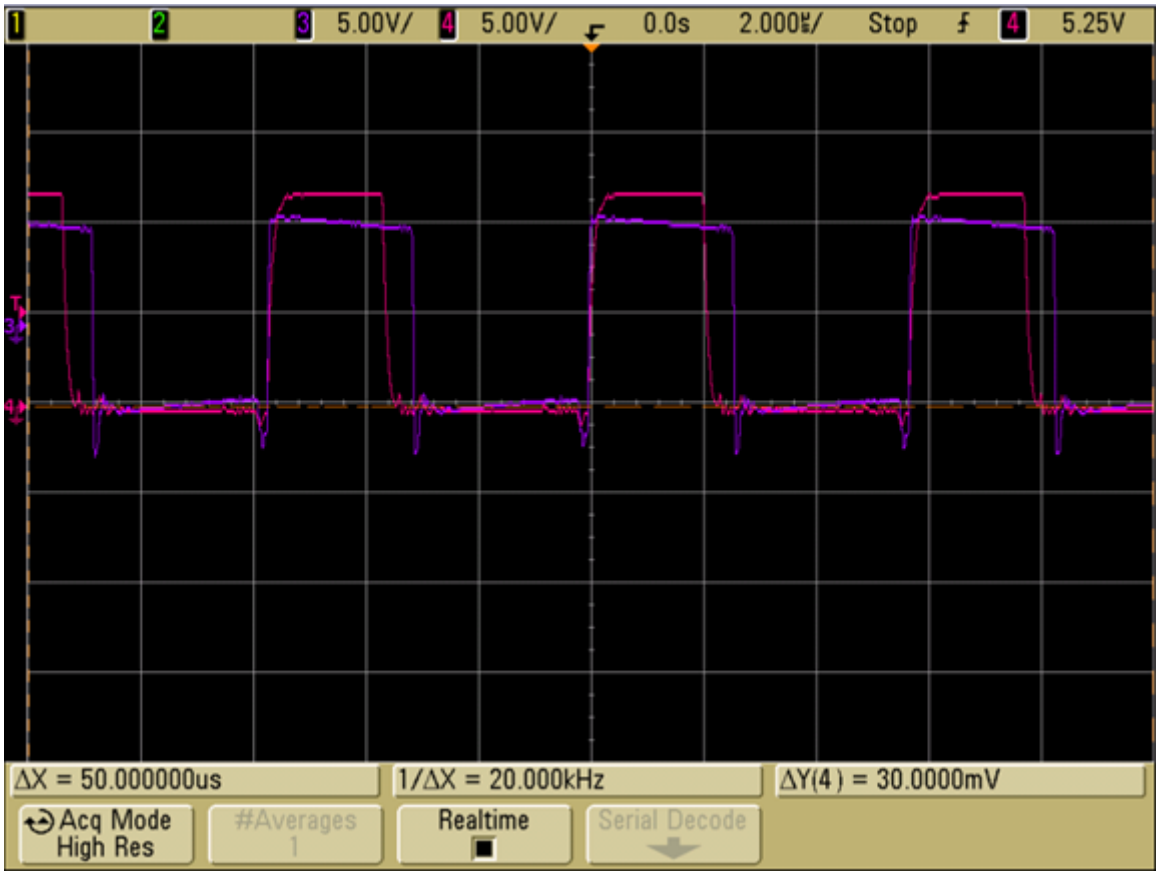


Legend:

Green and Red = Synchronous MOSFETs

Violet and Yellow = Half-bridge MOSFETs

FIGURE B-16: PWM GATE DRIVE WAVEFORMS BELOW RESONANCE



Legend:

Red = Synchronous MOSFET

Violet = Half-bridge MOSFET

APPENDIX C: LLC RESONANT CONVERTER CONTROL SYSTEM DESIGN

C.1 System Modeling

It is desirable to model and simulate any power converter in order to optimize its performance in advance. This approach is useful in achieving the desired performance before testing the design on actual hardware.

System modeling involves the following process:

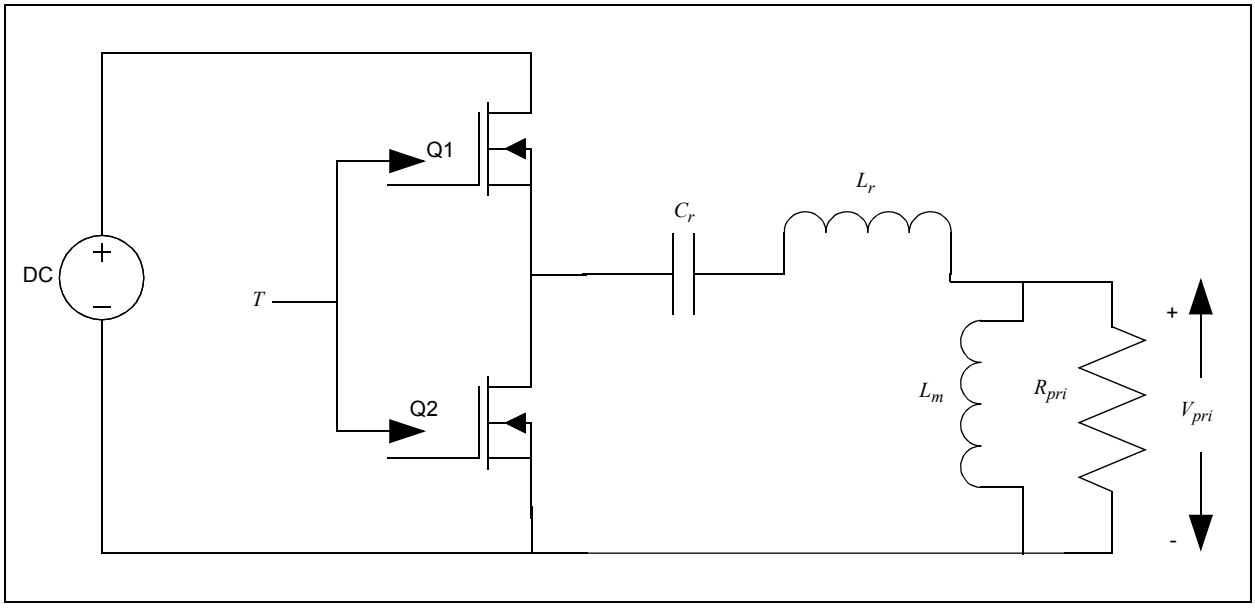
- Control loop coefficients are generated in MATLAB®, based on key system parameters and using an `.m` file.
- A graphical model of the system hardware and the control system is created using a Simulink® model (`.mdl`) file. The coefficients generated from the `.m` file are used in this Simulink model file.
- The model of the hardware and control system is then simulated at various operating points to ensure that the desired performance is achieved.
- The model of the control system is then implemented in software on the dsPIC DSC and the performance is verified on real hardware.

C.2 Principle of Operation of Half-Bridge LLC Resonant Converter

The LLC resonant converter operates on a fixed duty cycle, variable switching frequency to maintain a constant output voltage for varying load and line conditions.

The equivalent circuit of the LLC resonant converter is shown in Figure C-1. The operation of the converter is based on a potential divider impedance network. The output voltage is controlled by varying the voltage applied across the magnetizing inductance. This is achieved by changing the relative impedance of the LLC network elements using variable switching frequency. The output voltage can therefore be controlled using the switching frequency of the half-bridge.

FIGURE C-1: EQUIVALENT CIRCUIT OF LLC CONVERTER



C.3 Analysis

The LLC resonant converter is a highly nonlinear system and difficult to analyze using an analytical formula. Since it is a DC/DC converter, operating point analysis can be performed.

In a DC/DC converter, if the input and output voltages are nearly constant quantities under changing loads, properties of the system do not change significantly. Therefore, small signal analysis and linearization can be performed on the system.

A small change in input voltage, reference or load only causes a linearly dependent or proportional change in the switching period. Mathematically we approximate all nonlinear terms with a 1-term Taylor Series Approximation about an operating point.

Consider the following example: If x is an input (independent variable) and y is an output (dependent variable) with the following relationship:

$y = x\text{^}2$

The Taylor Series Approximation about the nominal operating point (x_0, y_0) will be:

$dy = 2x_0 \, .dx$

The relation dy/dx is the dynamic slope and can be used to study the system behavior. This method can be generalized to any number of variables with the use of partial derivatives.

The goal is to generate correct voltage (V_x) at the output of the rectifier and input to the LC filter, by varying the switching period (T) of the half-bridge. For an LLC Resonant Converter, the relation between V_x and T is nonlinear and therefore, the operating point approach is used.

The desired voltage V_x is obtained by varying the impedances of the various elements in the circuit shown in Figure C-1. The impedances are given by X_c, X_r and X_m and are functions of the half-bridge switching frequency. The voltage that gets applied to the magnetizing inductance is given in Equation C-1.

EQUATION C-1:

$$V_{pri} = \left(\frac{X_m}{(X_m + X_r - X_c)}\right) \cdot V_{in}$$

where, V_{in} is the input voltage

V_x appears across the output of the LC filter after getting scaled by the turns ratio, as shown in Equation C-2.

EQUATION C-2:

$$V_x = \frac{V_{pri}}{Turnsratio}$$

The voltage V_{pri} is determined by the gain of the LLC circuit. This gain is shown in Equation C-3.

EQUATION C-3:

$$G_p = \frac{V_{pri}}{V_{in}} = \frac{X_m}{(X_m + X_r + X_c)}$$

Where:

G_p = Gain of the LLC circuit.

$X_m = j2\pi f_s L_m$ = impedance of the magnetizing inductance.

$X_r = j2\pi f_s L_r$ = impedance of the magnetizing inductance.

$X_c = \frac{1}{j2\pi f_s C_r}$ = impedance of the series capacitor.

By modifying the switching frequency f_S, the gain of the LLC circuit is changed and therefore the output voltage can be controlled with varying load and input voltage.

The LLC circuit can be operated at any of the three operating regions:

- At resonance (G_p = 1)
- Below resonance (G_p > 1)
- Above resonance (G_p < 1)

For modeling of the system, we need to determine a relationship between the gain of the LLC circuit and the switching frequency. Due to the nonlinear nature of the gain equation, we perform operating point analysis about the nominal operating point, i.e. the resonant frequency. In order to perform operating point analysis, we define a new variable p at the resonant frequency f_r as shown in Equation C-4.

EQUATION C-4:

$$p = \frac{1}{G_p} = \frac{(X_m + X_r + X_c)}{X_m} = 1 + \frac{L_r}{L_m} - \left(\frac{1}{(4\pi^2 f_S^2 C_r L_m)}\right)$$

$$V_{pri} = \frac{V_{in}}{p}$$

As a result of the calculations in Equation C-4, V_{pri} is now expressed as shown in Equation C-5.

EQUATION C-5:

$$V_{pri} = \frac{V_{in}}{\left(1 + \frac{L_r}{L_m} - \frac{1}{(4\pi^2 f_S^2 C_r L_m)}\right)}$$

Differentiating both sides with respect to frequency, results in that of Equation C-6.

EQUATION C-6:

$$\delta V_{pri} = -\frac{V_{in}}{p^2} \cdot \left(\frac{1}{(2\pi^2 f_S^3 C_r L_m)}\right) \cdot \delta f_S$$

Where,
δ represents a small change in the variable.

δV_{pri} is the change in V_{pri} observed for a small change in frequency. Frequency is represented as a function of the switching period, as shown in Equation C-7.

EQUATION C-7:

$$f_S = \frac{1}{T_S}$$
$$\delta f_S = \frac{-1}{T_S{}^2} \bullet \delta T_S$$
$$= f_S{}^2 \delta T_S$$

Substituting the results of Equation C-7 into Equation C-6 is expressed in Equation C-8.

EQUATION C-8:

$$\delta V_{pri} = \left(\frac{V_{in}}{p^2 2\pi^2 f_S C_r L_m}\right) \cdot (\delta T_S)$$

As the change in frequency is assumed to be small, we can replace f_S in Equation C-8 to the nominal operating frequency (i.e., the resonant frequency f_r). The equation then changes to that of Equation C-9.

EQUATION C-9:

$$\delta V_{pri} = \left(\frac{V_{in}}{(p_0^2 2\pi^2 f_r C_r L_m)}\right) \cdot (\delta T_S)$$

where, p_0 is the inverse gain calculated at the resonant frequency

Now, the final period output is defined, as shown in Equation C-10.

EQUATION C-10:

$$T_S = T_{nom} + \delta T_S$$
$$= T_{nom} + \left(\frac{\delta V_{pri}}{V_{in}}\right) \cdot (p_0^2 2\pi^2 f_r C_r L_m)$$

In Equation C-10, the term, $(p_0{}^2 2\pi^2 f_r C_r L_m)$, is a constant, because the change in period is assumed to be small for the range of operation of the LLC converter. Therefore, we can replace this term with the constant, *voltagetotimefactor*, which is defined in Equation C-11.

EQUATION C-11:

$$voltagetotimefactor = p_0^2 2\pi^2 f_r C_r L_m$$

Also, δV_{pri} is the change in the V_{pri} for a corresponding change in period δT. Using Equation C-2, we can represent the change in voltage with respect to the output voltage, as shown in Equation C-12.

EQUATION C-12:

$$\delta V_{pri} = V_{pri} - V_{pri\_nom}$$
$$= (V_x - V_{x\_nom}) \cdot turnsratio$$

Substituting Equation C-11 and Equation C-12 in Equation C-10, we obtain the final expression for the desired switching period, as shown in Equation C-13.

EQUATION C-13:

$$T_S = T_{nom} + voltagetotimefactor \cdot (V_x - V_{x\_nom}) \cdot \frac{turnsratio}{V_{in}}$$

T_{nom} is known from the converter design, and *voltagetotimefactor* is a constant defined previously. The voltage V_x is the control voltage required to produce the desired output voltage. This voltage V_x is generated by the digital compensator for the LLC Converter. Therefore, Equation C-14 will produce the desired switching period based on the measured output voltage and input voltage.

A Proportional + Integral (PI) compensator is chosen for the LLC resonant converter. Use of a Derivative term is ruled out because the series parasitic resistance of the system acts as a natural damping factor, and swamps any effect of the derivative term.

Figure C-2 shows the block diagram of a generalized control system. In the LLC Converter, the output LC filter forms the plant for the system. The output LC filter, in combination with the PI compensator provides the characteristic equation for the closed loop system, shown in Equation C-14.

EQUATION C-14:

$$s^2LC + sRC + K_p + \frac{K_i}{s} = 0$$

Where:

L = output inductor

C = output capacitor

R = parasitic (lumped) series resistance of the circuit

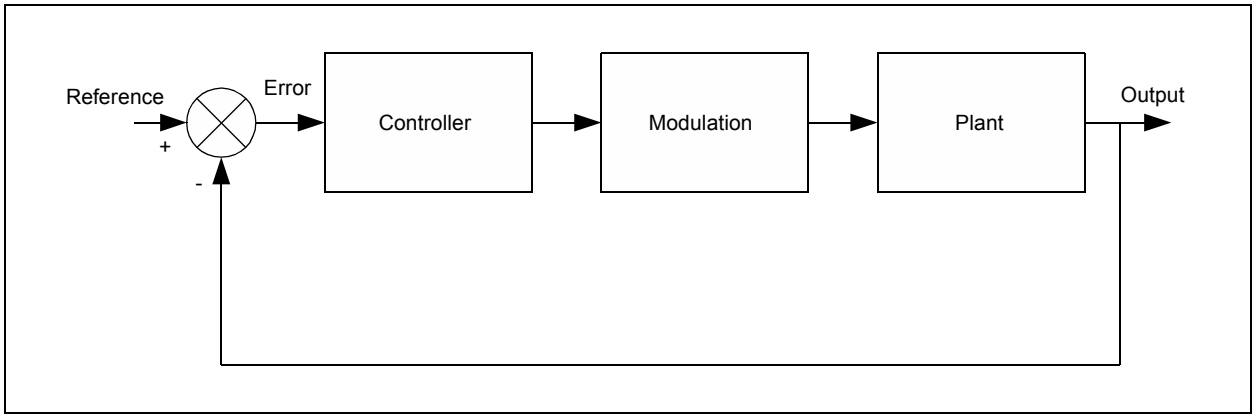
K_p = proportional gain of the compensator

K_i = Integral gain of the compensator

The roots of the characteristic equation are chosen to be -1400 Hz and -900 Hz at the nominal operating point (V_{in} = 400V). The characteristic equation is then solved for the unknowns K_p and K_i to determine the compensator gains.

The compensator gains obtained by solving the characteristic equation are then used to generate an analog transfer function of the compensator. The compensator transfer function is then converted to a discrete form by using the bilinear transform. The result of the bilinear transform generates the final difference equation of a digital PI compensator.

FIGURE C-2: HIGH-LEVEL BLOCK DIAGRAM OF CONTROL SYSTEM SHOWING PLANT AND CONTROLLER



C.4 Digital Control System Implementation:

Figure C-3 shows the top level block diagram of the LLC Converter model. The model consists of two separate implementations as follows.

- Analog LLC Converter model
- Digital LLC Converter model

The analog model provides most of the information needed for the compensator design. The digital system includes the effect of various phenomena like quantization errors, errors due to finite precision, effect of sampling and saturation limits. As a result, both analog and digital systems must be modeled to accurately model the real system. For simplicity, factors like scaling and ADC feedback gain are not included in the analog model.

FIGURE C-3: TOP LEVEL DIAGRAM OF SIMULINK MODEL OF LLC CONVERTER

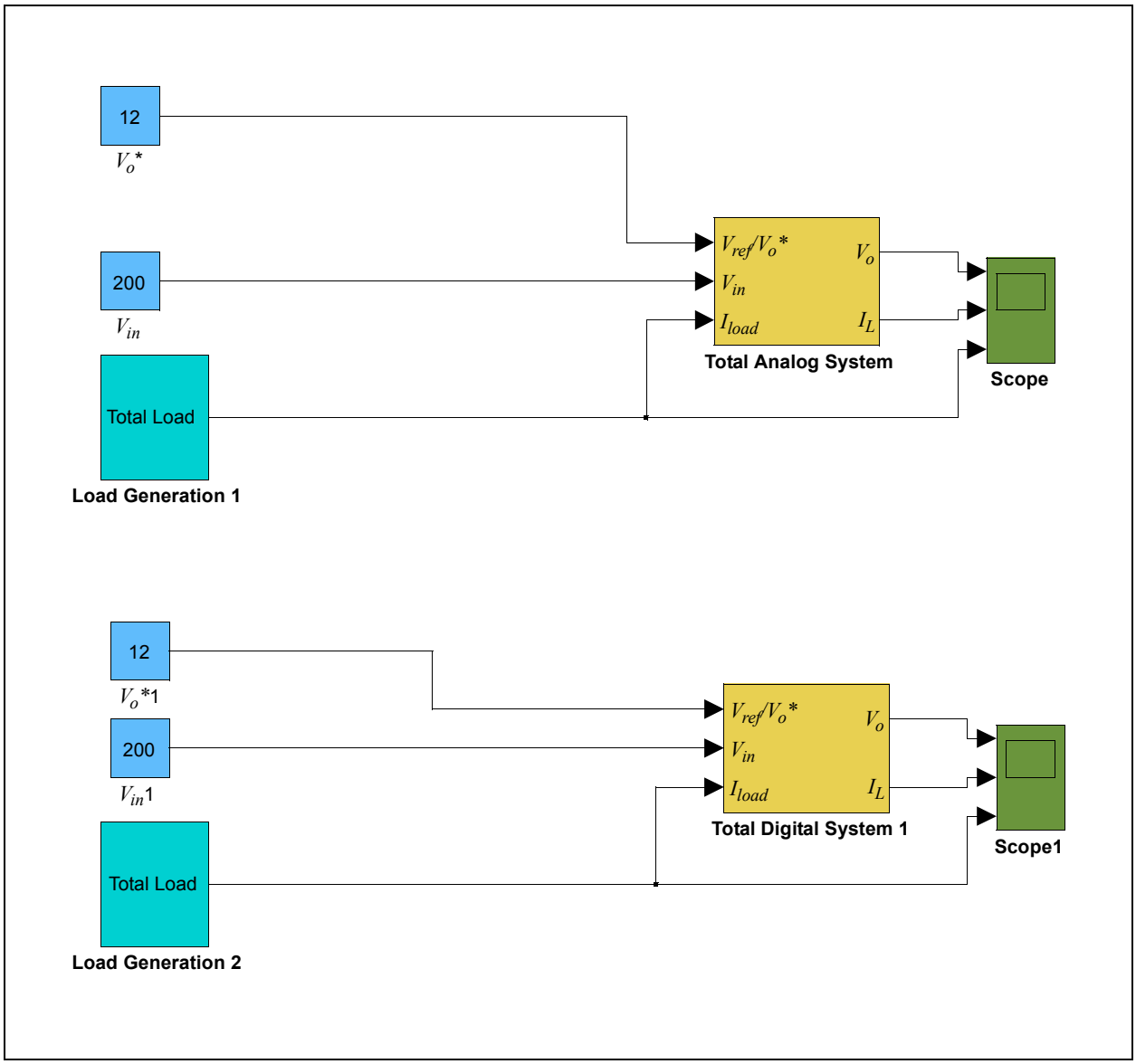
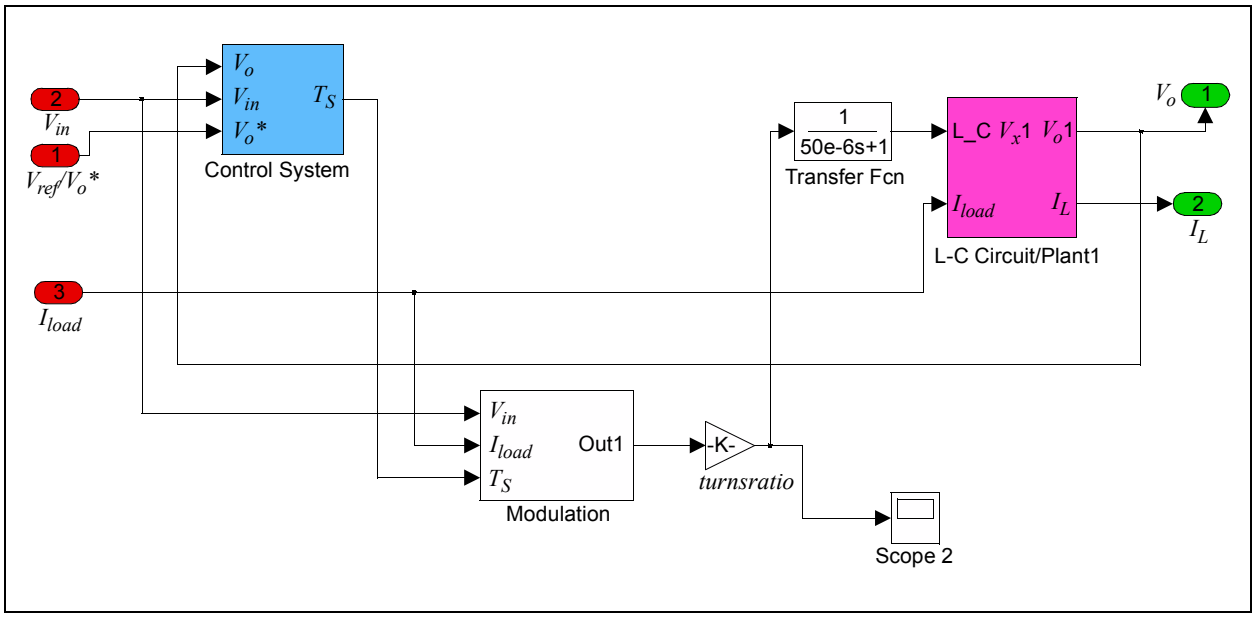


Figure C-4 shows the contents of the total analog system. All values are in real physical and standard units. It contains three main sub-systems:

- Output LC Filter / Plant
- Control System Block
- Modulation Block

FIGURE C-4: LLC CONVERTER ANALOG SYSTEM MODEL



The Output LC Filter/Plant block shown in Figure C-5, models the output inductor and capacitor with parasitics like the capacitor ESR and inductor DCR. The input to this block is the controlling voltage V_x and load current I_{load}, while the output of the block is the output voltage of the system.

FIGURE C-5: OUTPUT LC FILTER/PLANT

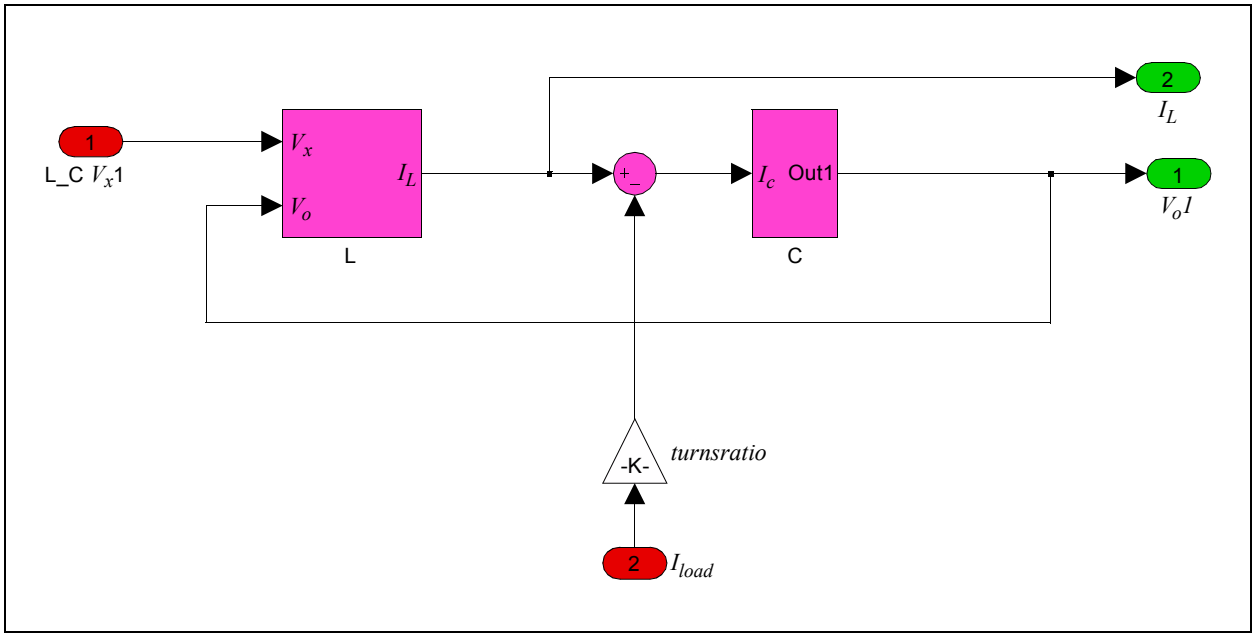
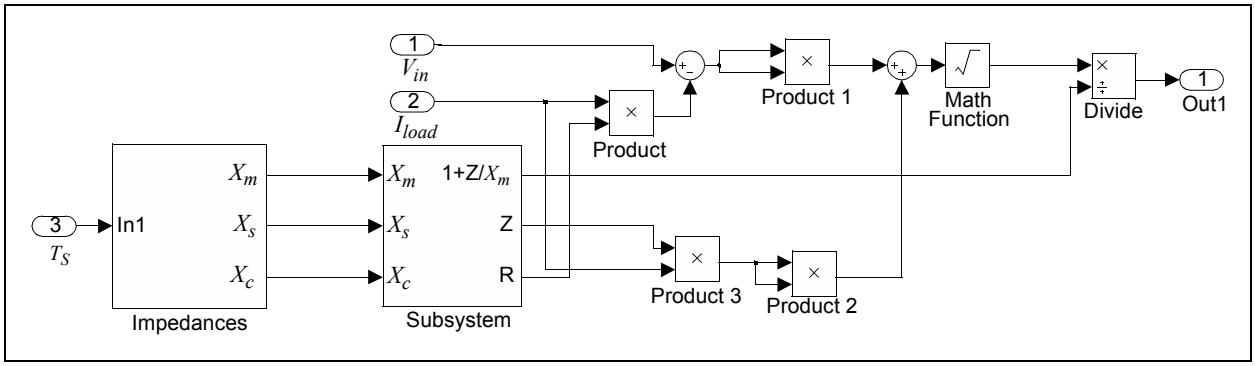


Figure C-6 shows the modulation block of the LLC Converter model. This block implements the gain equation of the LLC circuit, as given by Equation C-1. The input to the modulation block is the switching period value calculated by the control system block. The period value is converted into the transformer primary voltage V_{pri}, which is then converted to the controlling voltage V_x by using Equation C-2. In essence, the modulation block implements the operation of the LLC circuit. Due to the reactive nature of the LLC circuit, the current flowing through it may not be in phase with the voltage. The output voltage is only a function of the magnitude of the V_{pri} voltage. As a result, the modulation block calculates the magnitude of V_{pri} to obtain V_x.

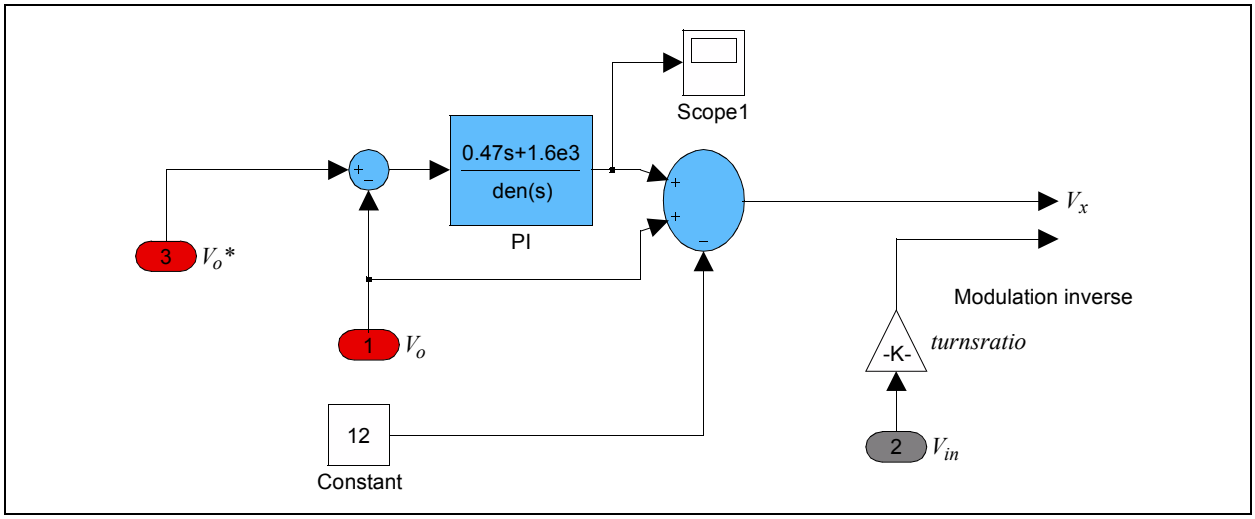
FIGURE C-6: MODULATION BLOCK



The control system block shown in Figure C-7 implements the digital PI compensator and an inverse modulation block. The inputs to the control system block are the voltage reference and measured output voltage, while the output is the desired switching period.

The PI compensator is designed for real units, and therefore the output of the PI block is in volts. The modulation inverse block converts the output of the PI compensator to the desired switching period and also factors in the effect of any changes in V_{in}.

FIGURE C-7: ANALOG CONTROL SYSTEM BLOCK



We use a method called digital by emulation. In this method, an analog control system model is created and then converted into a discrete control system. To account for discretization, Zero order hold, 16-bit finite precision, 10-bit ADC resolution (quantization) and computational delays must be incorporated in the digital control system model. These factors are implemented in the digital control system block, shown in Figure C-8.

All voltage quantities are scaled to a base voltage and all time quantities are scaled to base time quantity. The base voltage is the output voltage that will produce a full scale ADC reading. The base time quantity is the maximum allowable switching period in the system.

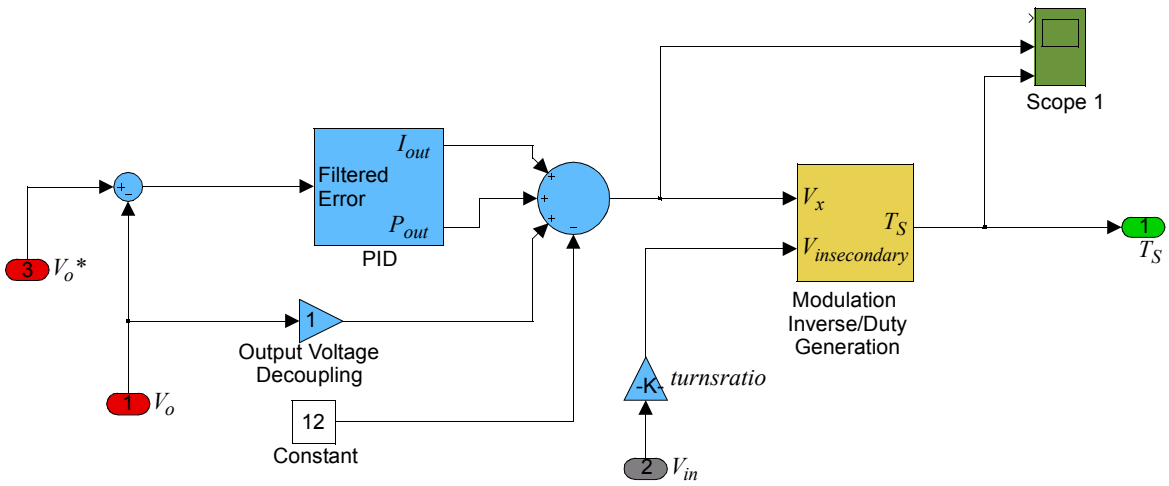
As a result, all voltage quantities used in the control system are represented as a fraction of the base voltage. Similarly, all time quantities are represented as a fraction of the base period. The actual implementation of the control system is therefore done using the Q15 fractional format.

Due to the conversion to Q15 on all inputs of the control system, the inverse conversion back to real units must be performed at the output of the control system. Therefore the final output is multiplied with the base period to generate the new period value.

The Q15 format limits all numbers in the range -1 to +1. Sometimes the coefficients generated after solving the characteristic equation and converting to discrete quantities may exceed this maximum range. In this case, the coefficients are divided using a prescaler in order to enable Q15 operations. The output is then post-multiplied to produce the correct result.

Ultimately, the equations to be implemented are as shown in Equation C-15.

FIGURE C-8: DIGITAL CONTROL SYSTEM BLOCK



EQUATION C-15:

$$T_{SQ15} = T_{nomQ15} + modifier \cdot voltagetotimefactor \cdot (V_{xQ15} + V_{oQ15} - V_{xnomQ15}) \cdot \frac{turnsratio}{V_{inmin}}$$

Where:

$$modifier = \frac{V_{inmin}}{V_{in}}$$

$$voltagetotimefactor = p_0^2 2\pi^2 f_r C_r L_m$$

V_{xQ15} = output of the digital PI compensator

V_{oQ15} = output voltage decouple term

$V_{xnomQ15}$ = Output voltage reference

We then define another constant, *multiplier*, as shown in Equation C-16.

EQUATION C-16:

$$multiplier = voltagetotimefactor \cdot \frac{turnsratio}{V_{inmin}}$$

We can then replace the constants in Equation C-16 with the constant *multiplier* and obtain the final expression for the switching period as shown in Equation C-17.

EQUATION C-17:

$$T_{SQ15} = T_{nomQ15} + modifier \cdot multiplier \cdot (PI_{outputQ15} - V_{xnomQ15} + V_{oQ15})$$
$$T_S = T_{SQ15} \cdot T_{max}$$

C.5 Simulation Results

FIGURE C-9: LOOP GAIN PLOT (ANALOG AND DIGITAL)

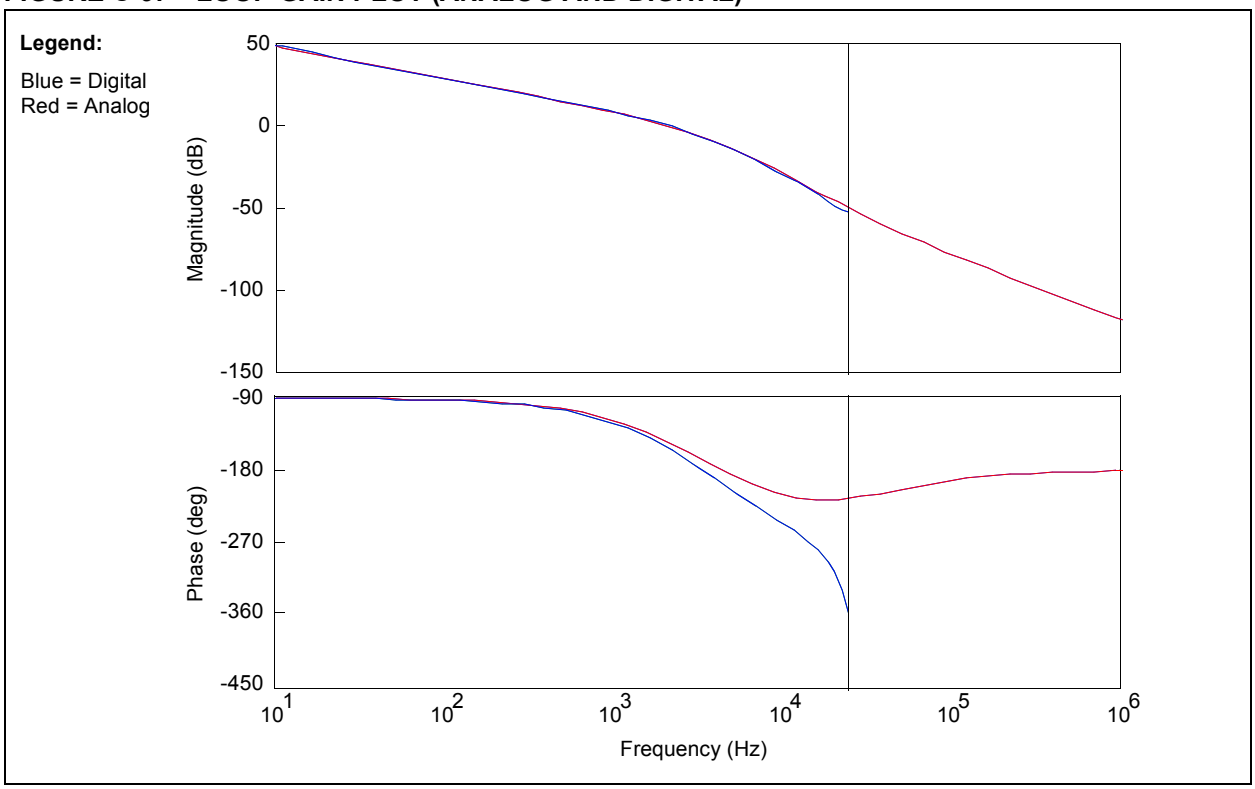


FIGURE C-10: CLOSED LOOP PLOT (ANALOG AND DIGITAL)

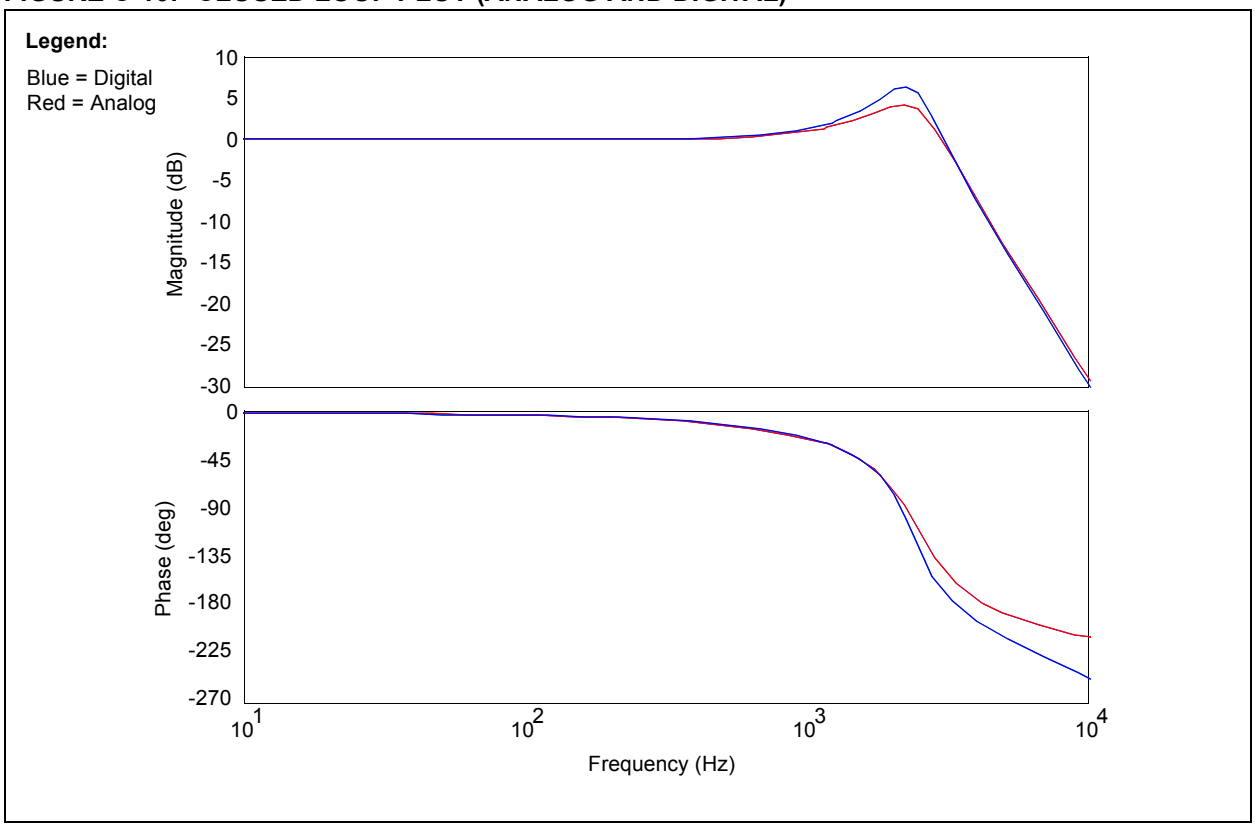


FIGURE C-11: DISTURBANCE REJECTION (ANALOG ONLY)

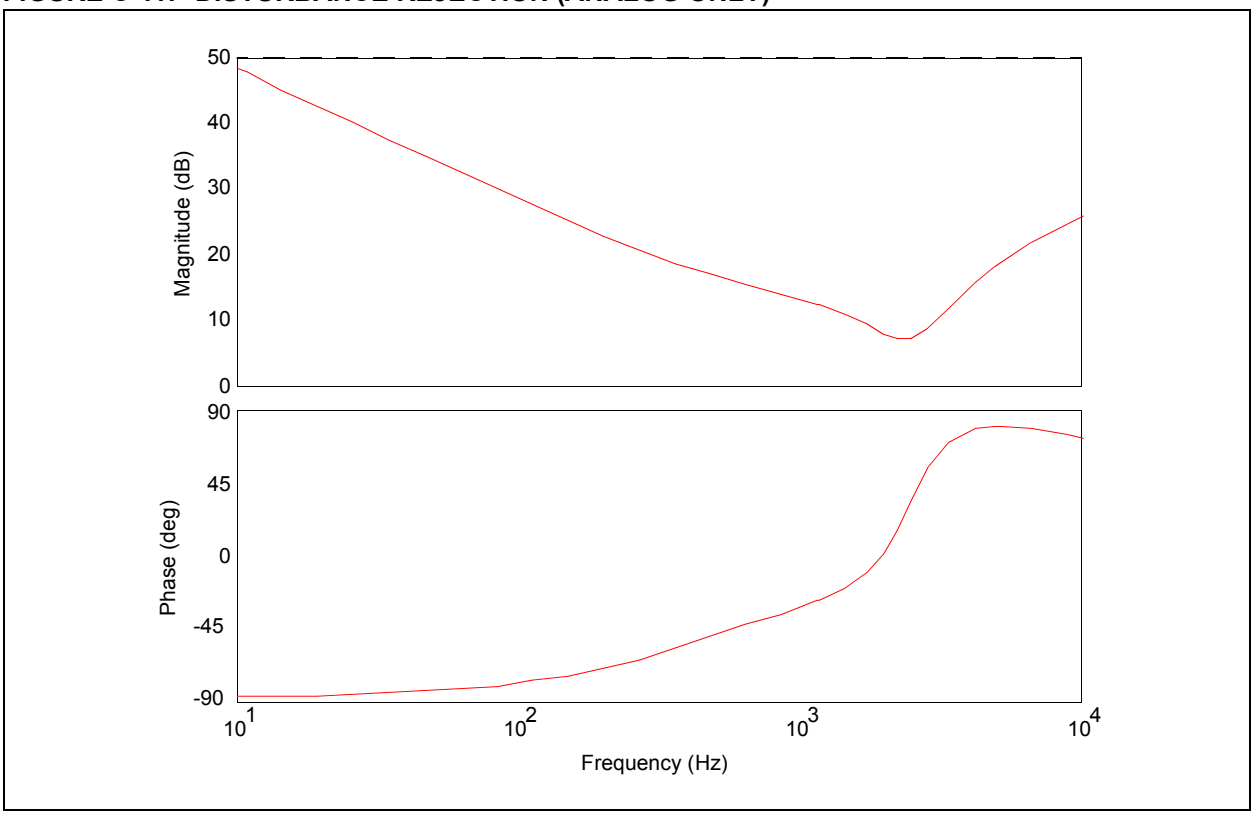
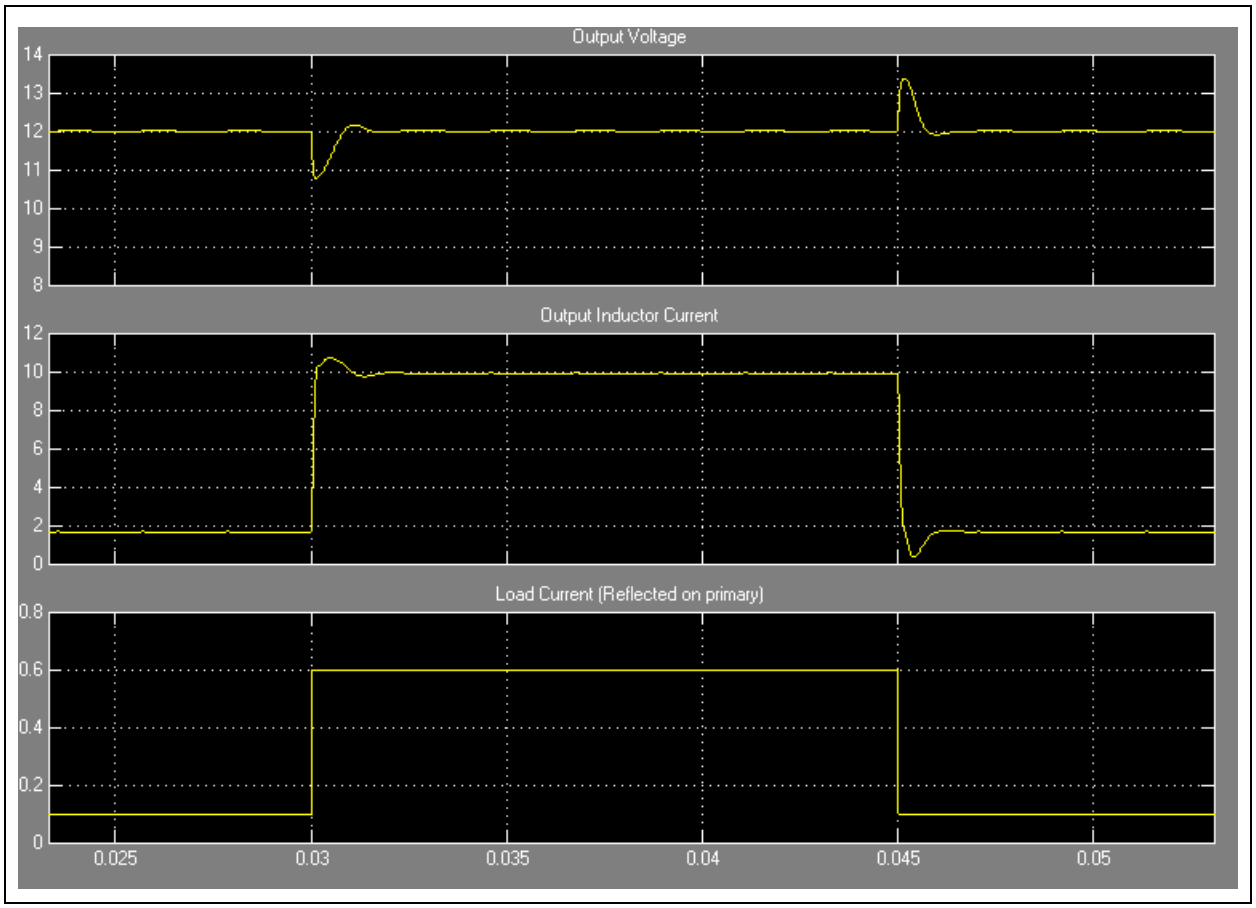


FIGURE C-12: TRANSIENT RESPONSE SIMULATION



APPENDIX D: DESIGN PACKAGE

A complete design package for this reference design is available as a single WinZip® archive file. This archive can be downloaded from the Microchip corporate Web site at: **www.microchip.com**

D.1 Design Package Contents

The design package contains the following items:

- Reference design schematics
- Fabrication drawings
- Bill of materials
- Assembly drawings
- Hardware design Gerber files

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