

# Active Clock Tuning for PIC16(L)F191XX Family

#### Introduction

Active Clock Tuning (ACT) is a feature on the PIC16(L)F191XX family of devices. The ACT module works by continuously adjusting the High-Frequency Internal Oscillator (HFINTOSC), using an available external 32.768 kHz oscillator attached to the Secondary Oscillator (SOSC) pins to achieve ±1.0% clock accuracy. Since the PIC16(L)F191XX family does not support other external crystal modes, the ACT was added to remove the need for an external high-accuracy clock source. The increased accuracy of the ACT module is useful in serial communications like UART, SPI, and I<sup>2</sup>C.

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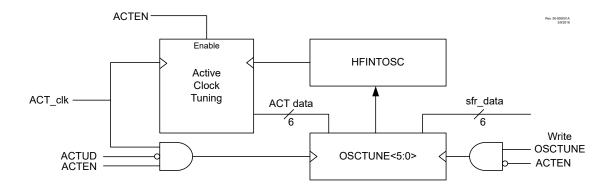
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## 1. Active Clock Tuning

The ACT module requires the use of a 32.768 kHz external crystal connected to the SOSC pins. The SOSC time base is then used to adjust the frequency of the HFINTOSC over the datasheet specified voltage and temperature range of the device. The ACT module does this by actively adjusting the OSCTUNE<5:0> bits in real time to closely maintain the calibrated oscillator frequency.

When the ACT module is enabled, the OSCTUNE bits are read-only to the user. Any writes by the user when the module is enabled are inhibited. The ACT module will adjust the HFINTOSC to maintain the calibrated frequency by updating the OSCTUNE bits at the specified ACT update rate. The operation of the ACT module works without the need for user software interaction, and instead only relies on the initial module configuration.

Figure 1-1. ACTIVE CLOCK TUNING BLOCK DIAGRAM



The ACT module makes the internal HFINTOSC a high-accuracy oscillator by using the SOSC as a "fixed" reference source over voltage and temperature. The ACT will only be as accurate as the 32.768 kHz crystal used in the application. It is important to note that if the selected crystal varies considerably over voltage or temperature, HFINTOSC will also display the same behavior.

#### 1.1 Secondary Oscillator Initialization

The SOSC is a separate oscillator block in the device that is required in order to use the ACT module. The oscillator block is optimized for a 32.768 kHz crystal oscillator connected to the SOSCI and SOSCO pins. There are two register bits associated with SOSC configuration: the Secondary Oscillator Power Mode Selection (SOSCPWR) bit of OSCCON3, and the Secondary Oscillator Manual Request (SOSCEN) bit of OSCEN.

In the event of a Power-on-Reset (POR) event, SOSCPWR is cleared and will operate in Low-Power mode. The SOSCEN bit is also cleared, leaving the SOSC in a state where it could be enabled by another peripheral. These settings allow the ACT module to enable the SOSC.

In low-power applications (e.g., battery-powered devices), the low-power setting of SOSCPWR is appropriate. The High-Power mode may be necessary for crystals requiring higher drive strength. To enable High-Power mode the SOSCPWR bit of the OSCCON3 must be set.

#### 1.2 Peripheral Module Disable Initialization

The Peripheral Module Disable (PMD) allows users the ability to disable selected modules, placing them into their lowest power state. The Disable Active Clock Tuning (ACTMD) bit of the PMD0 register is cleared by default, meaning the module is enabled. The ACT module can be manually disabled by setting the ACTMD bit of the PMD0 register (ACTMD = 1).

#### 1.3 Active Clock Tuning Initialization

The ACT module is enabled by writing to the ACTCON register. If the user requires any changes to the SOSC or PMD modules, those changes need to be made in their respective registers. The ACT can be enabled by setting the ACTEN bit in the ACTCON register. Once enabled, the ACT takes control of the OSCTUNE register. The OSCTUNE register is automatically adjusted every reference clock cycle. The code below demonstrates the basic setup and configuration of Active Clock Tuning.

```
...
// Set SOSC to high-power mode, Application/Crystal dependent
OSCCON3bits.SOSCPWR = 1;

// PMD (ACTMD) module enable, Not a requirement
PMD0bits.ACTMD = 0;

// Enable ACT
ACTCONbits.ACTEN = 1;
...
```

#### 1.4 Active Clock Tuning Update Disable

Active Clock Tuning can be suspended by setting the ACT Update Disable (ACTUD) bit of the ACTCON register. While in this mode, the ACT module is still enabled but no longer updates the OSCTUNE register. The user cannot write to the OSCTUNE register while ACTUD and ACTEN are set.

## 1.5 Active Clock Tuning Lock Status

The ACT Lock (ACTLOCK) bit of the ACTCON register is used to communicate the status of the ACT module. When HFINTOSC is successfully tuned within ±1.0% of its nominal value, hardware will set the ACTLOCK bit which is read-only by the user. The conditions where the ACTLOCK bit will be cleared include Out-of-Lock condition, a device Reset, and when the ACT module is disabled. The Out-of-Lock condition can occur during initial SOSC startup, SOSC failure, and instances where the ACT is Out-of-Range.

## 1.6 Active Clock Tuning Out-of-Range Status

When the ACT requires an OSCTUNE value that is outside the range of the OSCTUNE register, then the ACT Out-of-Range (ACTORS) bit of the ACTCON register is set by hardware. The Out-of-Range status can occur in one of two ways.

- When the HFINTOSC is tuned to its lowest frequency and the ACT module requests a lower frequency that OSCTUNE can accommodate, the hardware sets the ACTORS bit.
- When the HFINTOSC is tuned to its highest frequency and the ACT module requests a higher frequency that OSCTUNE can accommodate, the hardware sets the ACTORS bit.

HFINTOSC will continue to use the last written OSCTUNE value during an Out-of-Range event. Once the ACT module requests a frequency within the tunable range of OSCTUNE and hardware sets the ACTLOCK bit, the hardware will clear the ACTORS bit. Note that this bit is read-only.

#### 1.7 Active Clock Tuning Interrupts

Interrupts for the ACT module are enabled by setting the Clock Recovery Interrupt Enable (CRIE) bit in the PIE6 register. Along with the CRIE bit, peripheral interrupts need to be enabled by setting the Peripheral Interrupt Enable (PEIE) bit in the INTCON register. Once those interrupts are enabled, the Global Interrupt Enable (GIE) bit of the INTCON register needs to be set to enable interrupts to take place.

The Clock Recovery Interrupt Flag (CRIF) bit of the PIR6 register will be set when the ACTLOCK or ACTORS bits change state and the module is enabled (ACTEN = 1). This generates an interrupt whenever the ACT module changes state. Interrupts will not be generated for each OSCTUNE update unless that update results in a change of lock status.

# 2. Active Clock Tuning Accuracy

The ACT increases the accuracy of the HFINTOSC by continuously updating the OSCTUNE register. To compare the accuracy of the instruction clock, data was collected across temperature (-40°C to 125°C) and voltage (2.3V to 5.5V). The first test case demonstrated the instruction clock accuracy without ACT enabled, followed by the second test case to show the clock accuracy with ACT enabled. The preliminary data was collected from several PIC16F19186 devices with HFINTOSC set for 8 MHz operations and the clock divider set to 4 for a system clock of 2 MHz.

The SOSC oscillator used was an NDK NX2012SA-32.768K-STD-MUB-1 crystal with two Panasonic ECJ-1VC1H090D 9pF, 50V, NP0, 0603 sized ceramic capacitors. User results will be different with other crystal, capacitors, or if there is a load resistor (Rs) in series with the crystal. The variation of the crystal frequency over voltage and temperature will also affect the accuracy.

Figure 2-1 shows the percentage of deviation in frequency over temperature at different voltages, ranging from 2.3V to 5.5V, centered at 25°C with ACT disabled. Figure 2-2 shows the same information with ACT enabled. Notice the percentage of deviation is ±0.07% with ACT enabled. This is significantly less than the nominal value stated in the datasheets for PIC16(L)F191XX devices. These results were obtained with the specific crystal, capacitors, and PCB used in the data collection and user results will vary.

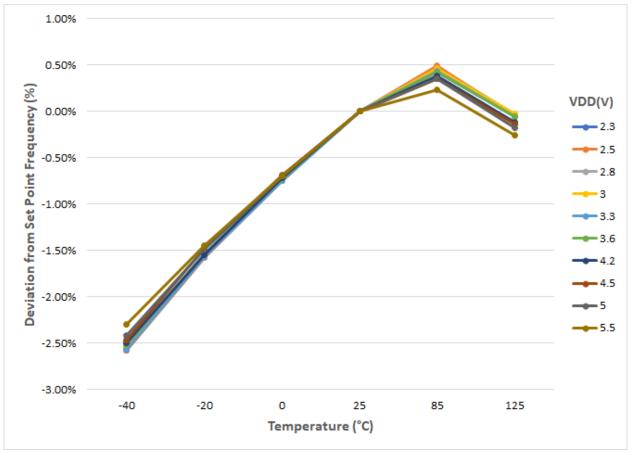


Figure 2-1. SYSTEM CLOCK ACCURACY WITH ACT OFF

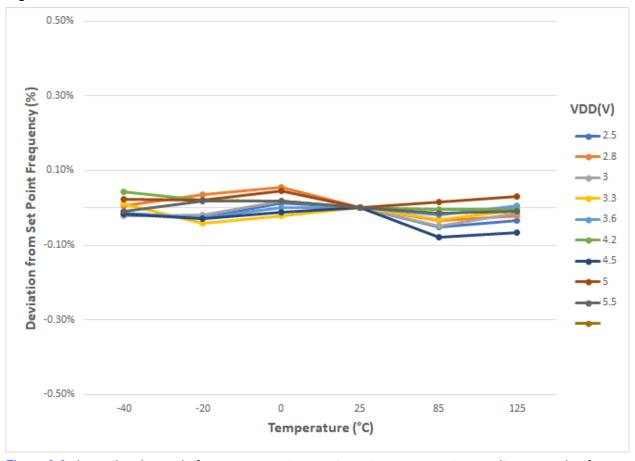


Figure 2-2. SYSTEM CLOCK ACCURACY WITH ACT ON

Figure 2-3 shows the change in frequency over temperature at common systems voltages ranging from 2.3V to 5.5V, with ACT disabled. In Figure 2-4 the same information was collected with ACT enabled. Here it is shown that with ACT enabled the deviation in frequency across temperature and voltage is less than with ACT disabled.

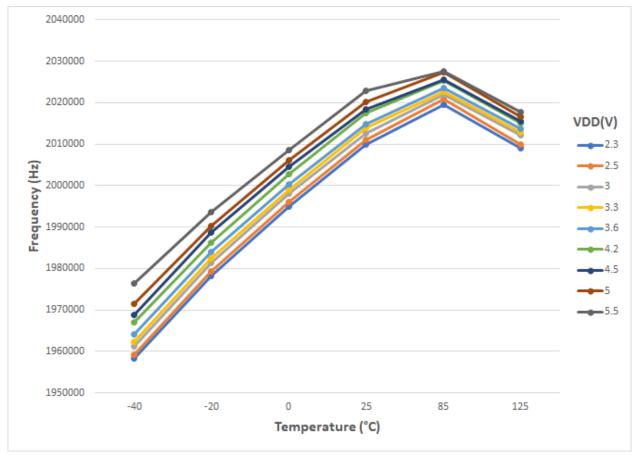
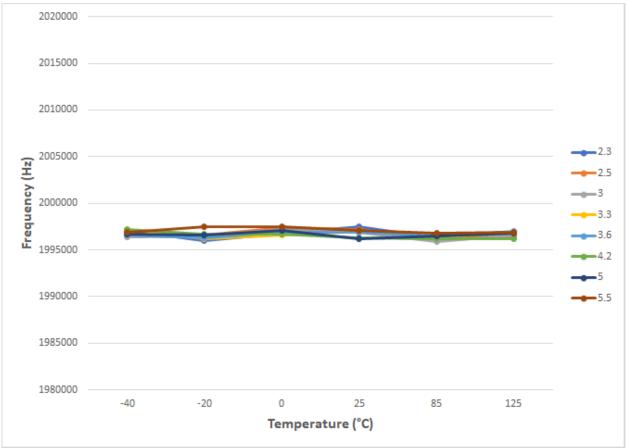


Figure 2-3. CHANGE IN FREQUENCY WITH ACT OFF

Figure 2-4. CHANGE IN FREQUENCY WITH ACT ON



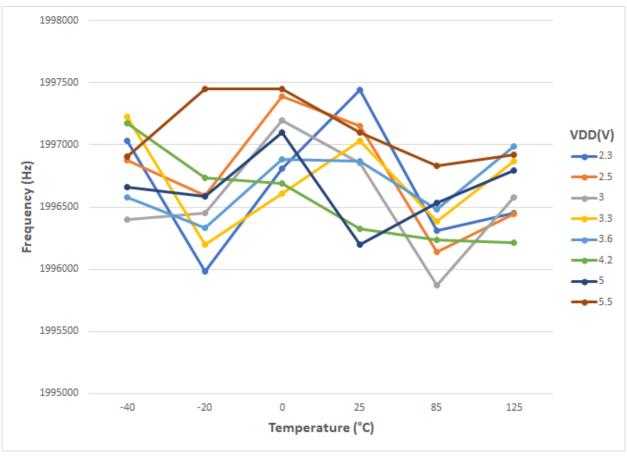


Figure 2-5. CHANGE IN FREQUENCY WITH ACT ON (Zoomed View)

## 3. Conclusion

The Active Clock Tuning feature on the PIC16(L)F191xx family of devices can provide a higher accuracy clock source than the HFINTOSC alone. As shown in Section 2: Active Clock Tuning Accuracy, with the addition of an external crystal and associated capacitors for the Secondary Oscillator, this is achievable. In applications requiring a higher accuracy clock, instead of using an expensive external clock source, an inexpensive 32.768 kHz crystal tied to the SOSC pins and ACT can meet the clock specification of the application.

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ISBN: 978-1-5224-3003-2

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