



Bringing the best of microcontroller innovations to new Cortex-M0+ devices

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The rate at which ARM-based microcontroller devices are being brought to the market is staggering. The use of a common family of compatible cores with different performance levels brings many benefits to embedded developers looking for a new device on which to base their new product design or new technology platform. However, in the rush to bring a device to the market microcontroller suppliers face the dilemma of spending time fine-tuning their peripheral set and architecture enhancements around the ARM core or, potentially, losing market share from loyal customers who need devices right now as they are embarking on new designs. This is very much the case with ARM's Cortex-M0/M0+ architecture. Realising that some of the power saving and peripheral enhancements incorporated in 8-bit devices over the past years have been highly valued by customers and that custom tailoring is needed to make the best possible product on any platform has made some microcontroller suppliers take a more thorough approach to bringing the latest Cortex-M0+ device to market. Atmel is one of them.

By first taking a step back with their first M0+ product, Atmel took stock of their 2 decades of experience developing 8-bit embedded flash microcontrollers and over 17 years being an ARM licensee. It was clear that much of the innovation made to their tinyAVR, megaAVR and AVR XMEGA devices would be highly relevant to their M0+ implementation. One example of an AVR feature that is highly valued by engineers is the Peripheral Event System. This is an approach that allows peripherals to cooperate with each other without using any CPU or bus resources. Atmel's low power IP has also been much valued. This includes

using low power oscillators, clock gating and prescaling in addition to sleep walking modes and serial communication improvements to allow no loss of data when waking up from a deep sleep mode.

As a result of incorporating many aspects of Atmel's own microcontroller innovations with ARM's core IP the Atmel Cortex-M0+ based-device, the SAM D20, has a CoreMark benchmark of 2.14coreMark/MHz and a power consumption better than 150 $\mu\text{A}/\text{MHz}$ in active mode and around 2 μA when in RAM retention mode. By comparison, other devices on the market have active power consumption in the range of 200 - 400 $\mu\text{A}/\text{MHz}$ performing the same tasks at the same performance levels. Let's look a bit more closely at some of the enhancements that have made this possible.

As previously mentioned, the Event System allows peripherals to communicate without involving any CPU activity. It is a routing network independent of the traditional data bus paths. Different triggers at the peripheral level can result in an event; like a timer tick triggering a reaction in another peripheral. Comprising eight independent channels the Event System has a fixed latency of 2 cycles. Without any jitter it is a 100% deterministic method and a perfect fit for real-time applications. No events are lost and they are handled at a peripheral level in 2 cycles, even if the CPU is performing a non maskable interrupt. Traditionally the way of handling actions for a low power application would be through the use of interrupts. Interrupts however would wake up the CPU. For example, consider a motor drive application using PWM. To detect erroneous situations many motor applications use an analog comparator or ADC to measure the current going into the motor drive, in an over current situation you want to shut down the PWM channels driving the motor as soon as you can to prevent permanent damage to the circuit and for safety reasons. Without an Event System the overcurrent situation will trigger an interrupt, but the interrupt service request might be delayed if the CPU is performing other higher priority tasks. Using the Event System you can connect the analog comparator or ADC directly to the timer and always shut down the timer in 2 cycles, regardless of what the rest of the MCU is doing.

Figure 1 illustrates how the Event System would manage the motor control current protection without the need for any intervention from the CPU. There are many advantages to this approach, the main ones being lowering the overall power consumption budget, the efficient off-loading of routine tasks from the CPU and achieving a totally predictable reaction time.

One of the other major differentiating features of Atmel's device is the provision of a highly configurable multiple serial communication module

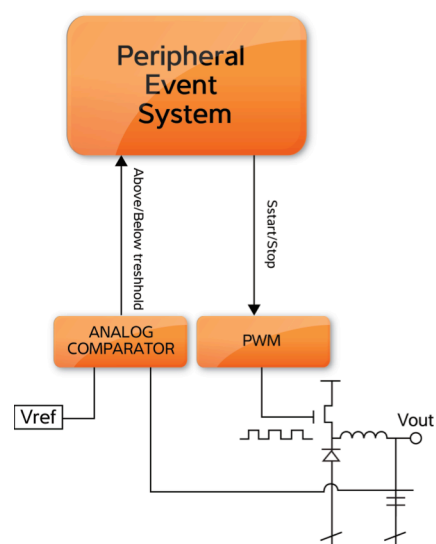


Figure 1 –Event System – Example of motor control driver

(SERCOM). Comprising up to 6 serial interface channels, each serial port is software configurable to become an I2C, SPI or USART interface. This gives developers immense flexibility when embarking on a design since it allows you to configure the available interfaces as you need them. For example, if you require 2 I2C and 4 UART that is what you do. There are two very important benefits to this approach for the embedded developer. Firstly, you no longer need to trawl through microcontroller specifications looking for a device with the number of types of serial interfaces you require. Not only does this save a lot of time but it also allows you to adopt a single microcontroller for a number of similar designs where the interfaces required may differ slightly and you no longer have to buy a device that has 5 UARTS because you need 3 SPIs. The second benefit relates to design of the PCB. By choosing the interface type to coincide with the location of any supporting interface components or interconnect on the PCB you can make more efficient PCB routing that is not only potentially shorter, but also avoids any long signal paths past electrically noisy components. This is made possible by having multiple SERCOM modules and the fact that each SERCOM module has multiple pin connection options. Atmel's SAM D20 device supports I2C fast mode of up to 400 kHz while SPI and UART are capable of up to 24 Mb/s transfer speeds. The serial communication modules all are connected to the peripheral event system, mentioned above, that allows peripheral cooperation without CPU intervention. While unlikely to be required for many applications, each SERCOM module is also capable of being reconfigured by software into another interface type on-the-fly.

Finally, in order to deliver a Cortex-M0+ design with the most useful features embedded developers might seek, Atmel has also added a peripheral touch controller into the SAM D20 based on the extensive knowledgebase from the maXTouch product line. This, the most innovative of the new peripherals on the SAM D20, can be used to implement touch control interfaces using buttons, wheels and sliders. The ability to detect using proximity is also possible. Supporting up to 256 channels in a matrix configuration, the peripheral touch controller module supports both mutual and self capacitance-sensing methods. Providing excellent noise rejection and sensitivity characteristics together with self-calibration gives the SAM D20 a lot of touch controls capabilities on-chip.



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