USB2422

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB2422. These checklist items should be followed when utilizing the USB2422 in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "USB Signals"
- Section 5.0, "USB Connectors"
- Section 6.0, "Clock Circuit"
- Section 7.0, "Power and Startup"
- Section 8.0, "Configuration Options"
- Section 9.0, "Hardware Checklist Summary"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The USB2422 implementor should have the following documents on hand:

- *USB2422 2-Port USB 2.0 Hi-Speed Hub Controller Data Sheet*
- USB2.0 Specification
- B1.2 Specification

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.4 USB-IF Compliant USB Connectors

- USB-IF certified USB Connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

3.0 POWER

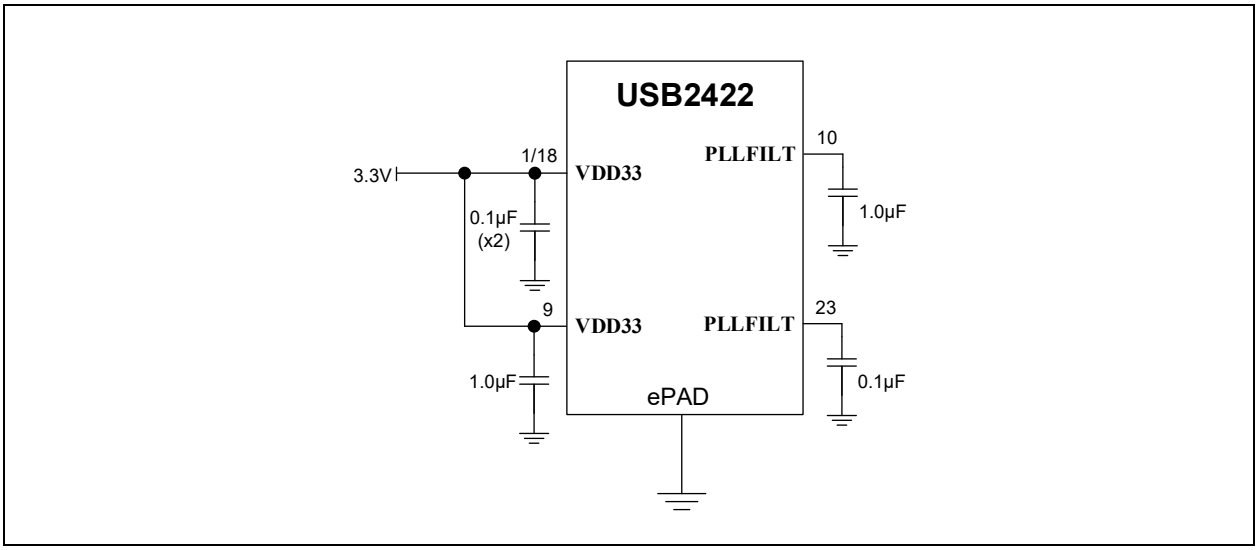
- The analog supplies (**VDD33**) are located on pins 1, 9, and 18. All these pins require a connection to a regulated 3.3V power plane.
- The **VDD33** pins 1 and 18 each should include 0.1 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The **VDD33** pin 9 should include 1.0 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- Pin 10 (**CRFILT**) is a core regulator output and should connect to an external filter capacitor. A 1.0 µF capacitor is

recommended. Do not power external circuitry from this regulator output.

- Pin 23 (**PLLFILT**) is a PLL regulator output and should connect to an external filter capacitor. A 0.1 µF capacitor is recommended. Do not power external circuitry from this regulator output.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



4.0 USB SIGNALS

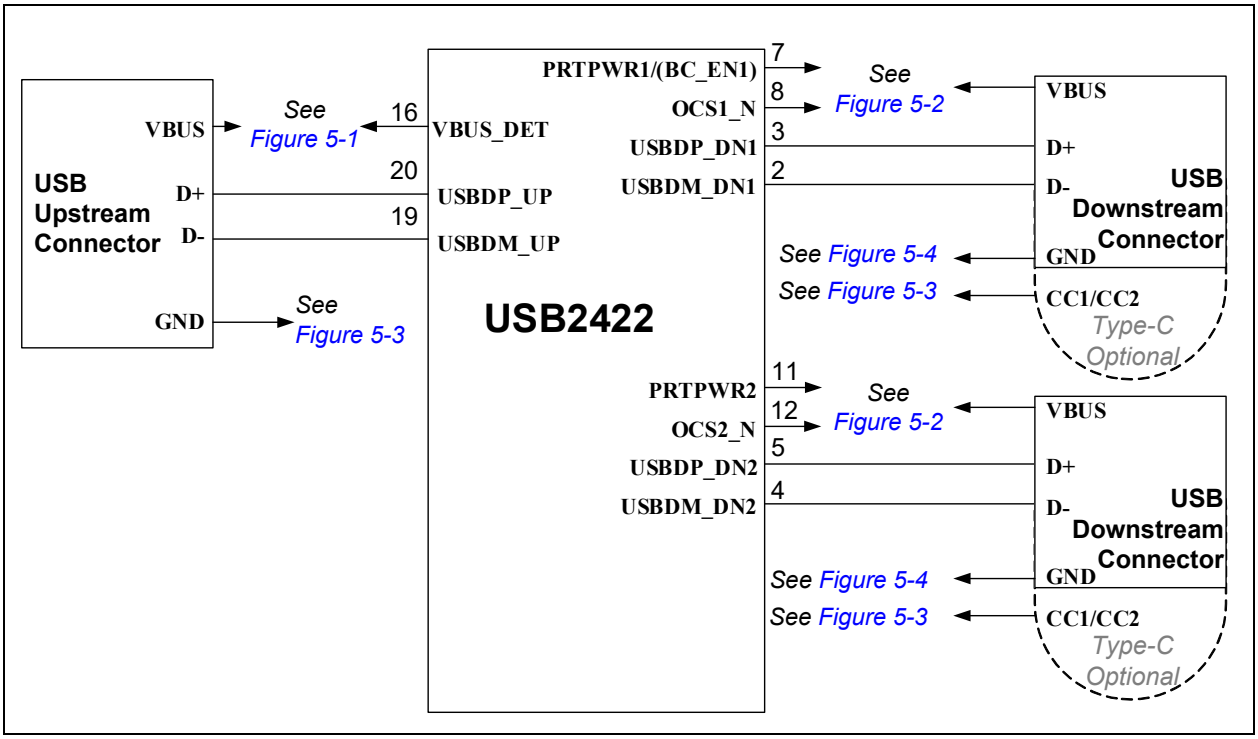
4.1 USB PHY Interface

- **USBDP_UP** (pin 20): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the **D+/DP** pin of a USB Connector.
- **USBDM_UP** (pin 19): This pin is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the **D–/DM** pin of a USB Connector.
- **USBDP_DN1** (pin 3): This pin is the positive (+) signal of the downstream port 1 USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the **D+/DP** pin of a USB Connector.
- **USBDM_DN1** (pin 2): This pin is the negative (–) signal of the downstream port 1 USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the **D–/DM** pin of a USB Connector.
- **USBDP_DN2** (pin 5): This pin is the positive (+) signal of the downstream port 2 USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the **D+/DP** pin of an embedded device or second tier hub either directly on the PCB or through a permanently attached USB cable/wiring harness.
- **USBDM_DN2** (pin 4): This pin is the negative (–) signal of the downstream port 2 USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the **D+/DP** pin of an embedded device or second tier hub either directly on the PCB or through a permanently attached USB cable/wiring harness.

Note: The polarity of any USB2.0 differential pair may be inverted intentionally either due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via SMBus/I^2C configuration registers.

For transmit and receive channel connections details, refer to Figure 4-1.

FIGURE 4-1: USB DATA SIGNAL CONNECTIONS



4.1.1 DISABLE DOWNSTREAM PORTS IF UNUSED

- If any downstream port of the USB2422 is unused, it should be disabled. This can be achieved through hub configuration (I^2C) or through a port disable strap option.

4.2 USB Protection

- The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These are generally grouped into three categories:

1. TVS protection diodes
   - ESD protection for IEC-61000-4-2 system level tests
2. Application-targeted protection ICs or galvanic isolation devices
   - DC overvoltage protection for short to battery protection
3. Common-mode chokes
   - For EMI reduction

The USB2422 can be used in conjunction with these types of devices, but it is important to understand the negative effect on USB signal integrity that these devices may have. Users must select components accordingly and follow the implementation guidelines from the manufacturer of these devices. They may also use the following general guidelines for implementing these devices:

- Select devices that are designed specifically for high-speed applications only. Based on the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
- These devices should be placed as close to the USB connector as possible.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- The effectiveness of TVS devices depends heavily on effective grounding. Always ensure a very low impedance path to a large ground plane.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

Note: Microchip PHYBoost configuration options are available for compensating the negative effects of these devices. This feature may help overcome marginal failures. It is simplest to determine the appropriate setting using laboratory experiments, such as USB eye diagram tests on physical hardware.

5.0 USB CONNECTORS

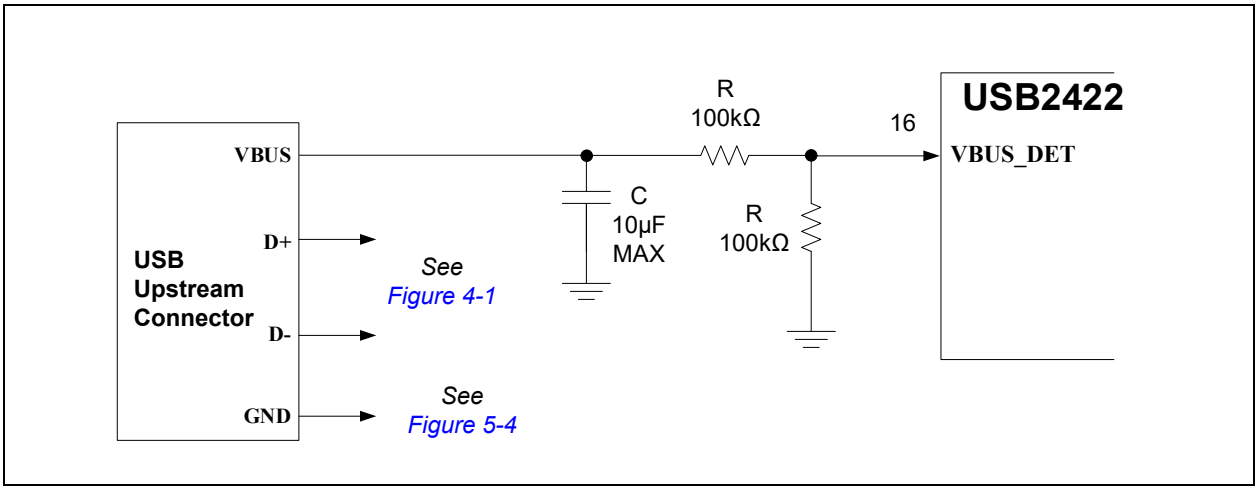
5.1 Upstream Port VBUS and VBUS_DET

- The upstream port VBUS line must have no more than 10 µF of the total capacitance connected.
- The **VBUS_DET** pin is used by the USB2422 to detect the presence of a USB host. The USB host can also toggle the state of VBUS at any time to force a soft Reset and reconnection of the USB2422.
- It is permissible to tie **VBUS_DET** directly to 3.3V. However, this is not recommended because the ability to force a Reset of the hub from the USB host VBUS toggling is lost.

The recommended implementation is shown in Figure 5-1. Note that the precise resistor values are not critical and alternate values may be selected as long as:

- The impedance from the **VBUS** pin of the USB connector to the **VBUS_DET** pin is sufficiently high-impedance to minimize pin leakage when VBUS is present before the Hub IC is powered on.
- A sufficient voltage level is present on the **VBUS_DET** for the full range of VBUS (4.5V – 5.5V).

FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS



5.2 Downstream Port VBUS and PRTPWRx/OCSx_N

5.2.1 PRTPWRX

The **PRTPWRx** pin is an output pin which has the following states:

1. PORT OFF: **PRTPWRx** drives low. The **PRTPWRx** pin will only transition to the PORT ON state through a specific command from the USB host.
2. PORT ON: **PRTPWRx** drives low. The **PRTPWRx** pin will only transition to the PORT OFF state if:
   - An overcurrent event is sensed on **OCSx_N** pin.
   - A command from the USB host is received which instructs the hub to disable power.
   - The hub is reset or experiences a POR event

- To ensure minimal BOM cost and simplicity, select a port power controller device with a 3.3V logic level, active-high input. If a device which operates from a 5V logic level is selected, the **PRTPWRx** signal may need to be boosted using external logic. If a port power controller with active-low input is selected, the **PRTPWRx** signal needs to be inverted using external logic.

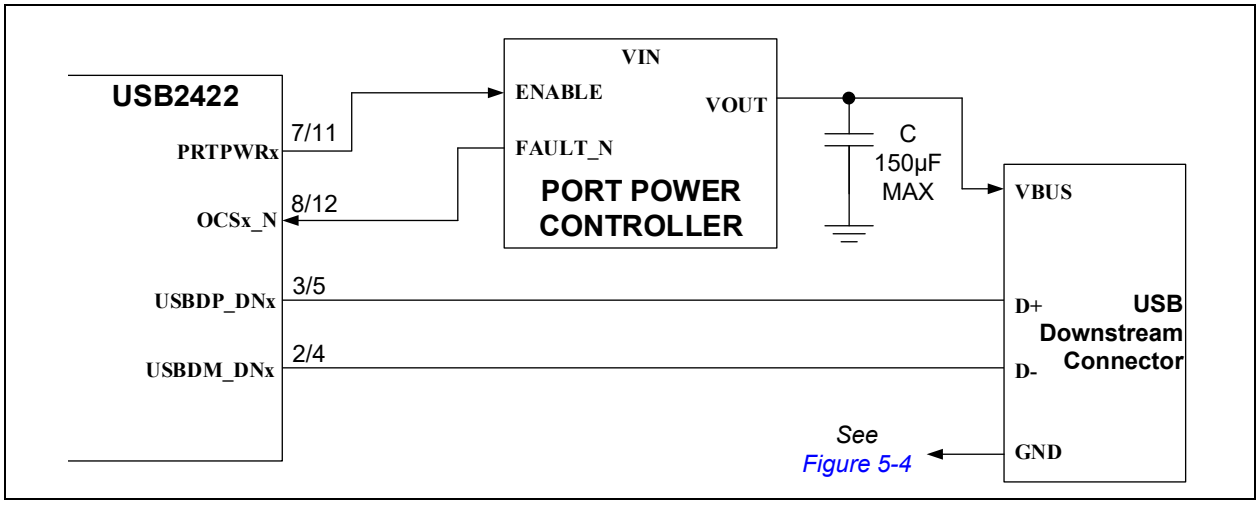
5.2.2 OCSX_N

The **OCSx_N** pin is an input buffer which monitors overcurrent events. The pin includes an internal pull-up resistor to the 3.3V domain, so an external pull-up resistor is not required. The pin state is ignored when the port is in the PORT OFF state. When the port is in the PORT ON state, an overcurrent event is detected if the state of the pin is detected as low (below the V_{ILI} voltage). When an overcurrent event is detected, the port automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

To ensure minimal BOM cost and simplicity, select a port power controller device with an active-low, open-drain Fault indicator output. If a port power controller with active-high Fault indicator output is selected, the OCSx_N signal needs to be inverted using external logic.

A typical VBUS port power control implementation is shown in Figure 5-2.

FIGURE 5-2: DOWNSTREAM VBUS AND PRTCTL1 CONNECTIONS



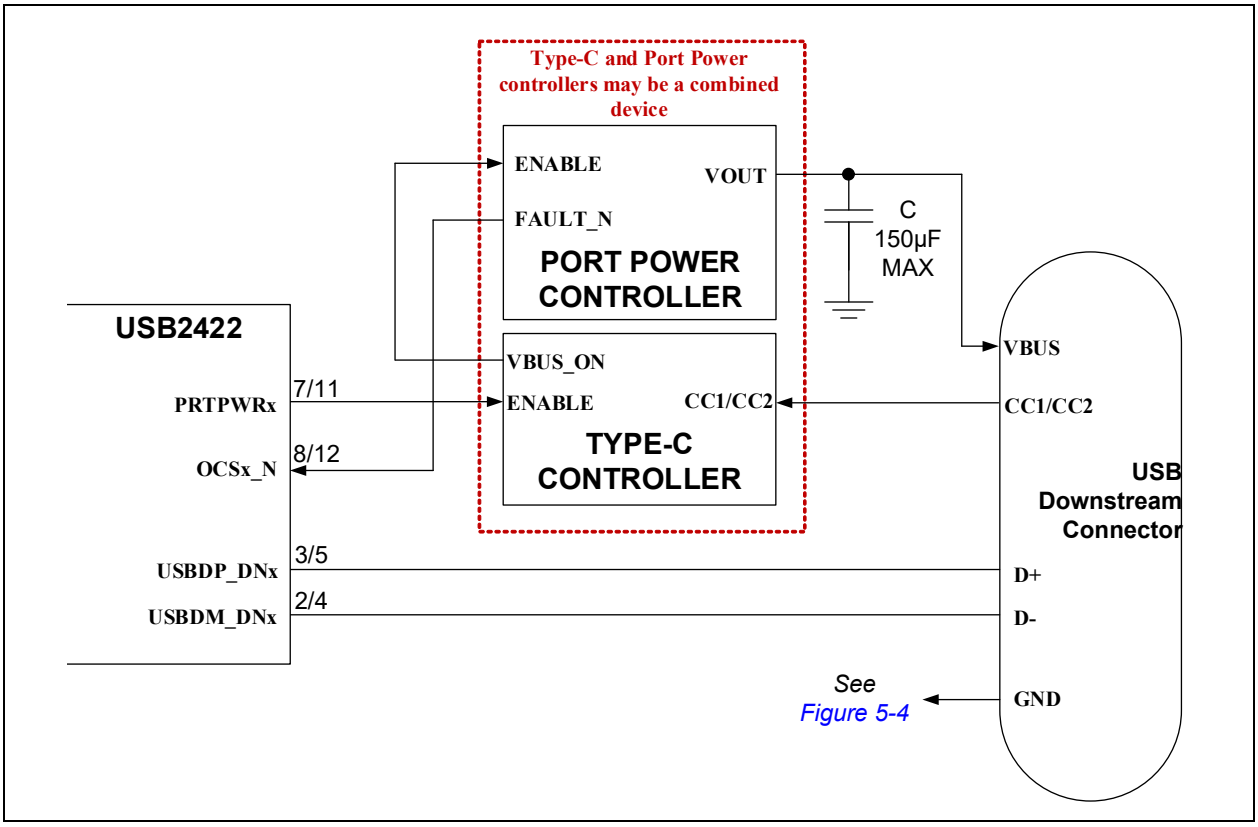
Note: The implementation, as shown in Figure 5-2, assumes that the port power controller has an active-high enable input, and an active-low, open-drain style Fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.3 Downstream Port USB Type-C® Support

- USB2422 may be used with USB Type-C® as the downstream port. This requires a Type-C port controller or combined port power controller and Type-C port controller. The USB2422 simply controls the Type-C port controller in same way it would control a standard Type-A port power controller. It does not require any kind of Type-C port status information from the Type-C port controller. The PRTPWRx signal should be connected to an enable pin on the Type-C controller, and the OCSx_N signal should connect to the Fault indicator output of the port power controller.
- If the Type-C controller and the port power controller are separate devices, the Type-C controller must control the enable pin of the port power controller. The PRTPWRx should not directly control the VBUS enable signal of the port power controller.
- A Type-C controller may be configured to signal a 500 mA, 1.5A, or 3.0A port power capability. The selected port power controller should be sized accordingly.

A typical implementation is shown in Figure 5-3.

FIGURE 5-3: DOWNSTREAM VBUS AND PRTCTL1 CONNECTIONS WITH A USB TYPE-C® PORT



Note: The implementation shown in Figure 5-3 assumes that the USB Type-C controller has an active-high enable input, and the port power controller has an active-low, open-drain style Fault indicator. External polarity inversion through buffers or FETs may be required if the USB Type-C controller and port power controller have different I/O characteristics.

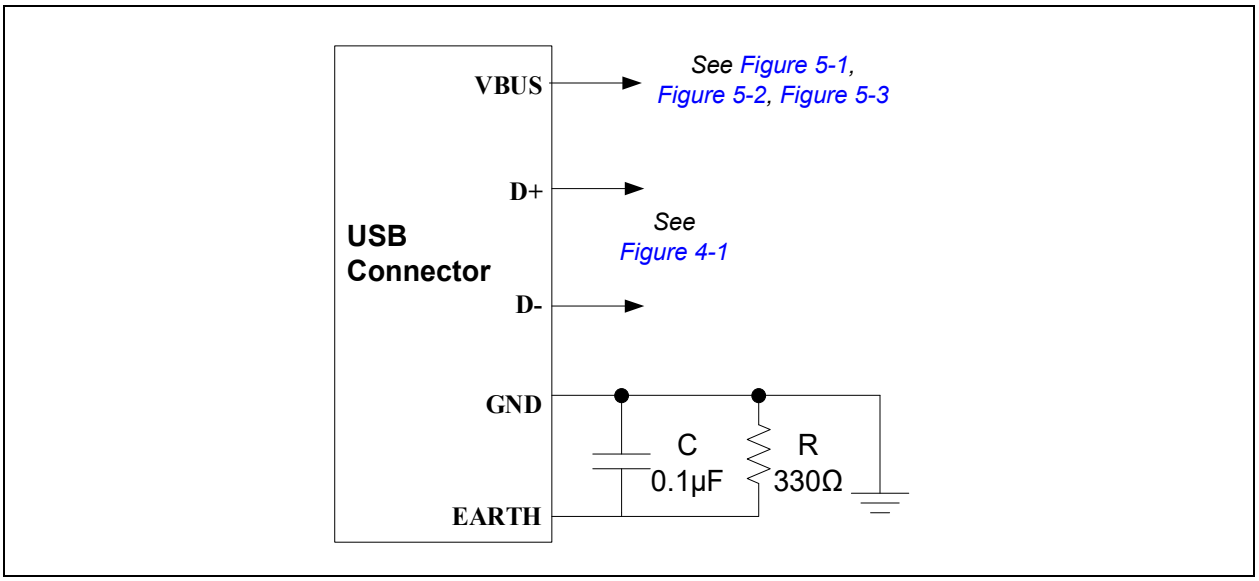
5.4 GND and EARTH Recommendations

- The **GND** pins of the USB connector must be connected to the PCB with a low-impedance path directly to a large **GND** plane.
- The **EARTH** pins of the USB connector may be connected with one of these two ways:

1. (Recommended) To **GND** through a resistor and capacitor in parallel. An RC filter can help to decouple and minimize EMI between a PCB and a USB cable.
2. Directly to the **GND** plane

The recommended implementation is shown in Figure 5-4.

FIGURE 5-4: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



6.0 CLOCK CIRCUIT

6.1 Crystal and External Clock Connection

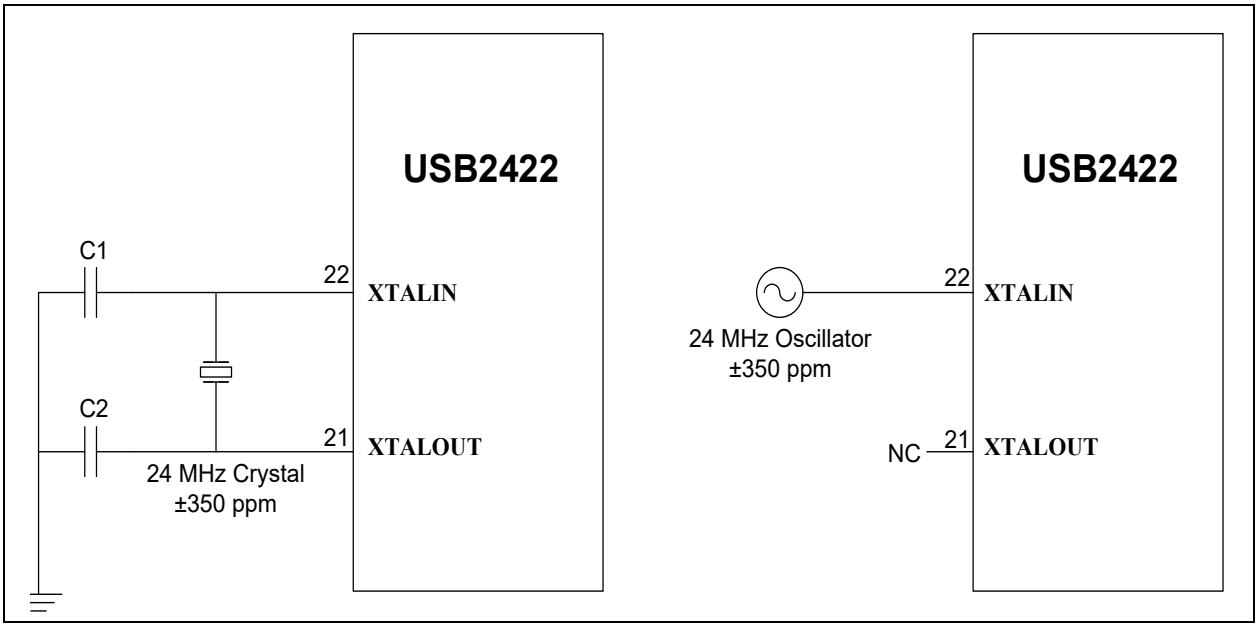
A 24.000 MHz (±350 ppm) reference clock is the source for the USB interface and for all other functions of the device. (See Figure 6-1.) For exact specifications and tolerances, refer to the latest revision of the *USB2422 Data Sheet*.

- **XTALIN** (pin 22) is the clock circuit input for the USB2422. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTALOUT** (pin 21) is the clock circuit output for the USB2422. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- The crystal loading capacitor values are system dependent based on the total C_L specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:
  - $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$
  - Where: CL is the spec from the crystal data sheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$

Note: C_{stray} is the stray or parasitic capacitance due to PCB layout. It can be assumed to be very small, in the 1 pF to 2 pF range, and then verified by physical experiments in the laboratory if PCB simulation tools are not available.

- Alternately, a 24.000 MHz, 1.2V to 3.3V clock oscillator may be used to provide the clock source for the USB2422. When using a single-ended clock source, **XTALOUT** (pin 21) should be left floating as a No Connect (NC).

FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS



7.0 POWER AND STARTUP

7.1 RBIAS Resistor

- **RBIAS** (pin 24) on the USB2422 must connect to ground through a 12 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close to the IC pin as possible, and be given a dedicated, low-impedance path to a ground plane.

7.2 Board Power Supplies

7.2.1 POWER RISE TIME

- The power rail voltage and rise time should adhere to the supply rise time specifications defined in the *USB2422 Data Sheet*.
- If a monotonic or fast power rail rise cannot be assured, then the RESET_N signal should be controlled by a Reset supervisor and only released when the power rail has reached a stable level.

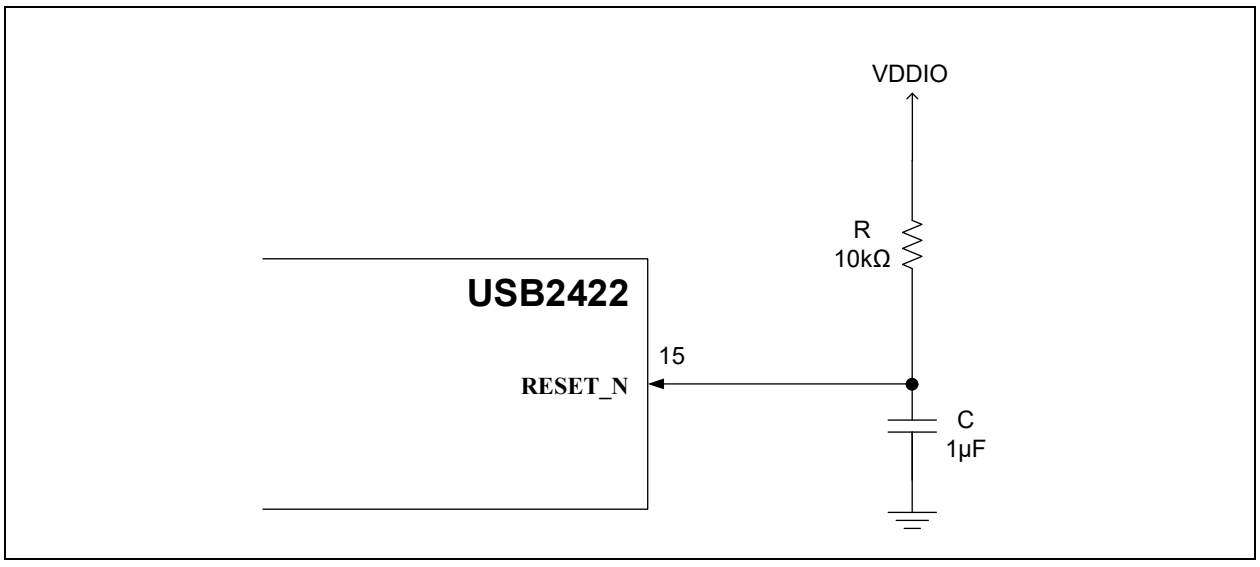
7.2.2 CURRENT CAPABILITY

- It is important to size the 5V and 3.3V power rails appropriately. The 5V power supply must be capable of supplying sufficient power for all exposed USB ports concurrently without drooping below the minimum voltage permissible in the USB specifications:
  - 500 mA per-port for USB2 Ports if BC1.1 is not enabled on the port
  - 1.5A per BC1.2-enabled port (if BC1.1 is enabled)
  - 1.5A or 3.0A per Type-C port (depending on the setting of the Type-C controller)
- The 3.3V power supply must be able to supply enough power to the USB hub IC. It is recommend that a 3.3V power rail be sized such that is able to supply the maximum power consumption specification, as displayed in the *USB2422 Data Sheet*.

7.3 Reset Circuit

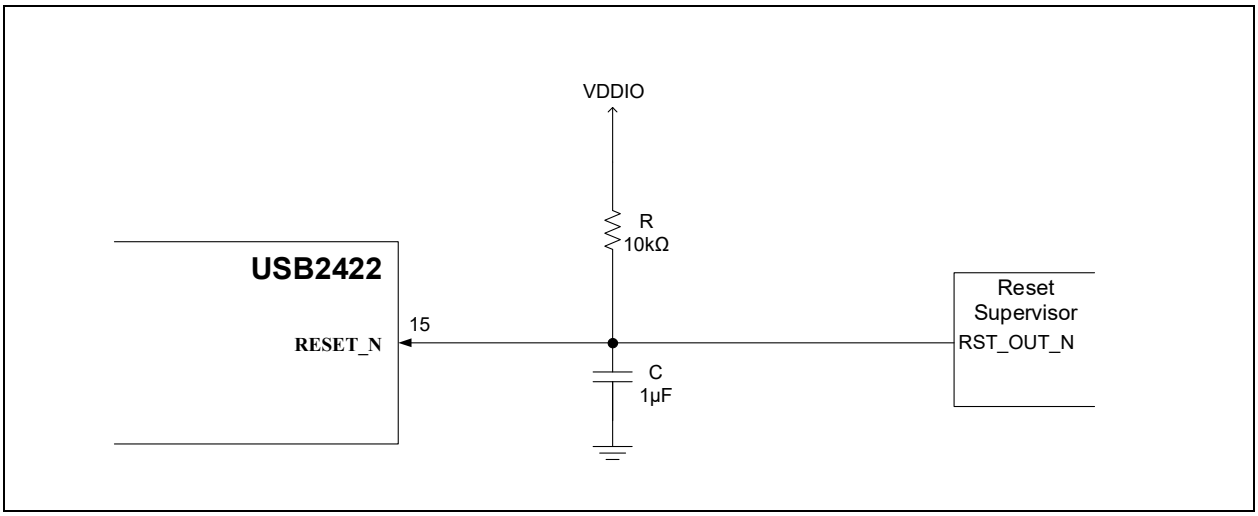
- **RESET_N** (pin 15) is an active-low Reset input. This signal resets all logic and registers within the USB2422. A hardware Reset (**RESET_N** assertion) is not required following power-up. Please refer to the latest copy of the *USB2422 Data Sheet* for Reset timing requirements.
- Figure 7-1 shows a recommended Reset circuit for powering up the USB2422 when a Reset is triggered by the power supply. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted based on individual system needs and preferences.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY



- Figure 7-2 details the recommended Reset circuit for applications where Reset is driven by an external CPU/MCU. The Reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm Reset after power-up. The values for the “R” resistor and “C” capacitor are not critical and my be adjusted based on individual system needs and preferences.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT



8.0 CONFIGURATION OPTIONS

- The USB2422 can be configured in one or two ways:
  1. SMBus (via external MCU/SOC)
  2. Hardware Resistor Straps (resistor pull-down/pull-up options)
- The hub must be configured completely via SMBus or hardware resistor straps. A combined or hybrid approach is not supported.

8.1 Configuration via MCU/SoC Memory

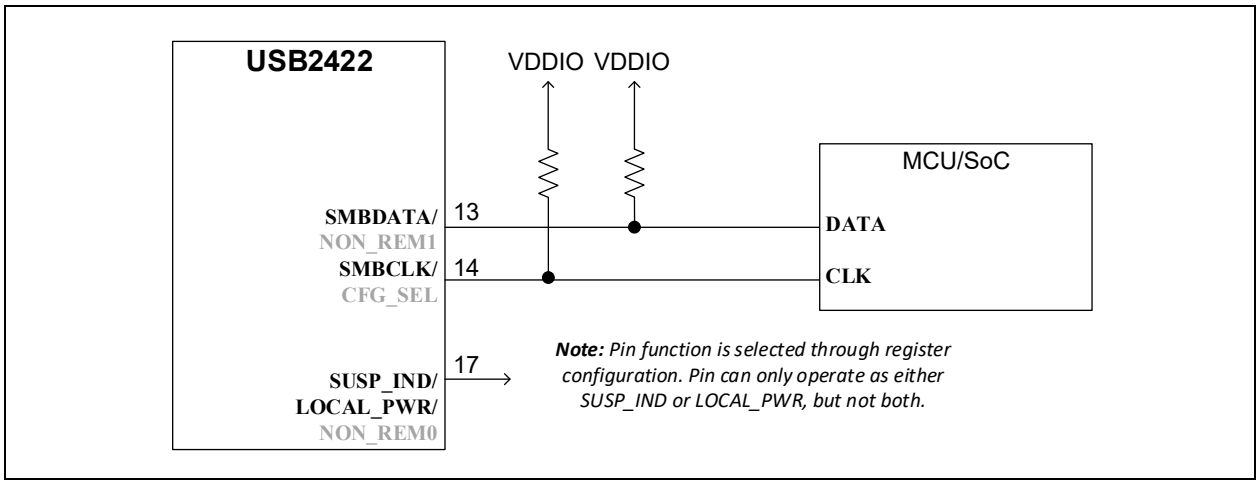
8.1.1 MCU/SOC OPERATION SUMMARY

- By default, the USB2422 executes based on internal register defaults, and an external MCU/SoC device is not explicitly required. If settings that differ from the internal defaults are required by the application, an external MCU/SoC may be used to modify the register settings. Only the specific settings which have to be modified from the default need to be changed.
- The USB2422 supports only one address option: 010_1100b

8.1.2 MCU/SOC CONNECTION DIAGRAMS

The recommended schematic connections for an MCU/SOC memory device are shown in Figure 8-1.

FIGURE 8-1: RECOMMENDED CONNECTIONS IF CONFIGURED VIA MCU/SOC



8.1.3 SELF-POWERED/BUS-POWERED SETTINGS (AVAILABLE VIA SMBUS CONFIGURATION ONLY)

- In a typical USB2422 application, the hub should be configured as self-powered, which is the default configuration setting. The following guidelines can be used to determine which setting to use:
  1. If the entire system (hub included) is powered completely from the upstream USB connector's **VBUS** pin and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is bus-powered.
  2. If the entire system (hub included) is always powered by a separate power connector, then the hub system is self-powered.
  3. If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely self-powered (even if all of the power is derived from the upstream USB connector's VBUS pin).
- The self-powered or bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors which the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host will typically limit the downstream ports of a self-powered hub to 100 mA. Any device connecting to a self-powered hub that needs more than 100 mA will be prevented from operating by the USB host.

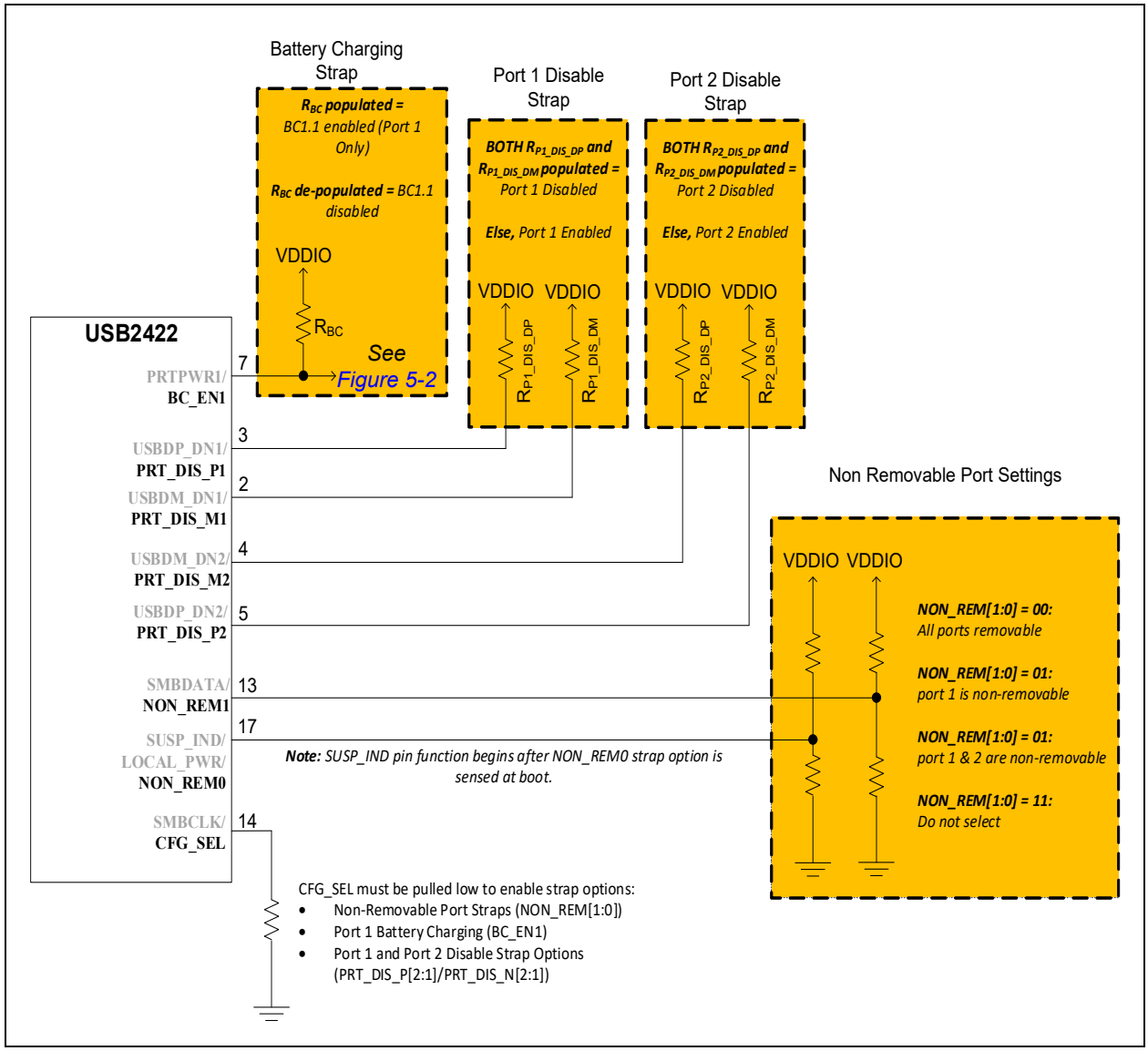
- The USB2422 also supports dynamic self-powered and bus-powered operation via the **LOCAL_PWR** control input pin. This feature must be enabled via SMBus configuration (DYNAMIC bit in CFG1 register). Once enabled, the **LOCAL_PWR** pin works as:
  1. 0: Self-powered, and no downstream port power restrictions will be in place.
  2. 1: Bus-powered – downstream port power restrictions will be enforced by the USB host.

The **LOCAL_PWR** cannot be changed dynamically. To change the mode of operation, the pin state must be changed, then the hub must be reset for the hub to communicate the new mode of operation descriptors to the USB host.

8.2 Configuration via Hardware Resistor Straps

Follow the schematic guidance in Figure 8-2 for strap configuration.

FIGURE 8-2: RECOMMENDED CONNECTIONS IF CONFIGURED VIA STRAP OPTIONS



8.2.1 BATTERY CHARGING SETTINGS

The USB2422 hub includes built-in battery charging support compliant to Charging Downstream Port (CDP) mode of the BC1.1 USB Battery Charging Specification. This allows portable device charging up to 1.5A with operational USB data. The feature is available on Port 1 only. Port 2 does not support BC1.1 operation. The BC_EN1 strap setting is sampled once at startup. The configuration strap options are described in Table 8-1.

TABLE 8-1: BC_EN1 CONFIGURATION STRAP OPERATION

Hardware Setting	Effect	Additional Notes
Floating or Pull-down to GND	All Ports - BC disabled	Battery Charging is not enabled. Select this option if configuration will be done via EEPROM or from an MCU/SOC via SMBus.
Pull-up to 3.3V	Port 1 BC enabled	Battery Charging is enabled on Port 1. See **Note 1**.

Note 1: Dedicated Charging Port (DCP) is not supported as the mechanism for a single port to switch between CDP and DCP modes was not introduced until the BC1.2 specification was released.

8.2.2 PORT DISABLE STRAPS

- If using the port disable strap option, the **USBDP_DNx** and **USBDM_DNx** signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net or through a pull-up resistor. The pins may also be shorted together to simplify the layout.

Note: Both USB D+ and D– signals must be pulled high to effectively disable the port. If only 1 pin is pulled to 3.3V, the port will not be disabled.

8.2.3 NON-REMOVABLE PORT SETTINGS

- In a typical USB2422 application, downstream ports are routed to a user-accessible USB connector and hence the downstream port should be configured as a removable port.
- The USB2422 has two configuration strap option pins, **NON_REM[1:0]**, which can be used to set the non-removable configurations for Ports 1 and 2. (See Table 8-2.) These are located on pins 13 and 17. The strap setting is sampled once at startup. A configuration strap option must be selected if the hub is not configured via EEPROM or from an MCU/SOC via SMBus.
- Note that the **SUSP_IND/LOCAL_PWR/NON_REM0** operates in the following manner when EEPROM or SOC-based SMBus configuration is not present:
  - During hub boot, the pin is sensed to determine the NON_REM0 setting.
  - During hub runtime, the pin operates as an output which reflects the suspend state of the hub:
    1. **Output Low (0V):** Hub is unconfigured (enumeration by the USB host is not complete) or in USB Suspend.
    2. **Output High (3.3V)**: Hub is configured (enumeration by the USB host is complete), and hub is active.

The LOCAL_PWR Output mode is not available. This pin function requires EEPROM or SOC-based SMBus configuration settings.

TABLE 8-2: NON_REM[1:0] SETTINGS

Setting	Effect
NON_REM1 = 0, NON_REM0 = 0	Ports 1 and 2 are removable.
NON_REM1 = 0, NON_REM0 = 1	Port 1 is non-removable. Port 2 is removable.
NON_REM1 = 1, NON_REM0 = 0	Ports 1 and 2 are non-removable.
NON_REM1 = 1, NON_REM0 = 1	Undefined setting. Do not select.

The following guidelines can be used to determine which setting to use:

1. If the port is routed to a user-accessible USB connector, it is removable.
2. If the port is routed to a permanently attached an embedded USB device on the same PCB or non-user-accessible wiring or cable harness, it is non-removable.
3. The removable and non-removable device settings do not have any impact on the hub's operations in any way. The settings only modify selected USB descriptors which the USB host may use to understand if a port is a user-accessible port, or if the device is a permanently attached device. Under standard operating conditions, the USB host may or may not modify its operations based on this information. Certain USB compliance tests are impacted by this setting, so designs required to undergo USB-compliance testing and certification must have correct configuration settings.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	Verify that the references are on hand.		
	Section 2.2, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.3, "Ground"	Verify that the grounds are tied together.		
	Section 2.4, "USB-IF Compliant USB Connectors"	Verify that USB-IF compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"		Ensure **VDD33** is within the range of 3.0V to 3.6V, 0.1 µF capacitors are connected to pins 1 and 18, and a 1.0 µF capacitor is connected to pin 9.		
		Ensure **CRFILT** has a 1.0 µF capacitor to **GND**.		
		Ensure **PLLFILT** has a 0.1 µF capacitor to **GND**.		
Section 4.0, "USB Signals"	Section 4.1, "USB PHY Interface"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
	Section 4.2, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
Section 5.0, "USB Connectors"	Section 5.1, "Upstream Port VBUS and VBUS_DET"	Verify that the Upstream Port VBUS has no more than 10 µF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub.		
	Section 5.2, "Downstream Port VBUS and PRTPWRx/OCSx_N"	If the downstream ports are standard Type-A ports, verify that **PRTPWRx** and **OCSx_N** are properly connected to the enable pin of the downstream port power controller and the Fault indicator output of the port power controller.		
	Section 5.3, "Downstream Port USB Type-C® Support"	If the downstream ports are standard USB Type-C® ports, verify that **PRTPWRx** is properly connected to the enable pin of the Type-C port controller, and **OCSx_N** is connected to the Fault indicator output of the port power controller.		
	Section 5.4, "GND and EARTH Recommendations"	Verify that the USB connector is properly connected to PCB ground on both the **GND** pins and the **SHIELD** pins. It is recommended that an RC filter be placed between the **SHIELD** pins and PCB ground.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 6.0, "Clock Circuit"	Section 6.1, "Crystal and External Clock Connection"	Confirm that the crystal or clock is 24.000 MHz (±350 ppm).		
		If a single-ended lock is used, ensure it is connected to **XTALI** while leaving **XTALO** floating.		
		If a crystal is used, ensure the loading capacitors are appropriately sized for the crystal loading requirement.		
Section 7.0, "Power and Startup"	Section 7.1, "RBIAS Resistor"	Confirm that a 12.0 kΩ 1% resistor is connected between the **RBIAS** pin and the PCB ground.		
	Section 7.2, "Board Power Supplies"	Verify that the board power supplies deliver 3.0V to 3.6V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet.		
		If the rise time requirement cannot be met, ensure that the **RESET_N** line is held low until the power regulators reach a steady state.		
	Section 7.3, "Reset Circuit"	Ensure that the **RESET_N** signal has an external pull-up resistor, or is otherwise properly controlled by an external SOC, MCU, or Reset supervisor device.		
Section 8.0, "Configuration Options"	Section 8.1, "Configuration via MCU/SoC Memory"	Determine which mode of configuration is required, and ensure that hardware is properly designed for either defaults, MCU/SoC configuration via SMBus, or Hardware Configuration Strap resistors.		
	Section 8.1.3, "Self-Powered/Bus-Powered Settings (Available via SMBus Configuration Only)"	If performing hub configuration via MCU/SOC, ensure the Self-Powered/Bus-Powered settings are correct, and hardware is designed appropriately.		
	Section 8.2, "Configuration via Hardware Resistor Straps"	Ensure the **RESET_N** is pulled to ground and that all other configuration strap pins are configured for the intended settings.		
	Section 8.2.1, "Battery Charging Settings"	Verify if the Battery Charging configuration strap is set via hardware properly (if configuring hub via Hardware Resistor Straps).		
	Section 8.2.2, "Port Disable Straps"	Verify if the Port Disable configuration straps are set via hardware properly (if configuring hub via Hardware Resistor Straps).		
	Section 8.2.3, "Non-Removable Port Settings"	Verify if the non-removable configuration straps are set via hardware properly (if configuring hub via Hardware Resistor Straps).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004196B (05-03-24)	Section 4.1, "USB PHY Interface"	Removed the statement, “This should not be wired to a user-accessible USB port,” from **USBDP_DN2** (pin 5) and **USBDM_DN2** (pin 4).
DS00004196A (09-20-21)	Initial release	

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