# TB3118

# Complementary Waveform Generator Technical Brief


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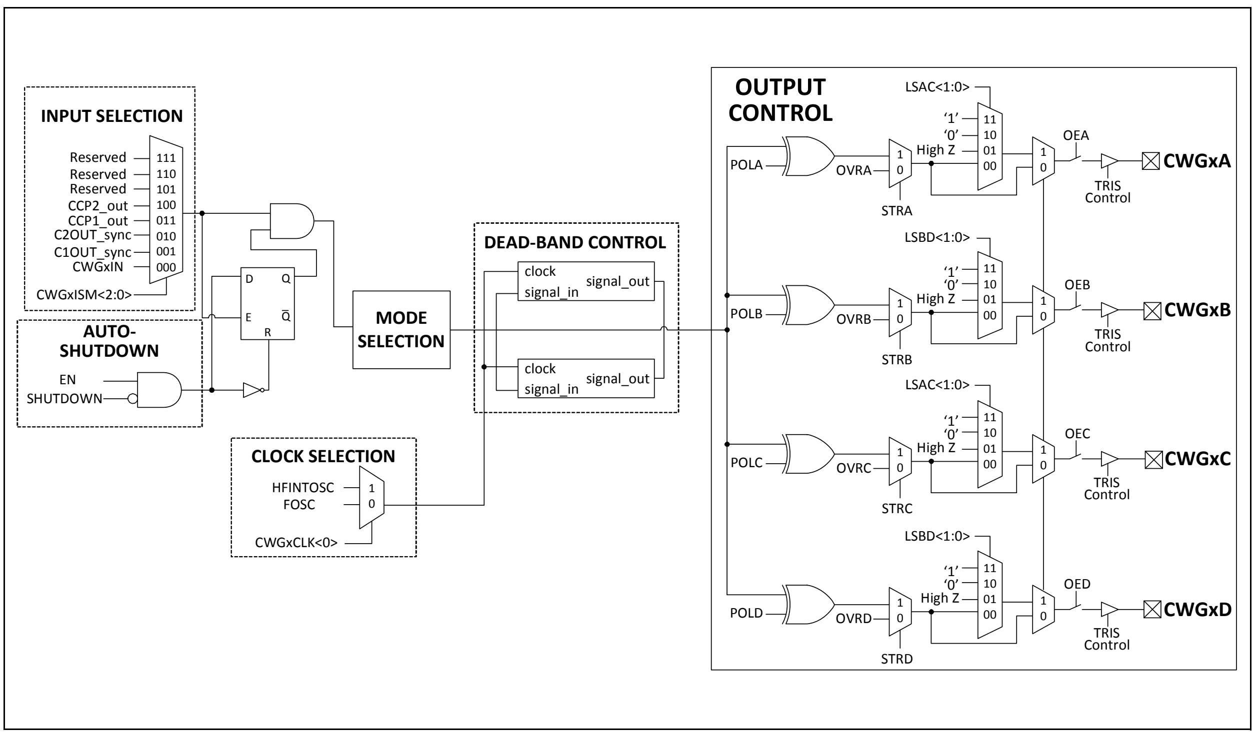
## INTRODUCTION

In applications that require precise half-bridge and full-bridge control, as in a motor driver application for example, a Complementary Waveform Generator with selectable input sources, dead-band control, polarity control, auto-shutdown and auto-recovery is desirable. The Complementary Waveform Generator (CWG) peripheral in Microchip's 8-bit microcontrollers can provide these advantages with no processor overhead. This document briefly describes the CWG features, the method of configuration and calculation of important values.

## BLOCK DIAGRAM

Figure 1 shows the simplified block diagram of the CWG peripheral. Each block in Figure 1 represents the CWG's features. The CWG generates a complementary output from one of several selectable input sources. The complementary output can be further modified in different modes of operation such as Push-Pull, Half-Bridge, Full-Bridge and Steering PWM. The clock source can be selected and used in order to insert a dead-band delay between the pair of complementary output waveforms. Each CWG output pin has individual output enable control and the polarity of these pins can be controlled individually as well. In addition, the CWG output can be terminated immediately during a Fault event and can also be recovered when the Fault event is removed.

**FIGURE 1: CWG SIMPLIFIED BLOCK DIAGRAM**



## INPUT SOURCE SELECTION

The CWG generates two complementary output waveforms from one of several selectable input sources. These input sources can be an external input to the CWGxIN pin or an output from other internal peripherals. The Input Source Selection bits (GxIS) are used in selecting the input source. CWG's input sources and bit selection settings may vary from device to device. Some of the available peripherals used as input sources are Comparator, CCP (Capture, Compare, PWM), NCO (Numerically Controlled Oscillator) and CLC Output (Configurable Logic Cell). The selected peripheral should be configured first before using it as CWG's input. For devices that have Peripheral Pin Select (PPS), the CWGxIN input pin can be moved to any other pin with the PPS Input Selection register (xxxPPS). By changing the "xxx" notation in the register name to CWGxIN, any available I/O pin can be selected as CWGxIN.

## MODE SELECTION

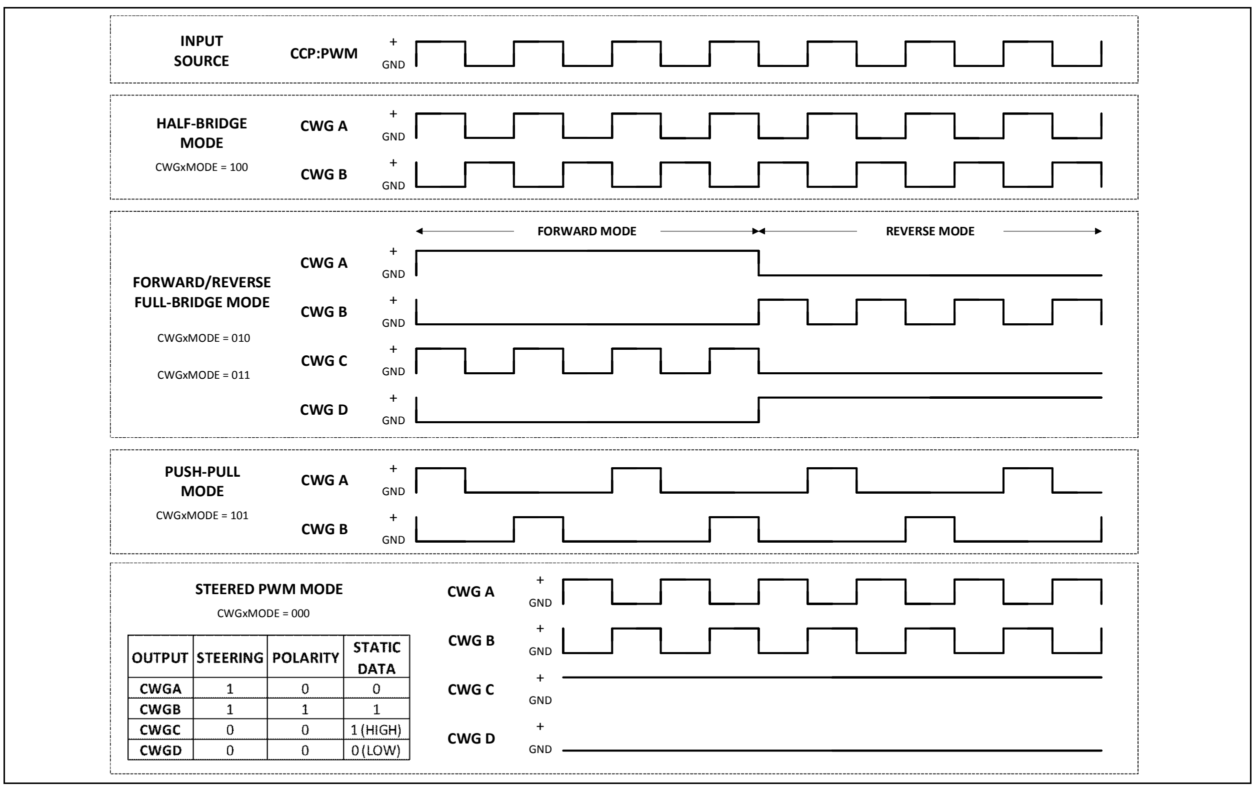
The CWG output can be modified to operate in several different modes. These modes are:

- Half-Bridge mode
- Forward Full-Bridge mode
- Reverse Full-Bridge mode
- Push-Pull mode
- Steering PWM mode

Mode Selection is only available in some device families. One of the device families that has this CWG feature is the PIC16F161X family. In this family, these modes can be selected by setting the CWG Mode Selection bits (CWGxMODE). Figure 2 shows the output of the CWG in different modes of operation for the PIC16F161X family.

In Half-Bridge mode, two output signals are generated as true and inverted version of the input. In Forward and Reverse Full-Bridge modes, three outputs drive static values while the fourth output replicates the input data signal. To change between Forward and Reverse Full-Bridge mode, toggling the MODE<0> bit of the CWGxCON0 register is required. In Push–Pull mode, the output signals generated are alternating copies of the input. In Steered PWM mode, enabling the Steering Enable bits (STRA:D) allows the input event signal to be replicated to any or all of the four CWG outputs (CWGxA:D). When Steering Enable bits (STRA:D) are cleared, the CWG output (CWGxA:D) signal is determined by the Steering Data bits (OVRA:D). When using a Synchronous Steering mode, the next rising input event is required, before the changes on the STRA:D bits take effect. While in Non-Synchronous Steering mode, changes on STRA:D bits take effect on the next instruction cycle.

**FIGURE 2: CWG MODES OF OPERATION**




| OUTPUT | STEERING | POLARITY | STATIC DATA |
|---|---|---|---|
| CWGA | 1 | 0 | 0 |
| CWGB | 1 | 1 | 1 |
| CWGC | 0 | 0 | 1 (HIGH) |
| CWGD | 0 | 0 | 0 (LOW) |

## CLOCK SOURCE SELECTION

The reference clock for the dead-band control can be selected from several different clock sources. This is possible by using the CWG Clock Selection bits (GxCS). Like the input sources, the available clock sources may vary from device to device.

When the selected clock source is HFINTOSC (16 MHz) and the input source selected remains active, the CWG can still operate even when the microcontroller is in Sleep mode.

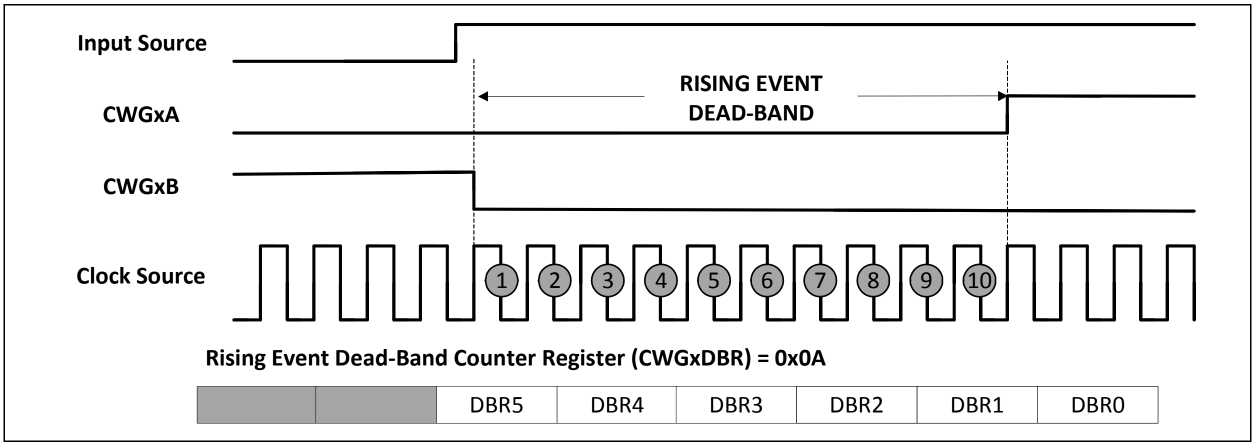
## DEAD-BAND CONTROL

The dead-band control provides non-overlapping output signals during Half-Bridge mode and changing direction during Full-Bridge mode.The non-overlapping signal prevents the cross conduction of external power switches. Dead-band control uses the selected clock source as a reference to create a delay. A maximum of a 6-bit value can be placed in the Rising Dead-Band Counter register (CWGxDBR) and the Falling Dead-Band Counter register (CWGxDBF) to indicate the count of clock delay periods.

## DEAD-BAND RISING EDGE CONTROL

In Figure 3, when CWGxB goes low, the rising edge dead band starts to count and delays the CWGxA for a 10-clock period before it goes high.

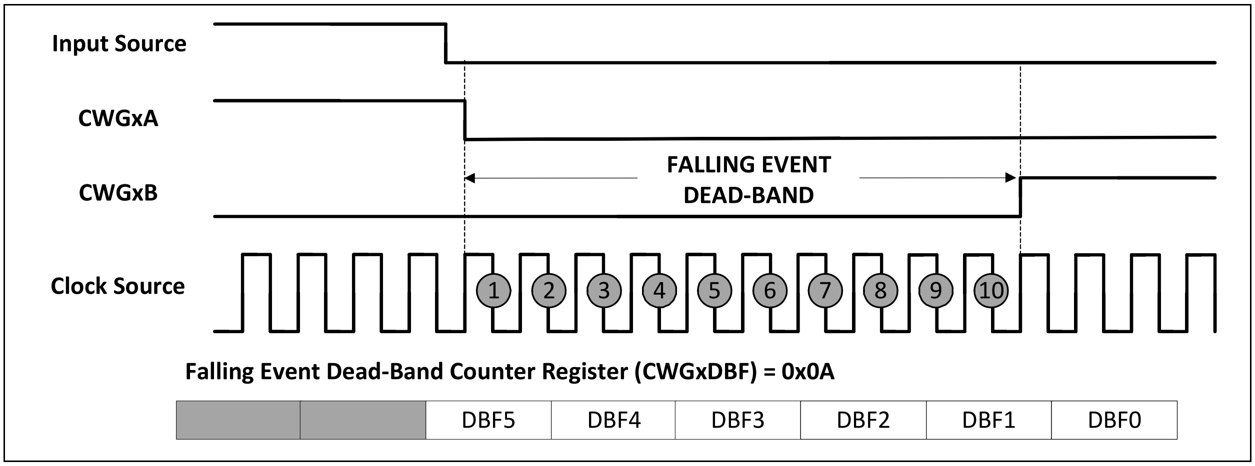
**FIGURE 3: RISING EVENT DEAD BAND**




## DEAD-BAND FALLING EDGE CONTROL

In Figure 4, when CWGxA goes low, the falling edge dead band starts to count and delays the CWGxB for a 10-clock period before it goes high.

**FIGURE 4: FALLING EVENT DEAD BAND**



The CWGxDBR and CWGxDBF are double-buffered registers. When CWG enable bit EN is ‘0’, the CWGxDBR and CWGxDBF registers are loaded right after writing to the CWGxDBR and CWGxDBF registers. When EN is ‘1’, the CWGxDBR and CWGxDBF registers are loaded on the next falling edge for the CWG input signal after setting the LD bit of the CWGxCON0 register. If the input source signal is not present long enough for the count to be completed, no output will be seen on the respective output.

## AUTO-SHUTDOWN

Auto-shutdown can be triggered by one of the available Fault event sources or by software execution. The Fault event source can be selected using the Auto-Shutdown Control register (CWGxAS1).

Auto-shutdown is an active-low operation. When the selected Fault event goes low, the output pin will be in shutdown state. The output pin shutdown state can be selected as forced-low, forced-high, tri-state or inactive by setting the Auto-Shutdown State Control bits (LSBD/LSAC). Also, setting the SHUTDOWN bit of the Auto-Shutdown Control register (CWGxAS0) in software will force the output into shutdown state.

The shutdown state can be held until cleared by the software or cleared automatically. Clearing the auto-shutdown automatically requires enabling auto-restart. Auto-restart can be enabled using the Auto-Restart Enable bit (REN).

## OUTPUT ENABLE

Each CWG output pin has individual output pin enable control. When an output pin enable bit is cleared, the CWG has no connection to the output pin. When the output enable is set, the override value or active waveform is applied to the pin per the internal port priority selection. The output control can be completely disabled by clearing the module enable bit. Output enables are selected in the CWG using the Output Enable bits (OEA:D). Setting the bit enables the output. By default, the complementary drive is configured as inactive in output CWGxA/C while the complementary drive is configured as active in output CWGxB/D.

Some devices allow CWG output to be moved to its alternate pins. Using the Alternate Pin Function register (APFCON), the CWG output function can be moved between its default and alternate pins.

For the devices that have Peripheral Pin Select (PPS), there is no output control available. Instead, each device pin has an individual output selection controlled by the PPS register. When the output is not selected in the PPS register, the peripheral has no connection to the output pin.

## POLARITY CONTROL

Polarity control can be set to invert the output signal. The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output will become active-low. Clearing the output polarity bit configures the corresponding output as active-high. Inverting the polarity of the output signal would allow Output A or Output B to output the exact same signal. Output polarity are selected using the Output Polarity bits (GxPOLA:D).

## DEAD-BAND TIME CALCULATION AND UNCERTAINTY

Dead band is timed by counting the clock periods from zero up to the value in its respective count registers. The exact dead-band time is calculated using Equation 1.

**EQUATION 1: TIME CALCULATION**

$$Time_{(min)} = \frac{Count}{Frequency_{(Clock\ Source)}}$$

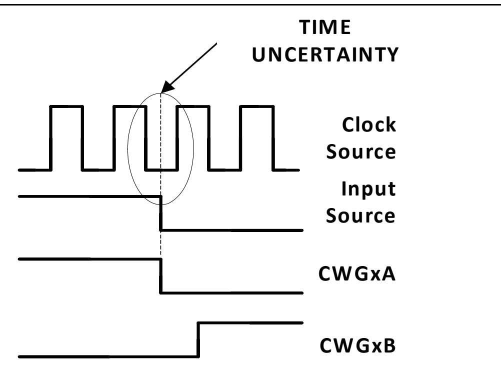
$$Time_{(max)} = \frac{Count + 1}{Frequency_{(Clock\ Source)}}$$

**Where:**

| TIME | COUNT |
|---|---|
| Rising Dead-Band | CWGxDBR |
| Falling Dead-Band | CWGxDBF |

There are instances when the time calculation may not be accurate every time. This is referred to as time uncertainty as shown in Figure 5.

**FIGURE 5: TIME UNCERTAINTY**




When the rising and falling sources that trigger the dead-band timer come from asynchronous inputs, such as the external input to CWGxIN pin, it creates an uncertainty in the time. Time uncertainty can be calculated using Equation 2.

**EQUATION 2: TIME UNCERTAINTY CALCULATION**

$$Time_{(uncertainty)} = Time_{(max)} - Time_{(min)}$$

$$Time_{(uncertainty)} = \frac{1}{Frequency_{(Clock\ Source)}}$$

## CONFIGURING CWG USING MICROCHIP MPLAB® CODE CONFIGURATOR (MCC)

In this section, the MPLAB® Code Configurator (MCC) is utilized to easily configure the CWG module. The MCC is a user-friendly plug-in tool for MPLAB® X IDE, which generates drivers for controlling and driving peripherals of PIC® microcontrollers, based on the settings and selections made in its Graphical User Interface (GUI). For installation and setup of the MCC in MPLAB® X IDE, refer to the *"MPLAB® Microchip Code Configurator User Guide"* which can be found at www.microchip.com.

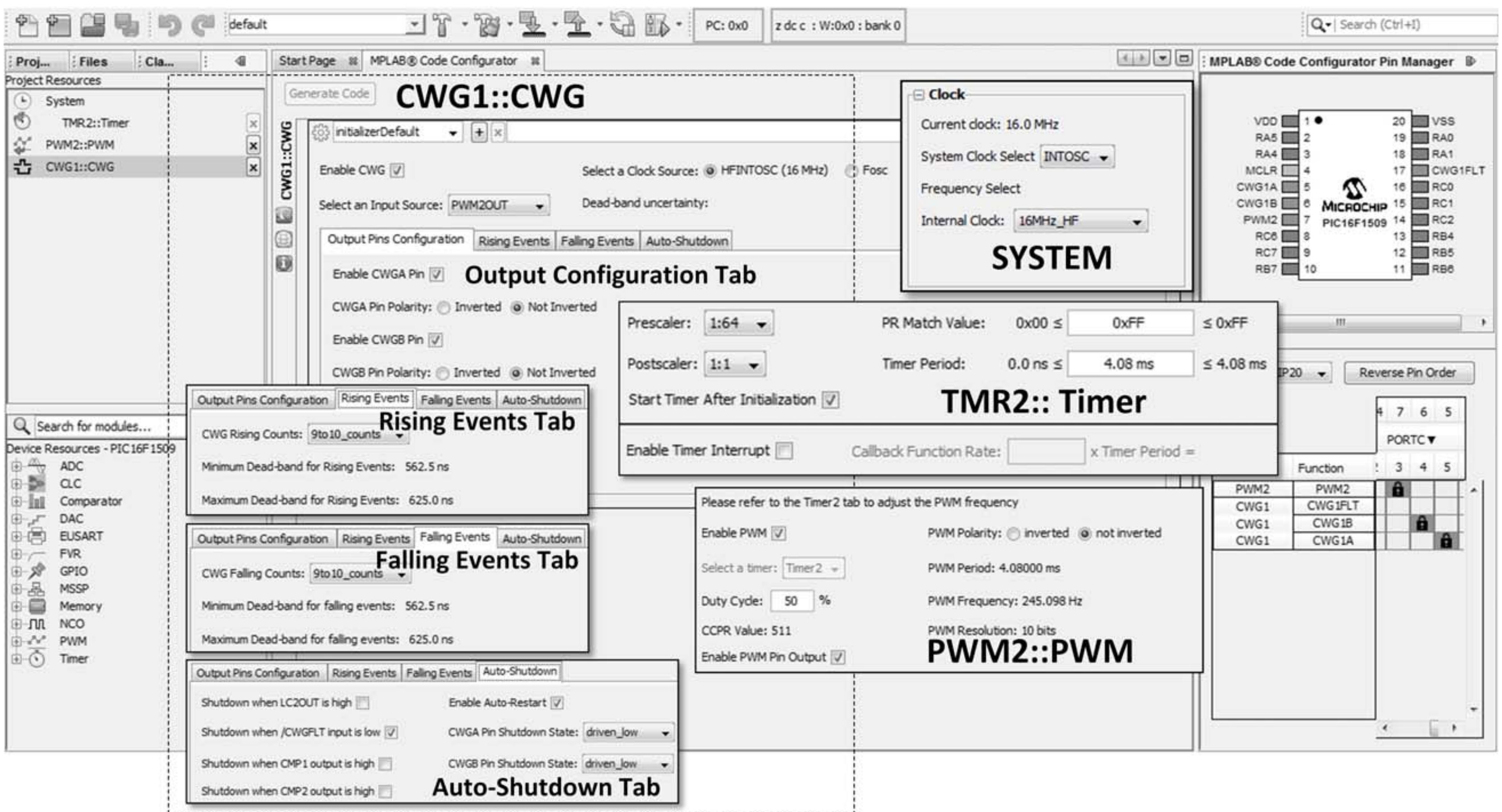
The following steps will guide on how to configure the CWG module in PIC16F1509 using the MCC. The CCP's Pulse-Width Modulation (PWM) output signal, running at 50% duty cycle, is used as the input source and the High-Frequency Internal Oscillator (HFINTOSC) is used as the dead-band reference clock. After a successful configuration, the CWG produces two complementary waveform outputs which can be terminated using an active-low external switch connected in CWGxIN for shutdown control.

1. Navigate to: "**Tools – Embedded – MPLAB Code Configurator**" to launch the MCC.
2. Set the desired Configuration registers and the system clock source on the "**System**" label inside of MPLAB X in the "**Project Resources**" window.
3. Configure the input source to be used:

- **PWM Configuration**
  - Under the device resources panel. Expand "**PWM**" and then double-click on "**PWM2**" to bring the module up to the "**Project Resources**" panel.
  - In the center panel, after clicking the "**PWM2::PWM**" in the "**Project Resources**" window, set the duty cycle to 50% and Timer2 as timer source. When Timer2 is selected as timer source for CCP1, the configurator will automatically add it in "**Project Resources**".
- **Timer2 Configuration**
  - In the center panel, after clicking the "**TMR2::Timer**" in the "**Project Resources**" window, set the Prescaler to 1:64 in the drop-down menu and the "**PR Match Value**" to 0xFF.
  - Check the "**Start Timer After Initialization**" check box.

4. After configuring the CCP, CWG can now be configured by bringing the module up to the "**Project Resources**" panel. The following instructions will configure the CWG.
5. In the center panel, after clicking the "**CWG1::CWG**" in the "**Project Resources**" window, check the "**Enable CWG**" checkbox to enable CWG. Select the "**PWM2OUT**" as input source in the "**Select an Input Source**" drop-down menu.
6. Select HFINTOSC (16 MHz) as the reference clock source for the dead-band timer.
7. Under the "**Output Pins Configuration**" tab, check the "**Enable CWGA Pin**" and "**Enable CWGB Pin**" to enable both outputs.
   - Choose the "**Non-Inverted**" checkbox on both CWGA and CWGB to disregard polarity change on the outputs.
8. Under the "**Auto-Shutdown**" Tab, check the "**Shutdown when CWGFLT input is low**" and "**Enable Auto-Restart**" checkbox to activate the auto-shutdown and restart feature. To avoid shutdown, drive the CWGFLT (RA2) pin to high.
   - Set the "**CWGA Pin Shutdown State**" and "**CWGB Pin Shutdown State**" to "**driven_low**" in the drop-down menu.
9. In configuring the dead-band control under the "**Rising Event**" and "**Falling Event**" tab, select "**9 to 10_counts**" as the CWG Rising/Falling counts.
10. Click the "**Generate Code**" button in the top left corner of the center panel. This will generate a main.c file to the project automatically. It will also initialize each module and leave an empty while(1) loop for custom code entry. See Figure 6 for the User Interface of CWG in MCC and Example 1 for the generated initialization code for the CWG module.

**FIGURE 6: MCC USER INTERFACE FOR CWG**



**EXAMPLE 1: MCC GENERATED INITIALIZATION CODE FOR CWG**



```
void CWG1_initializerDefault(void)
{
    // Set the CWG to the options selected in MPLAB® Code Configurator
    // Writing to CWGxCON0, CWGxCON1, CWGxCON2, CWGxDBR & CWGxDBF registers
    // G1ASDLA driven_low; G1IS PWM2OUT; G1ASDLB driven_low;
    CWG1CON1 = 0xA3;
    // G1ASDSCLC2 disabled; G1ASDSC2 disabled; G1ASDSC1 disabled;
    // G1ARSEN enabled; G1ASDSFLT enabled; G1ASE no_auto_shutdown;
    CWG1CON2 = 0x42;
    // CWG1DBR 9to10_counts;
    CWG1DBR = 0x09;
    // CWG1DBF 9to10_counts;
    CWG1DBF = 0x09;
    // G1EN enabled; G1OEA enabled; G1OEB enabled; G1CS0 HFINTOSC;
    // G1POLA normal_polarity; G1POLB normal_polarity;
    CWG1CON0 = 0xE1;
}
```

**TABLE 1: SUMMARY OF 8-BIT MICROCONTROLLER FAMILIES FEATURING THE CWG MODULE**

| Family | Input Sources | Clock Sources | Shutdown Sources | Modes |
|---|---|---|---|---|
| PIC10(L)F3XX | LC1OUT<br>NCO1OUT<br>PWM2<br>PWM1 | HFINTOSC<br>FOSC | LC1OUT<br>CWG1FLT (CWG1IN) | n/a |
| PIC1X(L)F150X | CLC1OUT<br>NCO1OUT<br>PWM4<br>PWM3<br>PWM2<br>PWM1 | HFINTOSC<br>FOSC | C2<br>C1<br>CLC2<br>CWG1FLT (CWG1IN) | n/a |
| PIC16(L)F145X | PWM2<br>PWM1<br>C1<br>C2 | HFINTOSC<br>FOSC | C2<br>C1<br>CWG1FLT (CWG1IN) | n/a |
| PIC1X(L)F157x | PWM3<br>PWM2<br>PWM1<br>C1 | HFINTOSC<br>FOSC | C1<br>CWG1FLT (CWG1IN) | n/a |
| PIC1X(L)F1612/3 | CCP2<br>CCP1<br>C2<br>C1<br>CWG1IN | HFINTOSC<br>FOSC | TMR6<br>TMR4<br>TMR2<br>C2<br>C1<br>CWG1FLT (CWG1IN) | Half-Bridge<br>Full-Bridge<br>Push-Pull<br>Steering mode |

## CONCLUSION

This technical brief briefly covers the CWG peripheral features and capabilities. It also provides the calculations of relevant value such as dead-band time. The configuration of CWG is demonstrated using code configurator MCC and example initialization code is generated using MCC as well.

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