Device Configuration

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all dsPIC33/PIC24 devices.

Please consult the note at the beginning of the **"Special Features"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

1.0 INTRODUCTION

At their highest level of functionality, dsPIC33/PIC24 devices integrate several features that affect the entire device as a whole. They add convenience and flexibility of design for the user, and allow the devices to be incorporated into a wider range of designs. These include:

- Flexible Configuration Options – Allowing users to select a wide range of basic microcontroller operating options and changing them if needed during run time
- Device Identification – Allowing electronic confirmation of a device part number and revision level in the target application

2.0 DEVICE CONFIGURATION

The basic behavior and operation of dsPIC33/PIC24 devices are set by the device Configuration bits. These bits allow the user to select a wide range of options and optimize the microcontroller's operation to the application's requirements.

In all dsPIC33/PIC24 family devices, device Configuration bits are mapped to the device's program memory space.

The method by which the Configuration bits are programmed differs between major device families. The details are discussed in **Section 2.1 "Volatile Memory Implementation"** and in **Section 2.2 "Nonvolatile Memory Implementation"**. Refer to the specific device data sheet for information on which method is implemented for your particular device.

Table 2-1 provides a list of the most common Configuration bit options. Note that this is not a comprehensive list. Certain device families will have unique configuration options that are specific to its peripheral set. For more information on the Configuration bit mapping of a particular device, refer to the specific device data sheet.

Note: All of the bits that are described in Table 2-1 are not present on all the devices. Refer to the specific device data sheet for availability.

Table 2-1: Common dsPIC33/PIC24 Device Configuration Bits

Configuration Bit	Function
GSS	Enables General Segment code protection.
BSS	Enables Boot Segment code protection.
CSS	Enables Configuration Segment protection.
FNOSC	Selects the initial (default) device oscillator (three bits, up to eight configuration options).
FWDTEN	Enables the Watchdog Timer.
WDTPRE	Watchdog Timer Prescaler Select bits (1:128 and 1:32).
WDTPOST	Watchdog Timer Postscaler Select bits (1:1 through 1:32,768).
IESO	Enables Two-Speed Start-up.
IOL1WAY	Selects one-time or unrestricted run-time changes to peripheral mapping.
JTAGEN	Enables dedicated JTAG port and disables corresponding I/O ports on designated pins.
OSCIOFNC	Selects function of OSC2 pin (I/O port or CLKO) in certain External Oscillator modes.
POSCMD	Selects Primary (external) Oscillator configuration (2 bits, 4 configurations).
FCKSM	Configures device clock switching and Fail-Safe Clock Monitor (2 bits, 3 configuration options).
SOSCEL	Selects Secondary Oscillator power option.
CTXTx	Specifies the alternate register set association with Interrupt Priority Levels (IPL).

2.1 Volatile Memory Implementation

In certain dsPIC33/PIC24 devices, the Configuration bits are implemented as volatile memory; that is, the configuration data must be loaded each time the device is powered up. The actual configuration data is stored in the last several words at the end of the on-chip program memory space, known as User Space. During all types of device Resets, the configuration data is automatically loaded from the Flash Words to the proper Configuration registers. Refer to the specific device data sheet for implementation details.

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various configuration options. To prevent inadvertent configuration changes during code execution, all programmable device Configuration bits are write-once. After a bit is initially written, it cannot be written to again.

2.1.1 CONSIDERATIONS WHEN USING FLASH CONFIGURATION WORDS

Flash Configuration Words are 24-bits (three bytes) wide. However, depending on the device and register, all three bytes may not be implemented.

Erasing the last page of program memory (User Memory Space) will automatically enable code protection, which prevents further reads or writes to program memory. As a result, it is not recommended to perform a page erase on the last page of memory where the Configuration bits are stored.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration Words for configuration data in their code for the compiler. This is to make certain that program code is not stored in these addresses when the code is compiled.

Table 2-2 lists the Flash Configuration registers, including their primary function and memory locations, depending on the Flash size for dsPIC33EP(16/32/64)GS50X devices.

Table 2-2: Flash-Based Configuration Register Map for dsPIC33EP(16/32/64)GS50X Devices

Register	ADR (16k)	ADR (32k)	ADR (64k)	Primary Function
FSEC	0x2B80	0x5780	0xAF80	Code Protection Configure
FBSLIM	0x2B90	0x5790	0xAF90	Boot Segment Address Limit
FOSCSEL	0x2B98	0x5798	0xAF98	Oscillator Select
FOSC	0x2B9C	0x579C	0xAF9C	Oscillator Configure
FWDT	0x2BA0	0x57A0	0xAFA0	Watchdog Timer Configure
FPOR	0x2BA4	0x57A4	0xAFA4	Reset Configure
FICD	0x2BA8	0x57A8	0xAFA8	Debug Configure
FDEVOPT	0x2BAC	0x57AC	0xAFAC	Peripheral Pin Mapping
FALTREG	0x2BA4	0x57A4	0xAFA4	Alternate W Registers IPL Configure
FBTSEQ	0x2BFC	0x57FC	0xAFFC	Panel Sequence Number

Table 2-3 lists the Flash Configuration registers, including their primary function and memory locations, depending on the dsPIC33E/PIC24E device Flash size.

Table 2-3: Flash-Based Configuration Register Map for dsPIC33EP/PIC24E devices

Register	ADR (32k)	ADR (64k)	ADR (128k)	ADR (256k)	ADR (512k)	Primary Function
FICD	0x57F0	0xAFF0	0x157F0	0x2AFF0	0x557F0	Debug Configure
FPOR	0x57F2	0xAFF2	0x157F2	0x2AFF2	0x557F2	Reset Configure
FWDT	0x57F4	0xAFF4	0x157F4	0x2AFF4	0x557F4	Watchdog Timer Configure
FOSC	0x57F6	0xAFF6	0x157F6	0x2AFF6	0x557F6	Oscillator Configure
FOSCSEL	0x57F8	0xAFF8	0x157F8	0x2AFF8	0x557F8	Oscillator Select
FGS	0x57FA	0xAFFA	0x157FA	0x2AFFA	0x557FA	General Code Protection

Note: Refer to the specific device data sheet for Configuration register availability.

2.2 Nonvolatile Memory Implementation

With nonvolatile memory implementation, the Configuration bits are implemented as a physically separate block of nonvolatile memory. Once programmed, configuration data is maintained indefinitely. Although they act like fuses, the Configuration bits are freely reprogrammable. Since they lie inside the configuration memory space, the Configuration bits are not directly accessible; they can only be written and read using Table Read (TBLRD) and Table Write (TBLWT) instructions.

Unlike volatile memory implementation devices, the Configuration bits with nonvolatile memory implementation devices are organized into 8-bit registers that are always the Least Significant Byte (LSB) of a program memory address. These Configuration registers are symbolically named according to their primary function (i.e., General Segment protection, Oscillator Selection, and so on). Table 2-4 lists the names and addresses of typical Configuration registers. Note that not all Configuration registers are implemented on all devices and certain devices with extended feature sets may have additional registers. In addition, there may be variations in naming or location of registers in certain devices. Refer to the specific device data sheet for more information.

The Configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various configuration options.

The implementation of the Configuration bits in devices using nonvolatile memory implementation makes a Configuration Mismatch (CM) Reset and error, during full-speed operation, virtually impossible. However, a severe device disturbance (such as an ESD event) during Sleep may disrupt the configuration safety check, resulting in a CM Reset.

Table 2-4: Typical Configuration Registers

Register Name	Address	Primary Function
FGS	0xF80004	General Segment Protect
FOSCEL	0xF80006	Oscillator Select
FOSC	0xF80008	Oscillator Configure
FWDT	0xF8000A	Watchdog Timer Configure
FPOR	0xF8000C	Reset Configure
FICD	0xF8000E	Debug Configure

3.0 DEVICE IDENTIFICATION

dsPIC33/PIC24 devices have two read-only registers that provide device-specific identification information. These are located near the end of the program memory space. The Device ID registers are 24 bits wide and the upper 8 bits are unimplemented. Both registers can be read using Table Read instructions.

The DEVID register identifies the Microchip microcontroller architectural family and the specific part number. The DEVREV register identifies the particular silicon revision for that device in terms of major and minor revision levels (“letter and dot revision” format).

For any given family of dsPIC33/PIC24 devices, the corresponding Family Silicon Errata and Data Sheet Clarification document provides a list of values for DEVID and the corresponding part numbers for that family. The association of the value of DEVREV to a revision level is different for each part number. The translation of a DEVREV value to a revision level can be found in the associated Family Silicon Errata and Data Sheet Clarification document.

Register 3-1: DEVID: Device ID Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVID15	DEVID14	DEVID13	DEVID12	DEVID11	DEVID10	DEVID9	DEVID8
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVID7	DEVID6	DEVID5	DEVID4	DEVID3	DEVID2	DEVID1	DEVID0
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as ‘0’

bit 23-16 **Unimplemented:** Read as ‘0’

bit 15-0 **DEVID<15:0>:** Device ID Value bits

Register 3-2: DEVREV: Device Revision Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVREV15	DEVREV14	DEVREV13	DEVREV12	DEVREV11	DEVREV10	DEVREV9	DEVREV8
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVREV7	DEVREV6	DEVREV5	DEVREV4	DEVREV3	DEVREV2	DEVREV1	DEVREV0
bit 7							bit 0

Legend:	
R = Readable bit	U = Unimplemented bit, read as ‘0’

bit 23-16 **Unimplemented:** Read as ‘0’

bit 15-0 **DEVREV<15:0>:** Device Revision Value bits

4.0 UNIT IDENTIFICATION

Some devices may feature programmable Unit ID registers (FUIDx), which can be programmed by the user with unique device information. Refer to the specific device data sheet for FUIDx availability and memory locations.

5.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 Product Family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Device Configuration include the following:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33/PIC24 family of devices.

6.0 REVISION HISTORY

Revision A (November 2009)

This is the initial released version of this document.

Revision B (July 2010)

This revision includes major updates that have been incorporated throughout the document.

Revision C (June 2011)

This revision includes the following updates:

- Updated all paragraphs of **2.1 “Volatile Memory Implementation”** and replaced references to Configuration Words with Configuration Bytes
- Removed section 30.5 “In-Circuit Programming and Debugging”
- Changes to formatting and minor text updates were incorporated throughout the document

Revision D (August 2013)

This revision includes the following updates:

- Added Table 2-1 and Table 2-2
- Updated Register 3-1 and Register 3-2
- Minor text updates and major formatting changes were incorporated throughout the document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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