SmartFusion2 MSS

ARM® Cortex™-M3 Configuration

Microsemi

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Introduction

The ARM® Cortex™-M3 offers configurable features as well as available signals at the FPGA fabric interface.

The values entered in the configurator will be exported into the programming files for programming of the flash bits that control this functionality. The flash bits are loaded in the system registers at power up (or when the DEVRST_N external pad is asserted/de-asserted).

For complete details about the ARM® Cortex-M3 feature set offered in the SmartFusion2 devices please refer to the Microsemi SmartFusion2 User's Guide.

1 – Configuration Options

Memory Protection Options

Use Memory Protection Unit - Select this option to enable the MPU block (Figure 1-1).

***Figure 1-1* • MPU Configuration**

Sys Tick Timer

Calibration Register - The calibration register - STCALIB - is a 26-bit register that determines the rollover value for the internal SysTick timer to the Cortex-M3 microcontroller.

STCLK - Configure the STCLK frequency as a division (4, 8, 16 or 32) of M3_CLK. This must be configured so that STCLK is less than half the frequency of M3_CLK. The division factor is loaded into the STCLK_DIVISOR register (Figure 1-2).

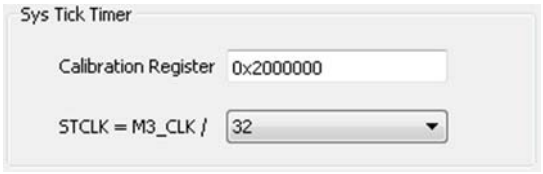

***Figure 1-2* • Sys Tick Timer**

Events

You can expose the Cortex-M3 RXEV and TXEV signals at the FPGA fabric (Figure 1-3).

***Figure 1-3* • RXEV and TXEV FPGA Fabric Interface Configuration**

System Power Management

The Cortex-M3 provides various power modes. M3_CLK is gated off when in SLEEPING or SLEEPDEEP mode. SLEEPING and SLEEPDEEP signals are available at the FPGA fabric interface. Sleep mode extension handshake signals are available at the FPGA fabric interface. Use the System Power Management options to expose these signals to the FPGA fabric (Figure 1-4).

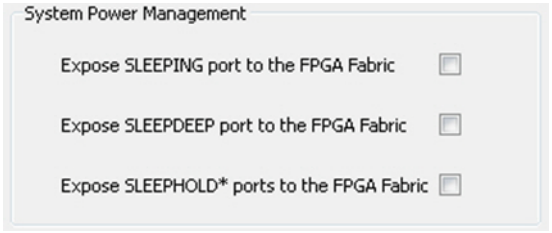

***Figure 1-4* • System Power Management FPGA Fabric Interface Configuration**

Trace Port Interface Unit (TPIU)

The TPIU signals TRACECLK and TRACEDATA[3:0] signals can be exposed to the FPGA fabric (Figure 1-5). You can also select whether the TRACECLK is M3_CLK/2 (check box off) or M3_CLK/4 (check box on).

***Figure 1-5* • TPIU FPGA Fabric Interface Configuration**

2 – Port Description

Table 2-1 **• Port Description**

Port Name	Direction	PAD ?	Description
RXEV	In	No	Causes the Cortex-M3 to wake up from a WFE (wait for event) instruction. The event input, RXEV, is registered even when not waiting for an event, and so affects the next WFE.
TXEV	Out	No	Event transmitted as a result of a Cortex-M3 SEV (send event) instruction. This is a single-cycle pulse equal to 1 M3_CLK period.
SLEEP	Out	No	Signal is asserted when the Cortex-M3 is in sleep now or sleep-on-exit mode, and indicates that the clock to the processor can be stopped.
DEEPSLEEP	Out	No	Signal is asserted when the Cortex-M3 is in sleep now or sleep-on-exit mode when the SLEEPDEEP bit of the System Control Register is set.
SLEEPHOLD*			TBD
TRACECLK	Out	No	TBD
TRACEDATA[3:0]	Out	No	TBD

A – Product Support

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From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

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Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

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Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

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The technical support email address is soc_tech@microsemi.com.

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