

ATMEL®'S AT91SAM7S SERIES OF ARM®-BASED FLASH MICROCONTROLLERS AIM TO BRIDGE THE GAP BETWEEN 8- AND 32-BIT MICROCONTROLLER APPLICATIONS. IN PARTICULAR THEY FOCUS ON REAL-TIME CONTROL APPLICATIONS THAT REQUIRE FEATURES TRADITIONALLY INCORPORATED INTO 8-BIT MCUS (NOTABLY A DETERMINISTIC RESPONSE TO COMMANDS AND INTERRUPTS) TOGETHER WITH THE SUPERIOR PROCESSING POWER AND EXTENDED ADDRESS SPACE OF 32-BIT MCUS. THIS ARTICLE REVIEWS THE GENERAL ARCHITECTURE OF THE AT91SAM7S SERIES AND GIVES DETAILS OF THE UNIQUE FEATURES THAT ATMEL HAS BUILT INTO THESE PRODUCTS IN ORDER TO ENSURE A DETERMINISTIC RESPONSE TO AN EXTERNAL EVENT: A GUARANTEED RESPONSE WITHIN A SPECIFIED TIME INTERVAL.

Atmel's ARM-based Flash μ Cs Optimized for Real-Time Control Applications

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AT91SAM7S Architecture and Real-Time Control Features

As shown in Figure 1, Atmel's AT91SAM7S series microcontrollers are built around a 32-bit ARM7TDMI® processor core and on-chip Flash and SRAM memories. Flash memory densities range from 32K to 512-kbytes. An integrated Flash Programmer facilitates programming (or re-programming) of the Flash memory as required. A memory lock bit, when set, makes it impossible to read the Flash memory by an external device, in order to protect valuable application code and sensitive data.

The System Controller includes a Brownout Detector and Power On Reset controller to ensure power-down

and power-up without accidental (or deliberate) corruption of data or code. A Voltage Regulator enables the device to be supplied by a single 3.3 V supply and a Power Management Controller can put the processor and any combination of peripherals into idle mode when they are not in use in order to minimize power consumption.

The rich peripheral set of the AT91SAM7S features a USB V2.0 full speed device for PC connectivity, and a number of peripherals adapted for real-time control. These include a Pulse Width Modulator, several Timers and Timer/Counters supported by on-chip Oscillators and a Phase Locked Loop, and an 8-channel 10-bit ADC. A Parallel I/O Controller multiplexes peripheral I/Os with a set of general-purpose I/O lines in order to reduce the pin count and provide flexibility of external access.

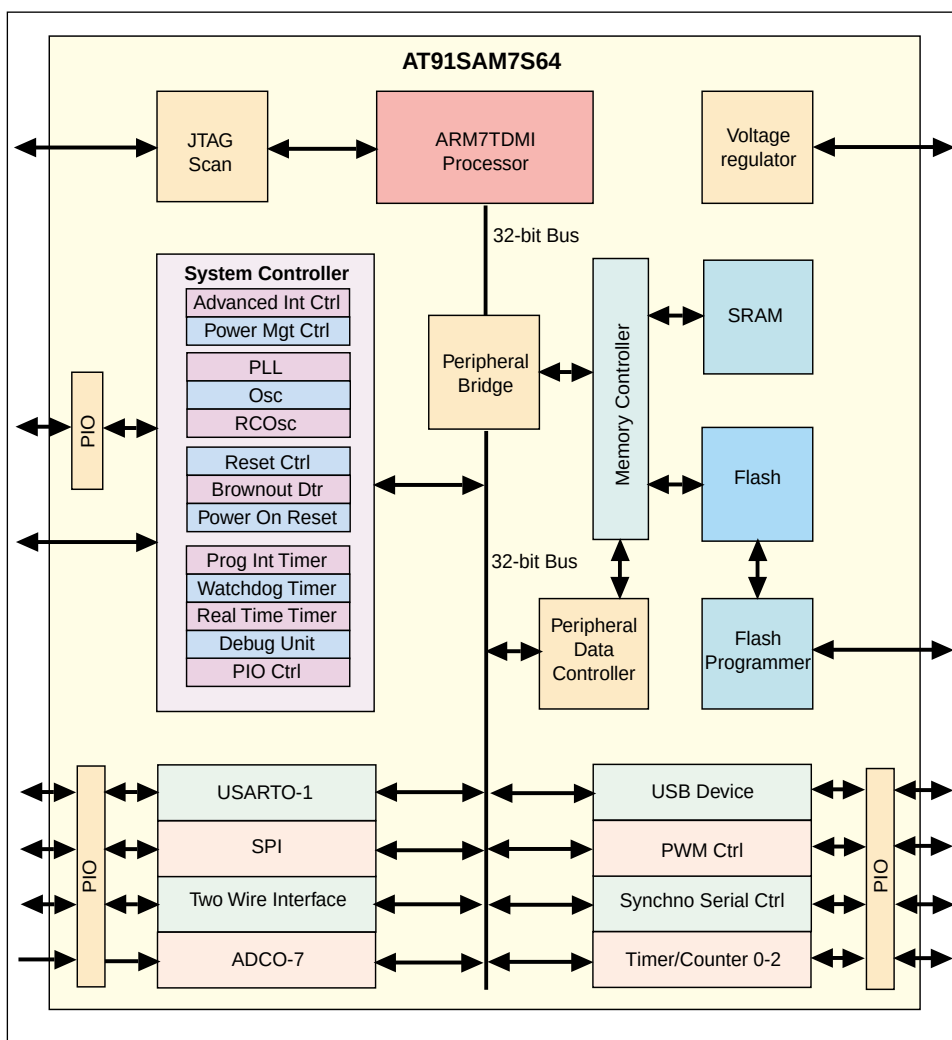
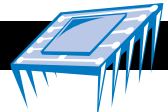


Figure1: AT91SAM7S Architecture



Single-Cycle Code Access from Flash Memory

The limiting deterministic performance of a fast processor running code from memory is established by the single-cycle access time of the memory. (Cache memories cannot be used where deterministic performance is mandatory.) Atmel's integrated high-speed Flash memory is capable of single-cycle access in 33 ns, giving maximum deterministic performance by the ARM7TDMI processor of 27 MIPS. This is a significant improvement over 8-bit MCU performance under deterministic conditions.

Rapid Interrupt Handling

Real-time control applications are typically interrupt-driven, with a response required within a specified time to each external event. Atmel has significantly enhanced the basic interrupt structure of the ARM7TDMI processor in order to provide an interrupt handling capability that meets this requirement. The Advanced Interrupt Controller (AIC) controls the two interrupt lines of the ARM7 processor (normal and fast interrupt). It provides a set of individually maskable, vectored interrupt sources with 8-level priority. One source is for the fast interrupt request, one is for the system peripherals and the remainder are for interrupts

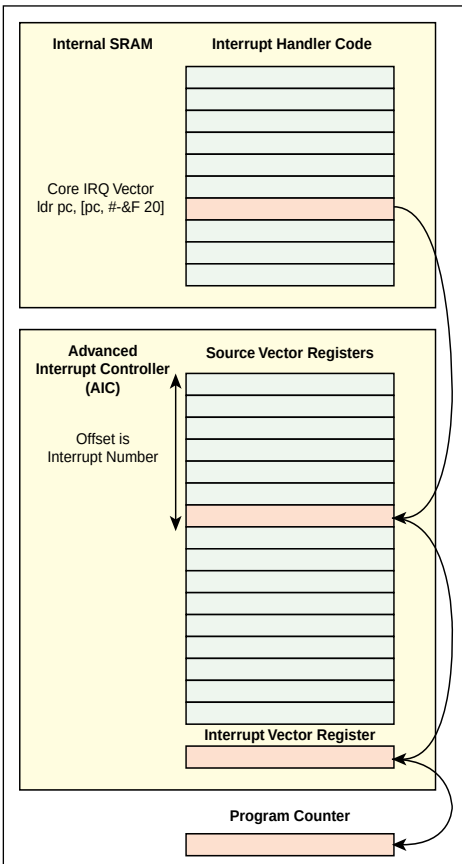


Figure 2: AT91SAM7S Advanced Interrupt Controller

from peripherals or external sources. The basic interrupt handler, permanently stored in SRAM, resolves interrupt priorities and then executes an instruction that uses the interrupt number as an offset to load the vector for the required interrupt service routine directly into the Program Counter (Figure 2). This simple, robust mechanism ensures the transfer of control to the required interrupt service routine in the minimum number of instruction cycles.

Single-Cycle Bit Set and Reset

Control applications frequently require individual bit set/reset operations, but the basic ARM7 processor architecture requires that this be accomplished by a read-modify-write sequence of operations that requires interrupt masking (itself a bit set/reset operation) to ensure that the entire sequence is carried to completion once it has started. To overcome this shortcoming, Atmel has provided the AT91SAM7S series with an atomic bit set/reset facility that works in the same way for all the peripheral control/monitoring registers.

As shown in Figure 3, complementary Enable and Disable Registers are connected by RS flip-flops to each Status Register. A bit is set in the Status Register by writing 1 to the corresponding bit position in its Enable Register (writing a zero has no effect). Writing a 1 in the Reset register clears the corresponding bit in the Status Register.

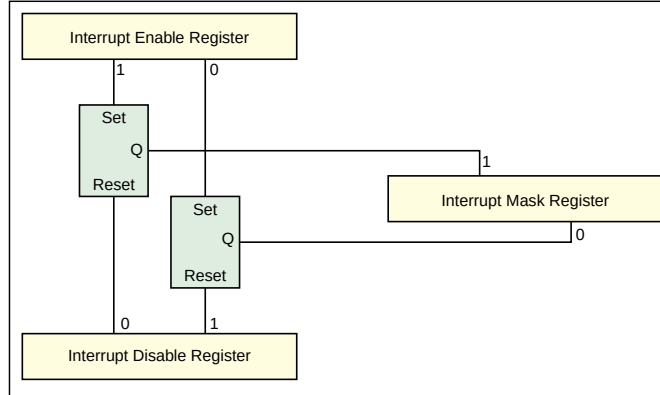


Figure 3: AT91SAM7S Register Bit Set/Reset Mechanism

This provision, commonly found in 8-bit microcontrollers, reduces bit manipulation to a single instruction executed in a single clock cycle. It reduces code size (by approximately 60% for the instruction sequence concerned) and speeds program execution.

Peripheral Data Controller for Direct Memory Access

Many of the AT91SAM7S peripherals are designed to transfer blocks of data between SRAM and an external communications channel (USART, Debug Unit, SSC, SPI and ADC). In order to carry out these transfers as efficiently as possible, Atmel has incorporated a Peripheral

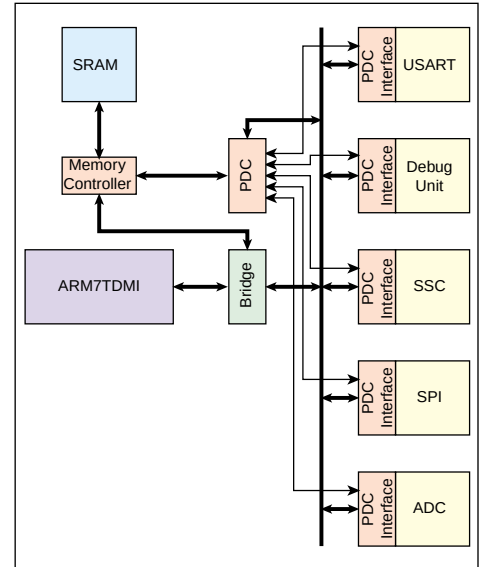


Figure 4: AT91SAM7S Peripheral Data Controller

Data Controller (PDC) into the AT91SAM7S architecture that provides a direct memory access (DMA) function.

The PDC (Figure 4) manages the transfer of blocks of data between SRAM and these serial peripherals with minimum processor overhead. On the one hand this reduces the programming requirement for data transfers to writing or updating the contents of the appropriate PDC Interface registers, and on the other hand the transfer time for blocks of data is considerably reduced.

The transfer of successive blocks can be chained to avoid generating unnecessary interrupts until the entire transfer is complete. These features significantly enhance the real-time performance of the AT91SAM7S.

Conclusion

The AT91SAM7S series incorporates a number of architectural features that bring the real-time

control capabilities of 8-bit microcontrollers into the 32-bit arena with hardly any price adder. Most of these features are Atmel enhancements to the basic ARM7TDMI architecture, with the common aim of providing deterministic performance at a clock speed and data throughput significantly higher than can be achieved with 8-bit microcontrollers. At the same time these devices achieve a commendably low power consumption while driven from a single-voltage supply, and protect valuable application code and reference data.

Further information can be obtained from Atmel's Web site at www.atmel.com.