ENT-AN1055

Application Note

IEEE 1588 and SyncE Clock Design

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

In revision 2.0 of this document, formatting was updated.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

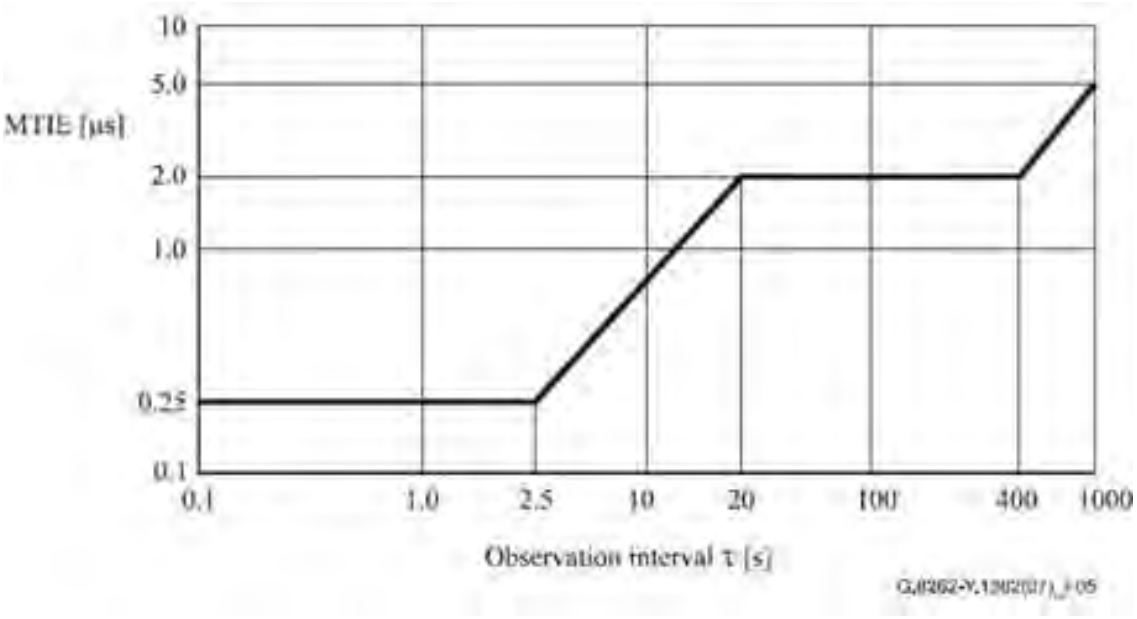
2 IEEE 1588 and SyncE Clock Design

This application note describes how to design a system with both IEEE 1588v2 PTP and Synchronous Ethernet (SyncE). This is not intended to provide a detailed description but rather highlight the importance of having separate clock domains for IEEE 1588 and SyncE.

2.1 The Problem

In synchronous Ethernet networks, all nodes are locked to a central clock source and all signals are transmitted using this clock. In systems where the IEEE 1588 uses the same clock, any wander on the SyncE clock generates wander on the 1588 network. The allowed wander for SyncE is specified in ITU-T G.8262, as shown in the following illustration.

Figure 1 • SyncE Wander Tolerance



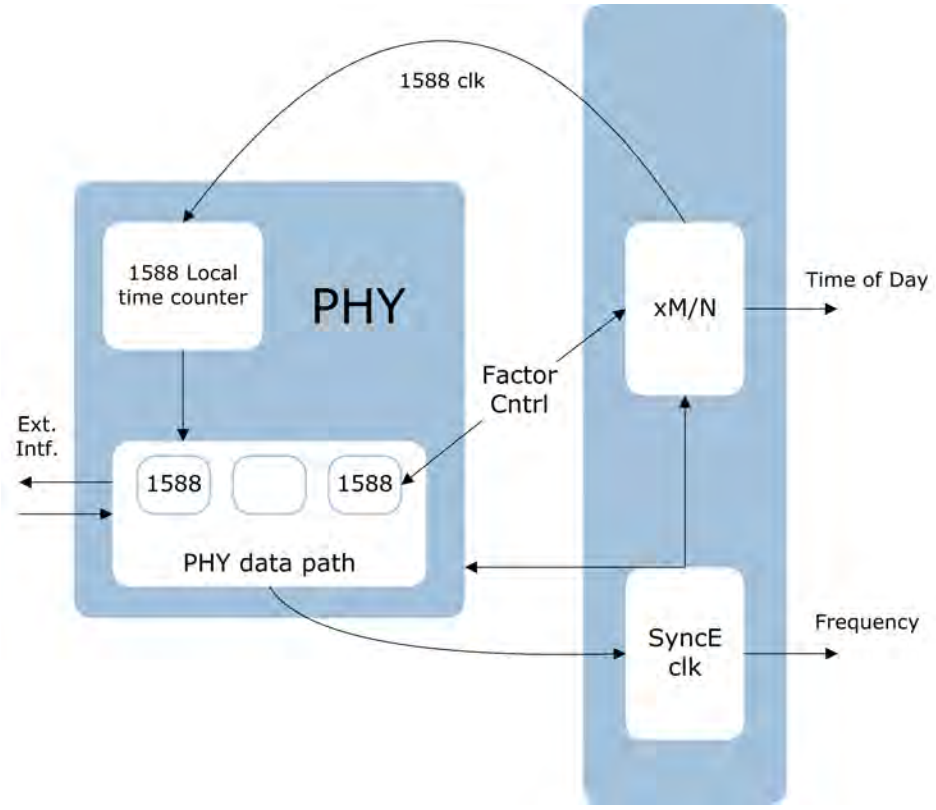
An offset of up to 250 ns per sec is allowed, which could be generated by a reference clock switchover. This offset is allowed and no alarm is raised, but it will transfer directly to the 1588 clock. With a PTP frame rate of 1 packet per second, this will result in a PTP time error of 250 ns.

In a design with common clock domains for IEEE 1588 and SyncE (EEC), the received clock is used to drive a SyncE PLL that again drives the transmission clocks and the 1588 local time counter.

An advantage of using the derived SyncE clock is that the normally high quality SyncE reference clock is used for the 1588 clock, relaxing the requirement for the local oscillator. However, wander on the SyncE clock generates wander on the 1588 clock.

The following illustration shows IEEE 1588 and SyncE with a common clock domain.

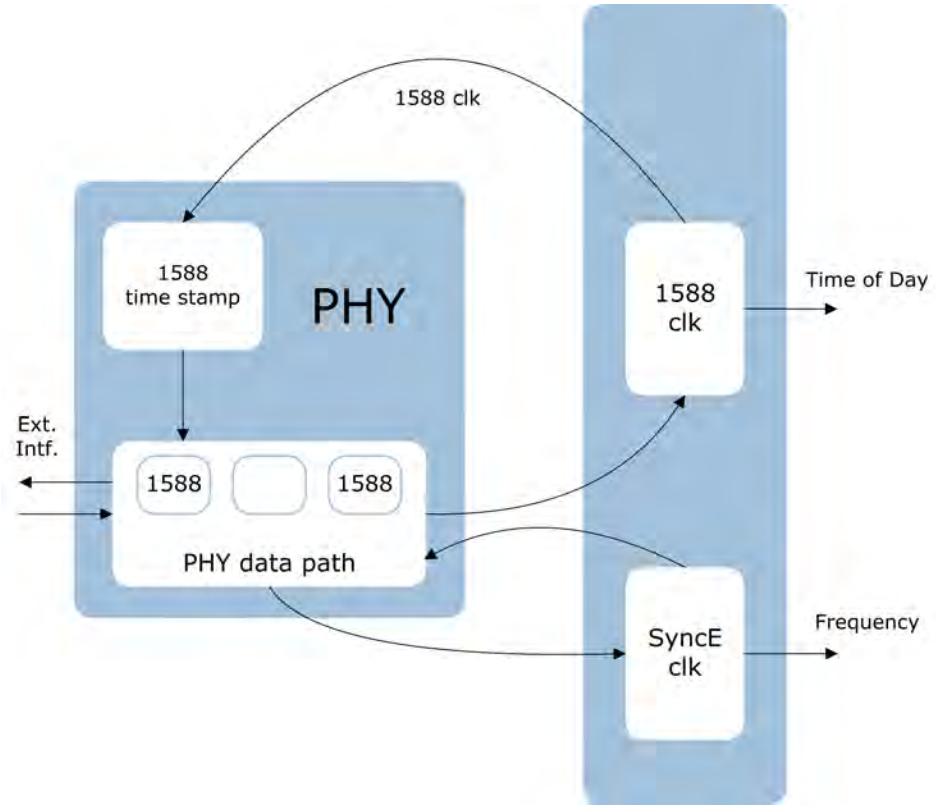
Figure 2 • IEEE 1588 and SyncE with a Common Clock Domain



2.2 The Solution

The solution is simply to use separate clock domains for 1588 and for SyncE, as shown in the following illustration.

Figure 3 • IEEE 1588 and SyncE with Separate Clock Domains



The derived clock from the selected clock source port is used by the SyncE PLL and this clock is used to drive all transmit clocks on the node. The 1588 uses a separate local clock for timestamping and time of day counter.

In this setup, any wander on the SyncE clock will not influence the 1588 clock and there are two independent ways to distribute synchronization.

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