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Supporting 100BASE-FX Fiber Media for Microchip's Ethernet Controller, Switch, and EtherCAT® Controller

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INTRODUCTION

Microchip provides design solutions targeted to support next generation Ethernet switches, EtherCAT® industrial controllers, and 10/100 Industrial Ethernet MAC/PHY controllers. The Ethernet switch products are divided into host bus and MII categories with the host bus versions supporting a full-featured Ethernet MAC residing behind the switch fabric. The non-host bus versions support various MII, RMII, and Turbo MII options with 1- and 2-port options.

Table 1 lists the various products available.

TABLE 1: MICROCHIP ETHERNET CONTROLLER, ETHERNET SWITCH, AND ETHERCAT® CONTROLLER PRODUCTS

Part Number	Description
LAN9250	10/100 Industrial Ethernet Controller and PHY
LAN9252	2-/3-Port EtherCAT Slave Controller with Integrated Ethernet PHYs
LAN9352	2-Port 10/100 Managed Ethernet Switch with 16-Bit Non-PCI CPU Interface
LAN9353	3-Port 10/100 Managed Ethernet Switch with Single MII/Turbo MII or Dual RMII
LAN9354	3-Port 10/100 Managed Ethernet Switch with Single RMII
LAN9355	3-Port 10/100 Managed Ethernet Switch with Dual MII/RMII/Turbo MII

This document highlights the design differences needed to implement 100BASE-FX fiber media on Microchip's Ethernet controller, switch, and EtherCAT controller.

Sections

This document includes the following topics:

Feature Differences for 100BASE-FX

EtherCAT® Over Optical Links (FX) — Applicable Only for LAN9252

Support for Copper Mode and Fiber Mode for LAN9252 ESC

Audience

The target audiences for this document are hardware design engineers and managers using Microchip's Ethernet controller, switch, and EtherCAT controller in a 100BASE-FX application.

References

The following documents should be referenced when using this application note. See your Microchip representative for availability.

- *LAN9250 Data Sheet*
- *LAN9252 Data Sheet*
- *LAN9352/LAN9354/LAN9355 Data Sheet*
- *LAN9355 Data Sheet*

Terms and Abbreviations

- CPLD - Complex Programmable Logic Device
- EEE - Energy Efficient Ethernet
- ESC - EtherCAT® Slave Controller
- FEF - Far-End-Fault
- FOT - Fiber Optics Transceiver
- LOS - Loss of Signal
- LVPECL - Low-Voltage Positive/Pseudo Emitter-Coupled Logic
- MAC - Media Access Control
- MII - Media Independent Interface
- PHY - Physical layer device
- RMII - Reduced Media Independent Interface
- SD - Signal Detect
- SFF - Small Form Factor
- SFP - Small Form-Factor Pluggable
- SMI - Serial Management Interface

FEATURE DIFFERENCES FOR 100BASE-FX

This section describes the hardware and software differences for a designer to implement the new 100BASE-FX fiber media in Microchip's Ethernet controller, switch, and EtherCAT controller.

Hardware Details

100BASE-FX is supported via external fiber transceiver.

When set for 100BASE-FX operation, the scrambler and MLT-3 blocks are disabled, and the analog receive (RX) and transmit (TX) pins are changed to differential LVPECL pins and are connected through external terminations to the external fiber transceiver. The differential LVPECL pins support a signal voltage range compatible with Small Form Factor or SFF (LVPECL) and Small Form-Factor Pluggable or SFP (reduced LVPECL) type transceivers.

While in 100BASE-FX operation, the quality of the RX signal is provided by the external transceiver as either an open-drain, CMOS-level, Loss of Signal (SFP) or an LVPECL Signal Detect (SFF).

100BASE-FX ENABLE AND LOSS OF SIGNAL (LOS) OR SIGNAL DETECT (SD) SELECTION

100BASE-FX operation is enabled using the FX mode straps (fx_mode_strap_1 and fx_mode_strap_2) and is reflected in the 100BASE-FX mode (FX_MODE) bit in the PHY x Special Modes Register (PHY_SPECIAL_MODES_x).

The Loss of Signal (LOS) mode is selected for both PHYs using the three-level FXLOSEN strap input pin. The three levels correspond to LOS mode for: neither PHY (less than 1V [typical]), PHY A (greater than 1V [typical] but less than 2V [typical]), or both PHYs (greater than 2V [typical]). It is not possible to select LOS mode for only PHY B.

If LOS mode is not selected, then Signal Detect (SD) mode is selected independently by the FXSDENA or FXS-DENB strap input pin. When LVPECL is greater than 1V (typical), SD mode is enabled, and when less than 1V (typical), twisted-pair copper is enabled.

Note:	The FXSDENA strap input pin is shared with the FXSDA pin, and the FXSDENB strap input pin is shared with the FXSDB pin. As such, the LVPECL levels ensure that the input is greater than 1V (typical) and that SD mode is selected. When twisted-pair copper is desired, the SD input function is not required and the pin should be set to 0V.

Make sure that a non-powered or disabled transceiver does not load the SD input below the valid LVPECL level.

TABLE 2: 100BASE-FX LOS, SD, AND TWISTED-PAIR COPPER SELECTION PHY A

FLXLOSEN	FXSDENA	PHY Mode
< 1V (typical)	< 1V (typical)	Twisted-pair copper
	> 1V (typical)	100BASE-FX SD (SFF)
> 1V (typical)	N/A	100BASE-FX LOS (SFP)

TABLE 3: 100BASE-FX LOS, SD, AND TWISTED-PAIR COPPER SELECTION PHY B

FLXLOSEN	FXSDENA	PHY Mode
< 1V (typical)	< 1V (typical)	Twisted-pair copper
	> 1V (typical)	100BASE-FX SD (SFF)
> 2V (typical)	N/A	100BASE-FX LOS (SFP)

Signal Detection

Signal Detect (SD) requires single-ended 3.3V LVPECL levels and supports SFF optical module. SD is used to determine normal operation and detect optical signaling.

SD is a logical complement of LOS.

- Single-Ended LVPECL
  - SD > VLVPECL_COMMON_MODE - Normal operation, optical signaling detected
  - SD < VLVPECL_COMMON_MODE - No optical signal detected
- 50Ω Single-Ended Impedance

Loss of Signal

Loss of Signal (LOS) requires CMOS levels and supports the SFP optical module. LOS is an Open Drain or Collector. LOS is a logical complement of SD.

- LOS < 0.8V - Normal operation, optical signaling detected
- LOS > 2.0V - No optical signal detected

LOS is an Open Drain/Collector output, which should be pulled up with a 4.7-10 kΩ resistor.

CONNECTION TO 100BASE-FX FIBER MODULE

The FX mode enables the 10/100 Mbps Ethernet PHY transport data over fiber optics medium using Fiber Optics Transceivers (FOT). The FX mode supports two form factors running at 100 Mbps. The SFF module can be configured using an AC- or DC-coupled channel, while the SFP module can only be configured in an AC-coupled channel.

- SFF
  - AC/DC Coupled
  - 100Ω equivalent TX/RX termination
- SFP:
  - AC Coupled
  - 100Ω TX/RX termination

The FX mode transceivers incorporate an LVPECL differential driver to transmit the 4b5b encoded data, while the receiver supports both LVDS and LVPECL signal levels.

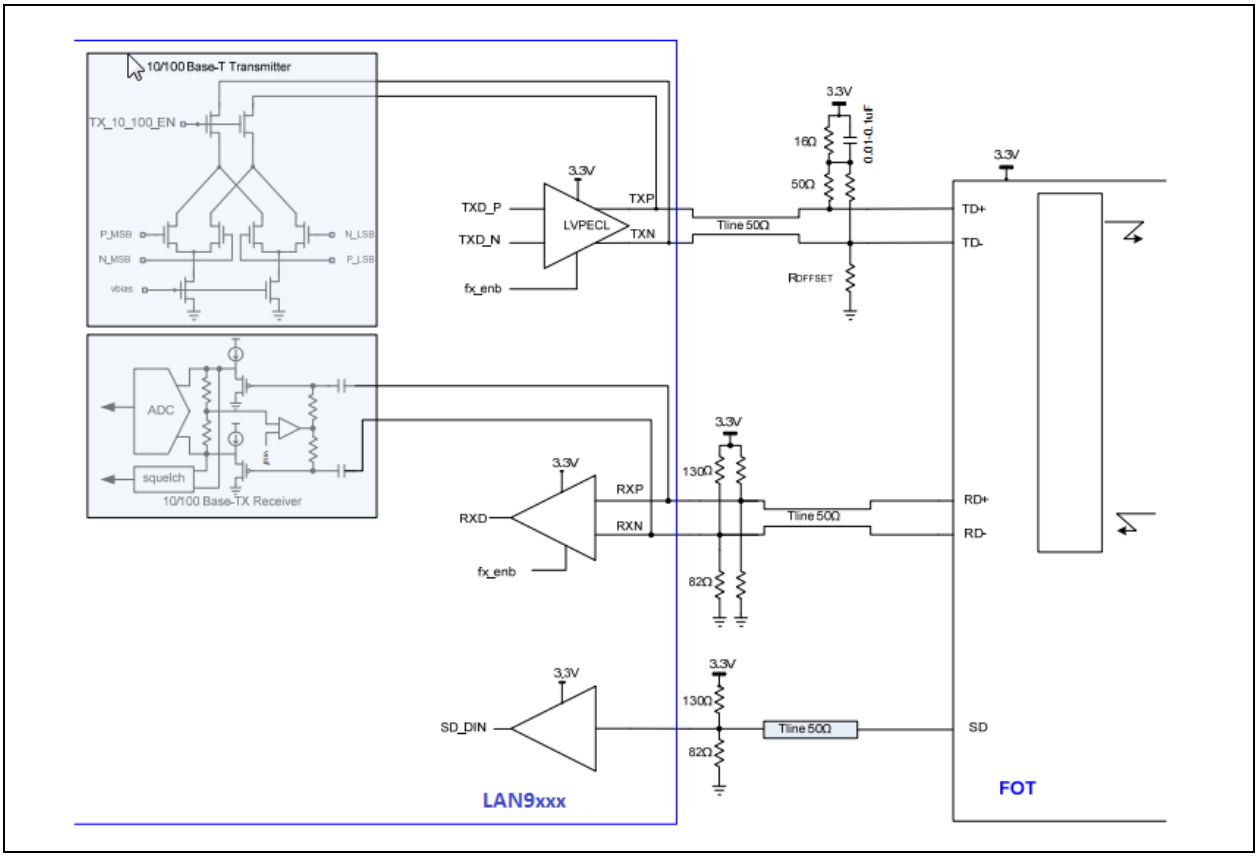
The following block diagrams show a common interface between the 10/100 Mbps Ethernet PHY and the FOT for various configurations.

DC Coupled (SFF Module)

Note:	DC coupling is recommended for 3.3V FOT modules.

The Jutland FX mode LVPECL output driver always requires a 50Ω termination. An additional 16Ω is required to set the proper common-mode voltage for the FOT. This configuration works only for 3.3V FOT. If the PHY is required to interface with 5V FOT, the value of the resistor that sets the common-mode voltage must change. It is recommended to use DC coupling for 3.3V FOTs. It is also a good practice to place the 50Ω termination resistor as close to the FOT as possible to minimize noise due to reflection. The Jutland FX mode receiver incorporates the 50Ω termination resistor external to the PHY to reduce on-chip power and to have flexibility on the value of the termination resistors to be used with AC-coupled channels. If offset is required on the transmitter path, ROFFSET resistor can be added from the TXN pad to ground. The value of the resistor is determined by the amount of offset required. SD is almost always DC-coupled and requires a 50Ω impedance with a 1.3V common-mode voltage.

FIGURE 1: 100BASE-FX DC-COUPLED CONFIGURATION (SFF MODE)

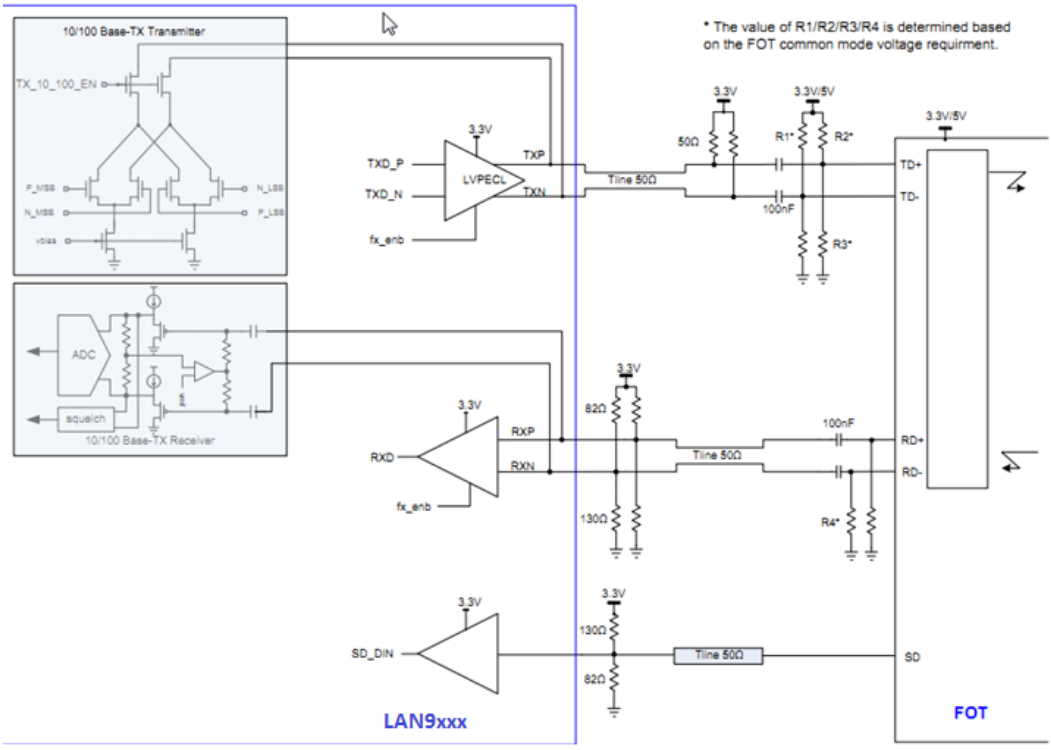


AC Coupled (SFF Module)

Note:	AC coupling is recommended for 5V FOT modules.

The Jutland FX mode LVPECL output driver always requires a 50Ω external termination. It is a good practice to place the 50Ω termination resistor as close to the FOT as possible to minimize noise due to reflection. The common-mode voltage of the receiver is set to be the same as the LVPECL common-mode voltage (VDD minus 1.3V). If offset is required on the transmitter path, increase or decrease the pull-up resistor at TD- as compared to the pull-up resistor at TD+. The mismatch value between the pull-up resistors is determined by the amount of offset required by the FOT. If zero offset is required, the values of the two pull-up resistors (R1* and R2*) at TD+ and TD- are equal. SD should be DC-coupled and include a 50Ω termination set to a common-mode voltage of 1.3V.

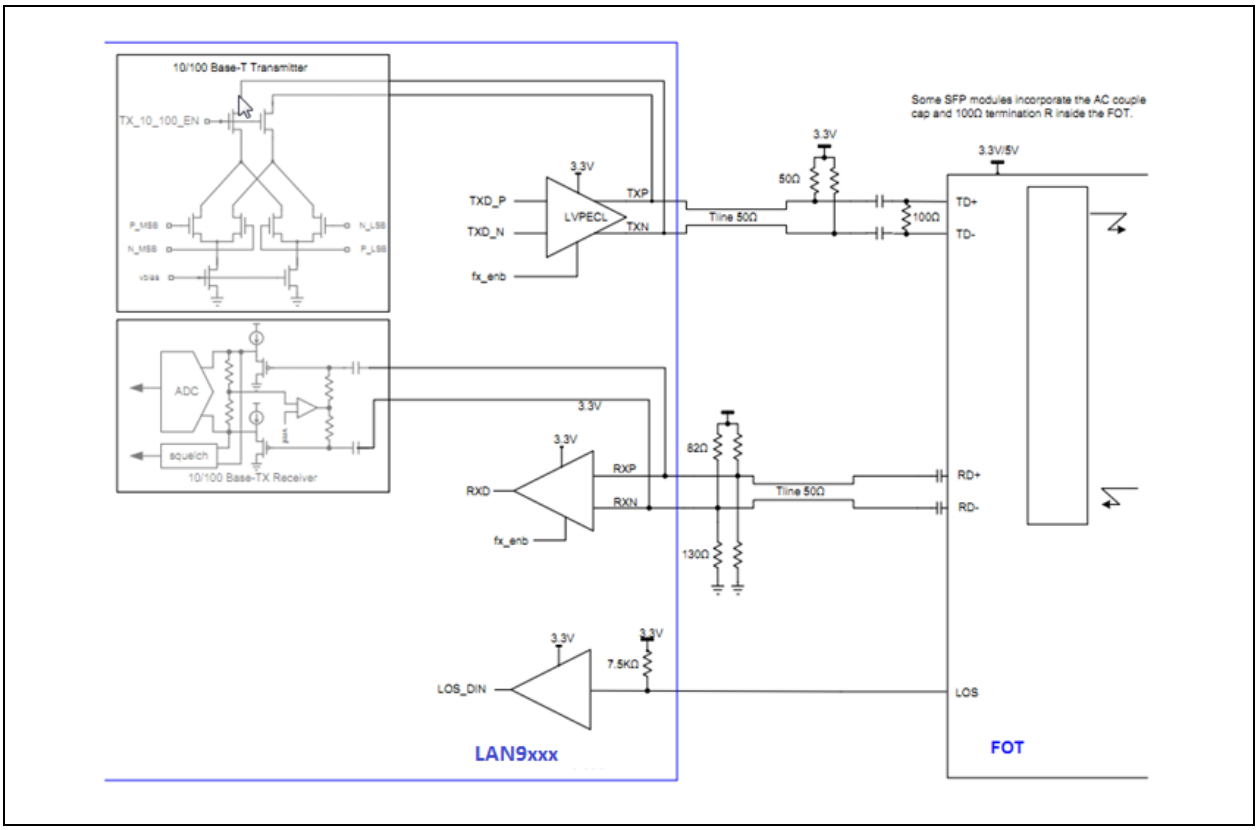
FIGURE 2: 100BASE-FX AC-COUPLED CONFIGURATION (SFF MODE)



AC Coupled (SFP Module)

The SFP module operates in a reduced LVPECL signaling level due to the AC couple nature of the channel and the 100Ω termination resistor embedded within the FOT module. The AC couple capacitor may or may not be embedded within the FOT module. The LVPECL transmitted data signal level will get reduced by half at the FOT input (TD+/-) due to the additional 100Ω termination. On the receive side, the 82Ω/130Ω off-chip termination resistors set the 50Ω termination as well as the common-mode voltage for the receiver. Jutland receiver requires the 50Ω termination resistors to be placed as close to the Jutland PHY as possible to minimize noise due to reflection. SD should be DC coupled and include a 50Ω termination set to a common-mode voltage of 1.3V.

FIGURE 3: 100BASE-FX AC-COUPLED CONFIGURATION (SFP MODE)



Register Settings

The Physical PHYs comply with the IEEE 802.3 Physical Layer for Twisted-Pair Ethernet and can be configured for full-/half-duplex 100 Mbps (100BASE-TX/100BASE-FX) or 10 Mbps (10BASE-T) Ethernet operation. All PHY registers follow the IEEE 802.3 (clause 22.2.4) specified MII management register set and are fully configurable.

100BASE-FX operation is enabled using the FX mode straps (fx_mode_strap_1 and fx_mode_strap_2) and is reflected in the 100BASE-FX mode (FX_MODE) bit in the PHY x Special Modes Register (PHY_SPECIAL_MODES_x).

Fiber Optical Modules

Several fiber optical modules may be used with an Ethernet PHY that supports 100BASE-FX (IEEE 802.3u):

- SFF Transceiver
  - AFBR-59E4APZ - Avago Technologies
  - (New 2x5 DIP style Package)
  - Differential LVPECL - TX, RX
  - Single-Ended LVPECL - SD
- 3.3V Supply
- Supported DC Coupling only

FIGURE 4: SFF TRANSCEIVER

- SFP Transceiver
  - FTLF1318P2xCL - Finisar Corporation
  - Reduced LVPECL - TX, RX
  - Open Drain/Collector - LOS
  - 3.3V Supply
  - Supported AC Coupling only

FIGURE 5: SFP TRANSCEIVER

Operational Controls and Indications

SUPPORTED FEATURES FOR 100BASE-FX

Because the 100BASE-FX mode uses 100BASE-T resources, its operational controls and indications are those of the 100BASE-T mode, such as LEDs, link status indication, and loopback modes.

- LED Indication - Any LED that supported 100BASE-TX now supports 100BASE-FX indication.
- Link Status - For link status indication, the Link Status bit Register 1.2 will indicate if a link is present for 100BASE-FX.

FEATURES NOT SUPPORTED FOR 100BASE-FX

Features not supported in FX mode include Auto-negotiation, AMDIX, TDR, EDPD, and EEE features.

ETHERCAT® OVER OPTICAL LINKS (FX) — APPLICABLE ONLY FOR LAN9252

EtherCAT communication over optical links using Ethernet PHYs is possible, but some requirements of EtherCAT should be taken into account, and some characteristics of EtherCAT slave controllers (ESC) should be considered.

This section intends to share current knowledge about FX operation with EtherCAT.

Link Partner Notification and Loop Closing

In case of link errors, the ESCs automatically disable unreliable links by closing loops. The ESCs rely on the LINK_MII signal from the PHYs for detecting the link state.

With FX PHYs, it could happen that the transceiver device is powered, while the PHY, the ESC, or both are not active. The communication partner would detect a signal, causing the link to open. All frames become lost because the PHY (or the ESC) is not operating.

Therefore, at least the following two requirements must be fulfilled; otherwise the frames will be lost:

- ESC in Reset state → Transceiver disabled
- PHY in Reset state → Transceiver disabled

The recommended solution for this issue is to enable the transceiver with the reset signal of the PHY. If the transceiver has no suitable input, the power supply of the transceiver can be switched off. Because the PHY's reset should be controlled by the ESC's reset output (delayed, see in the following section), the transceiver will power down while the PHY is in the Reset state and while the ESC is in the Reset state. Thus, the ESC and the PHY will be active when the transceiver becomes active, and no frames are lost.

FAR-END-FAULT (FEF) INDICATION

LAN9252 offers a feature called Far-End-Fault generation/detection, which indicates the link partner of a bad link.

The FEF feature is advantageous for EtherCAT because the PHYs will only indicate a link when the signal quality is high enough. Without FEF, the ESCs have to rely on the Enhanced Link Detection feature for detecting a low quality link.

Nevertheless, Enhanced Link Detection becomes active only after the link is already established, thus, in case of a low quality link, the link status will be toggling on/off (link up → Enhanced Link Detection tears down link → link up …). This is sufficient to locate an issue in the network, but it might disturb operation of the remaining network.

So, it is highly recommended to use PHYs that fully implement FEF generation and detection.

Standard Link Detection

The Enhanced Link Detection restarts auto-negotiation between the PHYs if a certain level of receive errors is reached. With FX PHYs, auto-negotiation is not available (it is a 100BASE-TX feature). Typically, PHYs ignore the restart auto-negotiation request. As a consequence, the ESC waits endlessly for the link to go down. Other PHYs might get into a dead-lock, because auto-negotiation is enabled by the restart auto-negotiation request, but it will not complete due to the FX operation mode.

Thus, Enhanced Link Detection has to be turned off for FX links (unless Enhanced FX Link Detection is used, which is recommended).

ISSUE: TEMPORARY ENHANCED LINK DETECTION WHILE EEPROM IS LOADING

Enhanced Link Detection is enabled after reset and can only be disabled by EEPROM. This takes about 170 ms. In the meantime, the FX PHYs are powering up. Since they do not need to go through an auto-negotiation sequence, the link (SD) comes very early. It is possible that the link is detected, but communication is not possible (RX_ERR are detected). This can trigger the ESC to restart auto-negotiation before the EEPROM is loaded, resulting in the ESC waiting for the link to go down. This will probably not happen because the PHY ignores this command, so the ESC remains in a dead-lock situation.

The recommended solution to overcome this issue is to power up the FX PHY (and the transceiver) at least 170 ms after the ESC, such as by an additional reset controller with delay or power sequencing (Figure 6 or Figure 7).

Another recommended solution is Enhanced FX Link Detection.

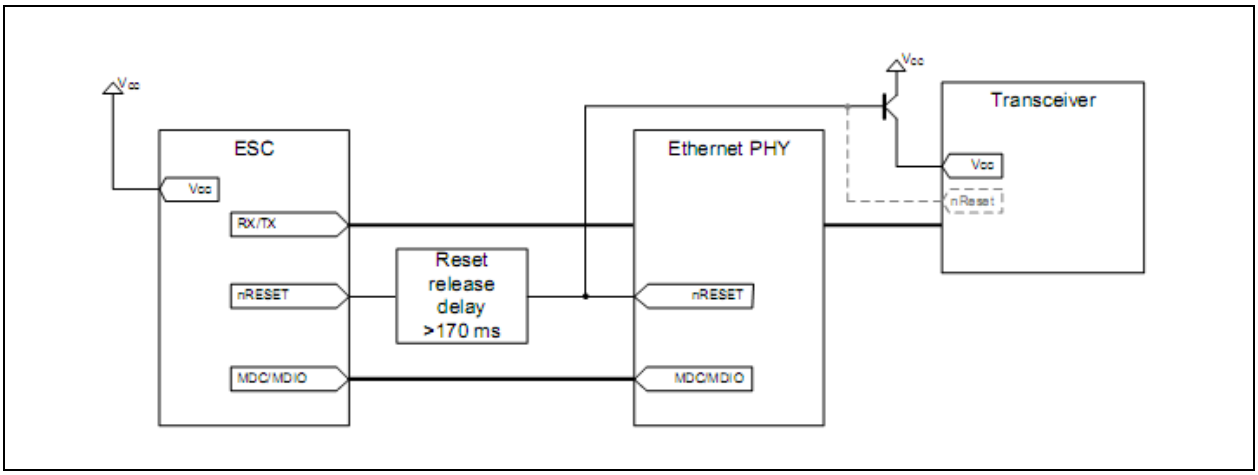
Minimum Solutions Without Enhanced Link Detection

These two solutions represent the minimum solution for proper power-up and reset operation, but they have drawbacks in detecting low quality links. The preferred solution is Enhanced FX Link Detection.

Standard Link Detection: By Delayed Reset to FX-PHY

RESET to External PHY is delayed by 170 ms after ESC (LAN9252) is getting ready.

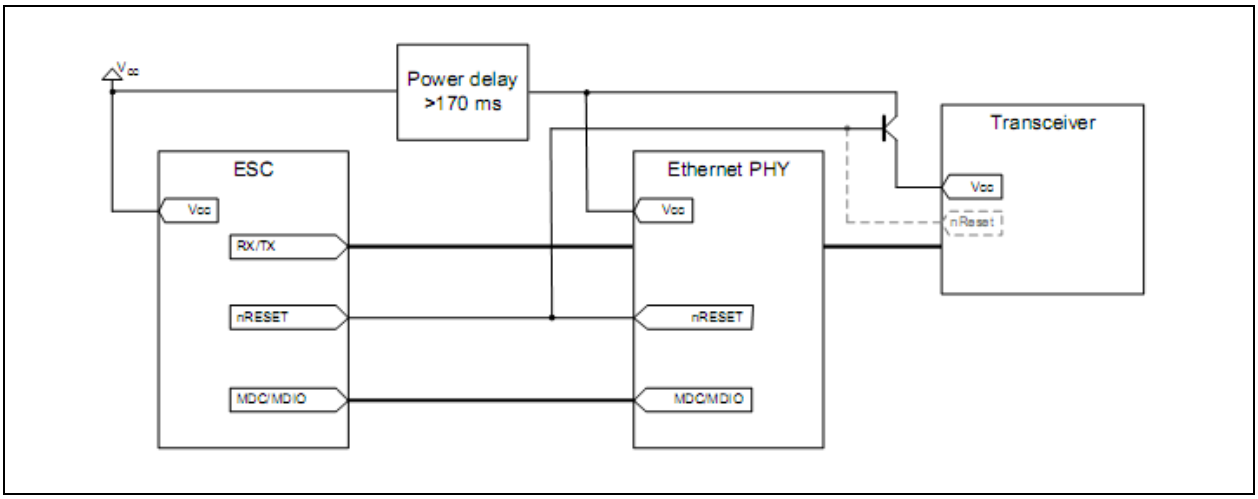
FIGURE 6: PHY RESET RELEASE DELAY WITH TRANSCEIVER POWER DOWN/RESET



Standard Link Detection: By Power Sequencing

POWER to External PHY is delayed by 170 ms after ESC is getting powered up.

FIGURE 7: PHY POWER SEQUENCING WITH TRANSCEIVER POWER DOWN/RESET



Enhanced FX Link Detection

To detect erroneous links fast enough, it is desirable to use the error detection principle of Enhanced Link Detection also for FX PHYs. One possible solution is to use the Enhanced Link Detection logic inside the ESC, and another possible solution is to implement Enhanced Link Detection logic with external logic, such as a CPLD.

LAN9252 ESC does not support Enhanced Link Detection logic for external MII port; hence an external logic should be implemented using a microcontroller/CPLD.

The preferred solution is to let the ESC count the RX_ERR of the PHY and to detect the restart auto-negotiation request of the ESC by some additional logic (CPLD or µController and so on.) attached to the MII management interface. This logic should reset the PHY and the transceiver (power-down) for a short time. This reset causes a link down that is detected by the local ESC (which leaves its potential dead-lock state) and by the communication partner (link down, loop closed). If this solution is selected, Enhanced Link Detection can be enabled in the EEPROM.

The MII management interface is still connected to the PHY, and the CPLD/µC only snoops the bus. It is possible to use one CPLD/µC for all ports of the ESC. The PHY address has to be evaluated, and individual reset outputs for each PHY have to be used.

PROPOSED SOLUTIONS WITH ENHANCED LINK DETECTION

Figure 8 and Figure 9 display the proposed solutions with Enhanced Link Detection.

FIGURE 8: CPLD/µC DETECTS AUTO-NEGOTIATION RESTART COMMAND AND RESETS PHY AND TRANSCEIVER

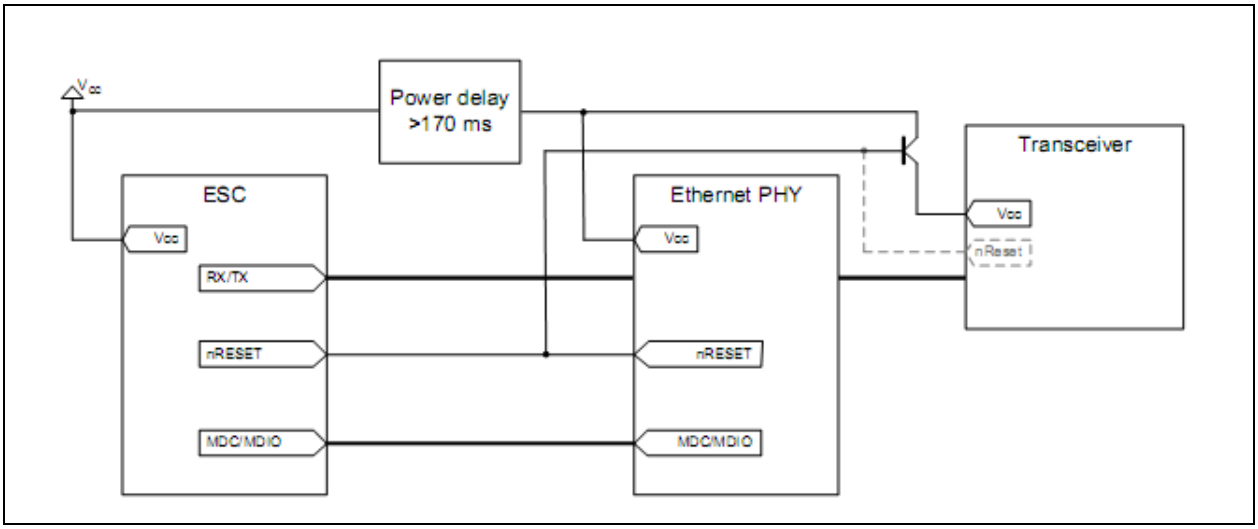
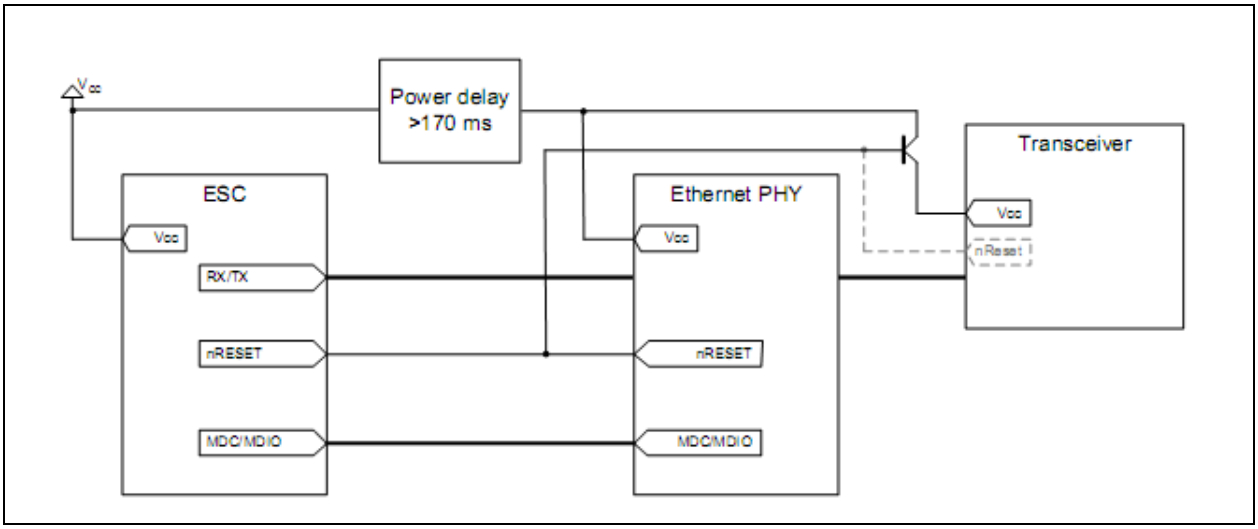


FIGURE 9: CPLD/µC DETECTS AUTO-NEGOTIATION RESTART COMMAND AND POWERS DOWN PHY AND TRANSCEIVER



Note: In Figure 9, the CPLD/µC is connected to the nRESET signal of the ESC/PHY to power down or reset the transceiver while the ESC/PHY is in the Reset state.

SUPPORT FOR COPPER MODE AND FIBER MODE FOR LAN9252 ESC

The LAN9252 ESC can support Copper mode (10/100BASE-TX) on one port and Fiber mode (10/100BASE-FX) on another port simultaneously. This section describes the required configuration for the SFP module support. As mentioned earlier, the SFP module uses LOS mode only. In LOS mode, the LAN9252 device can be strapped for any of these three configurations:

- PHY A copper, PHY B copper
- PHY A fiber, PHY B copper
- PHY A fiber, PHY B fiber

The fourth configuration (PHY A copper, PHY B fiber) is not valid for LOS mode.

TABLE 4: CONFIGURATION STRAPPING FOR PHY A COPPER, PHY B COPPER

Pin	Pull-Up/Pull-Down
FXLOSEN	Pull-Down
FXSDA/FXLOSA	Pull-Down
FXSDB/FXLOSB	Pull-Down

Note: A 10 kΩ pull-down resistor should be used.

TABLE 5: CONFIGURATION STRAPPING FOR PHY A FIBER, PHY B COPPER

Pin	Pull-Up/Pull-Down
FXLOSEN	Pull-up and Pull-Down (Note 1, Note 2)
FXSDA/FXLOSA	Pull-Up (Note 1)
FXSDB/FXLOSB	Pull-Down

Note 1: 10 kΩ pull-up and pull-down resistors should be used.

2: Voltage level 1.5V selects FX-LOS for port 0 and FX-SD/copper for port 1.

TABLE 6: CONFIGURATION STRAPPING FOR PHY A FIBER, PHY B FIBER

Pin	Pull-Up/Pull-Down
FXLOSEN	Pull-Up
FXSDA/FXLOSA	Pull-Up
FXSDB/FXLOSB	Pull-Up

Note: A 10 kΩ pull-up resistor should be used.

The fourth configuration (PHY A copper, PHY B fiber) requires SD signaling (SD mode) that allows the use of SFF module for PHY B. Table 7 shows the configuration strapping for this mode.

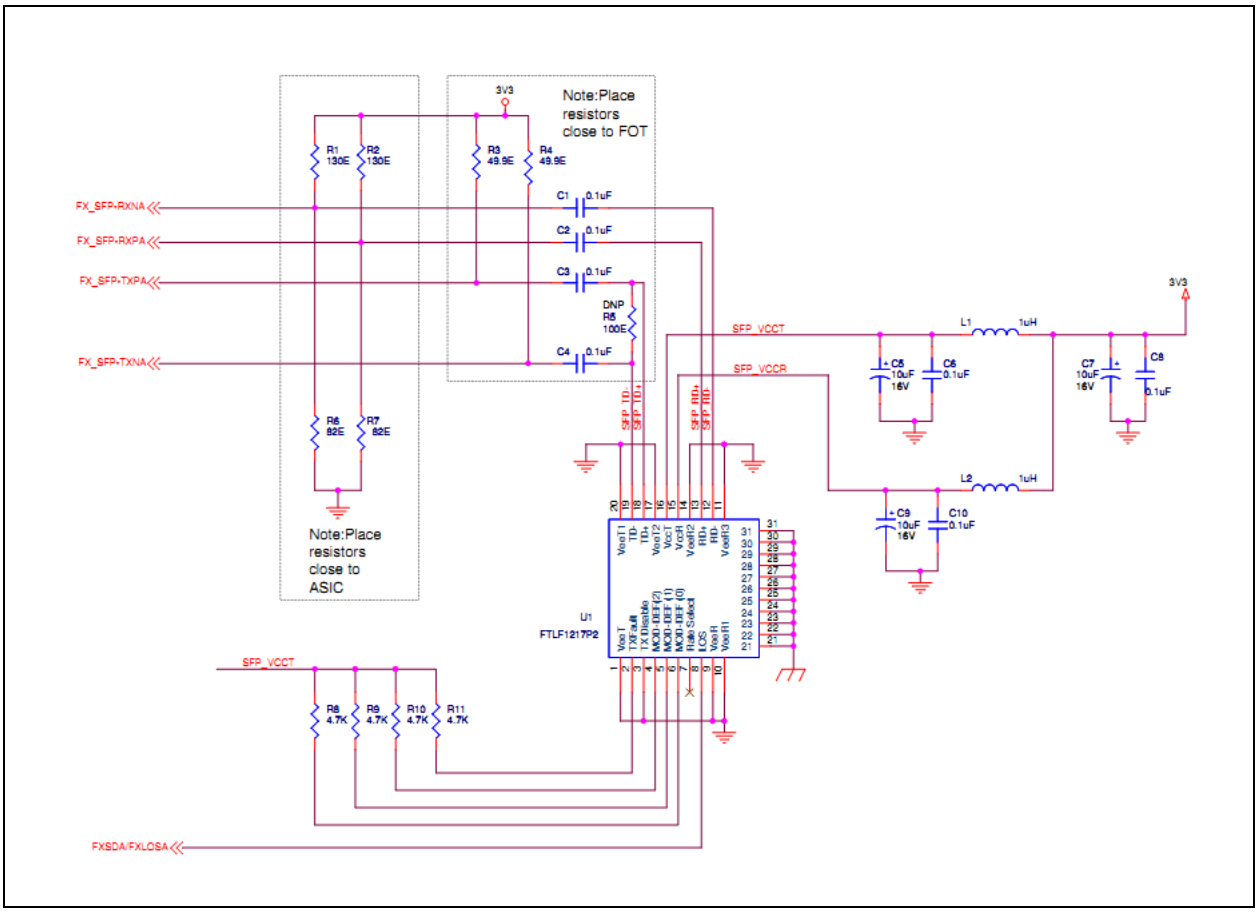
TABLE 7: CONFIGURATION STRAPPING FOR PHY A COPPER, PHY B FIBER

Pin	Pull-Up/Pull-Down
FXLOSEN	Pull-Down
FXSDA/FXLOSA	Pull-Down
FXSDB/FXLOSB	Pull-Up

Note: A 10 kΩ pull-up and pull-down resistors should be used.

APPENDIX A: SCHEMATICS

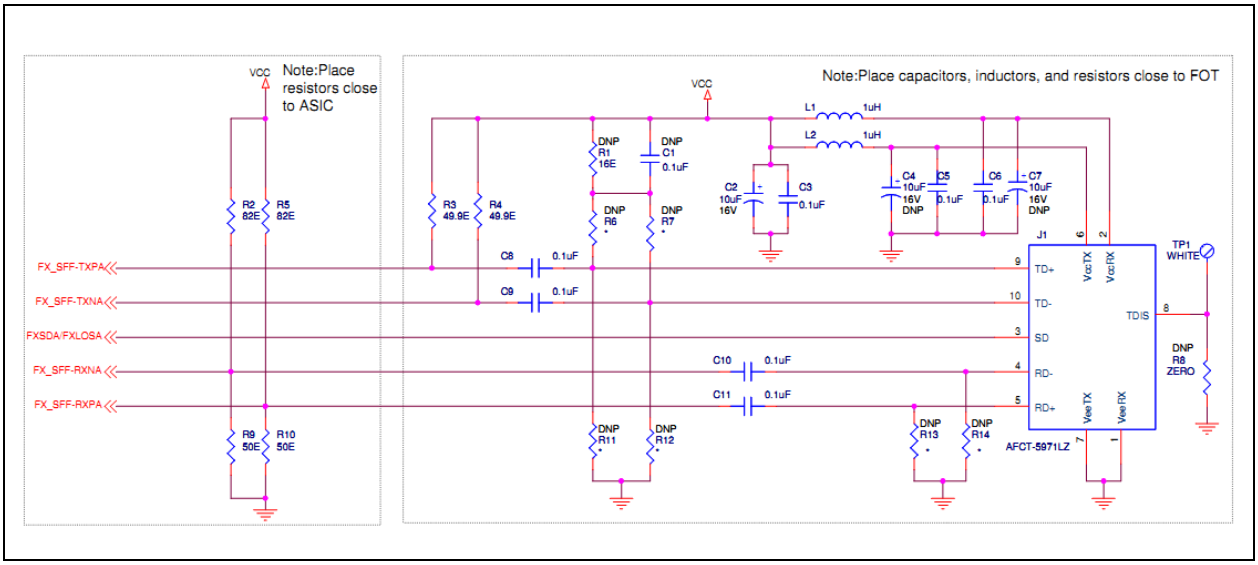
FIGURE A-1: INTERFACE BETWEEN LAN9XXX AND SFP (FTLF1318P2) FOT



Note 1: In SFP Transceiver FTLF1318P2, TX/RX DATA lines are AC-coupled. Hence, C1, C2, C3, and C4 are not required externally.

2: Refer to FOT supplier's recommendation regarding the interface between LAN9xxx and FOT. The proposed termination is recommended for AC Coupled Configuration (SFP mode). Other terminations could also be applied, depending on the FOT interface.

FIGURE A-2: INTERFACE BETWEEN LAN9XXX AND SFF (AFBR-59E4APZ) FOT



Note 1: In SFF Transceiver AFBR-59E4APZ, TX/RX DATA lines are AC-coupled. Hence, C8, C9, C10, and C11 are not required externally.

2: Refer to FOT supplier's recommendation regarding the interface between LAN9xxx and FOT. The proposed termination is recommended for AC Coupled Configuration (SFF mode). Other terminations could also be applied, depending on the FOT interface.

APPENDIX B: APPLICATION NOTE REVISION HISTORY

TABLE B-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002007B (01-27-20)	Support for Copper Mode and Fiber Mode for LAN9252 ESC	Added this section.
	All	Minor text changes throughout.
DS00002007A September 2015	Initial release.	

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Japan - Tokyo
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Korea - Daegu
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Malaysia - Penang
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Taiwan - Hsin Chu
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