AN3642

MEC172x System BIOS Porting Guide

INTRODUCTION

This document provides BIOS engineers a quick reference to port System BIOS in support of these MEC172x I/O devices: eSPI I/O Component (Configuration Port), eSPI Memory Component, Mailbox Interface, 8042 Emulated Keyboard Controller, ACPI EC0, ACPI EC1, ACPI EC2, ACPI EC3, ACPI EC4, ACPI PM1,Legacy Port92/GateA20, UART 0, UART 1, Glue Logic, EMI 0, EMI 1, EMI 2, Port 80 BIOS Debug Port 0 and Port 80 BIOS Debug Port 1.The MEC172x consists of MEC1721 and MEC1723 products.

References

The following document should be referenced when using this application note. Please contact your MCHP representative for availability.

- MEC172x Data Sheet
- Microchip “eSPI Controller with SAFS Support, Version 1.3” Specification

1.0 Contents

This guide consists of the following sections:

1.1 Terminology

This document contains the following terms, defined here for the purpose of convenience and general agreement:

TABLE 1-1: TERMS

Term	Description
System Host	Refers to the external CPU that communicates with this device via the eSPI Interface.
Logical Devices	Logical Devices are System Host-accessible features that are allocated a Base Address and range in the System Host I/O address space.
Runtime Register	Runtime Registers are registers that are directly I/O accessible by the System Host via the eSPI interface.
Configuration Registers	Registers that are only accessible in CONFIG_MODE.
EC_Only Registers	Registers that are not accessible by the System Host. They are only accessible by an internal embedded controller.

2.0 Obtaining the MEC172x Configuration Base Address

The eSPI Host can access the Chip's Configuration Registers through the Configuration Port when CONFIG MODE is enabled. The device defaults to CONFIG MODE being disabled.

Note: The data read from the Configuration Port Data register is undefined when CONFIG MODE is not enabled.

The Configuration Port is composed of an INDEX and DATA Register.

Logical devices are configured through three Configuration Ports (CONFIG, INDEX and DATA) (see Table 2-1, "Configuration Port"). The BIOS uses these ports to initialize the logical devices at POST.

The Base Address of the Configuration Ports is determined by the I/O Space Base Address Register (BAR) that corresponds to Logical Device Dh, the eSPI I/O Component Interface CR34h-CR37h. The default eSPI I/O Host address is 2Eh that be initialized by the EC firmware (Note 2-1).

Note 2-1 Please see the Section 3.7.1.6, "eSPI BAR Init Register", bits[15:0]: BAR_Init descriptions in the Microchip "eSPI Controller with SAFS Support, Version 1.3" Specification."

The BAR (Section 3.0, "Configuration Register Programming," on page 4) of Configuration Port can be relocated through the Configuration Registers for LDN Dh (eSPI Interface) 34h-37h, the bit[0]: VALID must be "1". (See Section 3.4, "Example: Relocating the BAR of Logical Device Dh to 4Eh," on page 4).

TABLE 2-1: CONFIGURATION PORT

Default I/O Address	Type	Register Name	Relative Address	Default Value	Notes
002Eh	Read / Write	INDEX	Configuration Port's Base Address + 0	00h	Note 1
002Fh	Read / Write	DATA	Configuration Port's Base Address + 1	00h	

Note 1: The default Base I/O Address of the Configuration Port can be relocated by programming the BAR register for Logical Device Dh (eSPI, I/O Configuration Port). The Relative Address shows the general case for determining the I/O address for each register.

3.0 Configuration Register Programming

The MEC172x contains the Global Control/Configuration Registers [00h - 2Fh] and the Logical Device Configuration Registers.

CONFIGURATION SEQUENCE

To program the configuration registers, the following sequence must be followed:

1. Entering the Configuration State
2. Configuring the Configuration Registers
3. Exiting the Configuration State

3.1 Entering the Configuration State

The INDEX and DATA ports are effective only when the chip is in the Configuration State. The device enters the Configuration State when the Config Entry Key is successfully written to the I/O address of the INDEX register of the CONFIG PORT while the CONFIG MODE is disabled.

Config Entry Key = < 55h>

3.2 Configuring the Configuration Registers

Configuration registers are accessed in two steps:

1. Write the index of the Logical Device Number Configuration Register (that is, 07h) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT.
2. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note:	If accessing the Global Configuration Registers, step (1) is not required.

3.3 Exiting the Configuration State

CONFIG MODE defaults to disabled on a RESET_SYS, RESET_HOST, and, for systems using eSPI, when RESET_HOST is asserted. CONFIG MODE is also disabled when the following Config Exit Key is successfully written to the I/O address of the INDEX PORT of the CONFIG PORT while CONFIG MODE is enabled.

Config Exit Key = < AAh>

3.4 Example: Relocating the BAR of Logical Device Dh to 4Eh

The following is a configuration register programming example written in Intel 8086 assembly language.

```
;----------------------------.
; Enable Configuration State |
;----------------------------'
MOV     DX, 02Eh ; Config_Port_Base_Address
MOV     AX, 055h ; Config Entry Key
OUT     DX, AL
;------------------------.
; Configure Base Address,|
; Logical Device 0Dh     |
;------------------------'
MOV     DX, 02Eh ; Config_Port_Base_Address
MOV     AL, 07h
OUT     DX, AL   ; Point to Logical Device Number Config Register
MOV     DX, 02Fh ; Config_Port_Base_Address+1
MOV     AL, 0Dh
OUT     DX, AL   ;Point to Logical Device Dh
;-------------------------------------------------------------------------.
; Configure both CR36 and CR37 to relocate the Base Address Register to 4Eh|
```

```
;------------------------------------------------------------------------.
MOV     DX, 02Eh ; Config_Port_Base_Address
MOV     AL, 036h ; CR36
OUT     DX, AL   ; Point to Base Address Register
MOV     DX, 02Fh ; Config_Port_Base_Address+1
;-------------------------------------------.
;Read the eSPI I/O Configuration Register Port  |
;-------------------------------------------.
IN      AL,DX   ; (Optional)It should be 2Eh

MOV     AL, 04Eh
OUT     DX, AL   ; Update CR36

MOV     DX, 02Eh ; Config_Port_Base_Address
MOV     AL, 037h ; CR37
OUT     DX, AL   ; Point to CR37
MOV     DX, 02Fh ; Config_Port_Base_Address+1
MOV     AL, 00h
OUT     DX, AL   ; Update CR37

;----------------------------.
; Disable Configuration State |
;----------------------------'
MOV     DX, 02Eh ; Config_Port_Base_Address
MOV     AX, 0AAh ; Config Exit Key
OUT     DX, AL
```

Note:	If you want to relocate the BAR of Logical Device Dh to 164Eh, use the example initialization to configure CR37 to 16h.

Note 3-1 See Table 10-5, “CHIP-LEVEL (GLOBAL) CONTROL/CONFIGURATION REGISTERS” of the latest MEC172x Data Sheet.

4.0 GLOBAL CONTROL/CONFIGURATION REGISTERS [00H - 2FH]

Host access to Global Configuration Registers is through the Configuration Port (the INDEX PORT and the DATA PORT) using the Logical Device Number 3Fh and the Index shown in the “Offset” column of the following table.

All Global Configuration registers are accessible to the Host through the Configuration Port for all Logical Devices. at offsets 00h through 2Fh.

TABLE 4-1: CHIP-LEVEL (GLOBAL) CONTROL/CONFIGURATION REGISTERS

Register	Offset	Description
CHIP (GLOBAL) CONTROL REGISTERS		
Reserved	00h - 01h	Reserved - Writes are ignored, reads return 0.
TEST	02h	TEST. This register location is reserved for Microchip use. Modifying this location may cause unwanted results.
Reserved	03h-06h	Reserved - Writes are ignored, reads return 0.
Logical Device Number	07h	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. **Note:** The Activate command operates only on the selected logical device.
Reserved	08h - 18h	Reserved - Writes are ignored, reads return 0.
Device Revision	1Ch	A read-only register which provides current device revision information.
Device Sub ID	1Dh	Read-Only register which provides the device sub-identification.
Device ID[7:0]	1Eh	Read-Only register which provides Device ID LSB.
Device ID[15:8]	1Fh	Read-Only register which provides Device ID MSB.
Legacy Device ID	20h	A read-only register which provides Legacy device identification.The value of this register is FEh
TEST	22h - 23h	TEST This register location is reserved for Microchip use. Modifying this location may cause unwanted results.
OTP ID	24h	The register contains the OTP ID.
Validation ID	25h	The register contains the Validation ID.
Boot ROM Revision ID	26-27h	The register contains the Boot ROM Revision ID
TEST	28h - 2Fh	TEST. This register locations are reserved for Microchip use. Modifying these locations may cause unwanted results.

5.0 Logical Device Configuration Registers

The Logical Device Configuration registers support motherboard designs in which the resources required by their components are known and assigned by the BIOS at POST.

Every logical device may have a set of directly I/O addressable Runtime Registers, Configuration Registers accessible via the Configuration Port, or DMA registers. The following table lists the register types for each eSPI-Host-accessible Logical Device implemented in the design. The Embedded Controller (EC) can access all Configuration Registers and all Runtime Registers directly.The Logical Devices physically located in the MEC172x are identified in Table 5-1, "Host Logical Devices on MEC172x eSPI".

TABLE 5-1: HOST LOGICAL DEVICES ON MEC172X ESPI

Logical Devices	Logical Device Number (hex)	Configuration Register Bank			eSPI I/O Runtime Access	eSPI I/O Configuration Access
		Host Config Index	Default eSPI I/O Host Address	Reset Default		
eSPI I/O Component (Configuration Port)	D	34h	002E	002E_0000h	yes	yes
eSPI Memory Component	E	38h	0000	0000_0000h	no	yes
Mailbox Interface	0	3Ch	0000	0000_0000h	yes	no
8042 Emulated Keyboard Controller	1	40h	0060	0060_0000h	yes	yes
ACPI EC0	2	44h	0062	0062_0000h	yes	no
ACPI EC1	3	48h	0000	0000_0000h	yes	no
ACPI EC2	4	4Ch	0000	0000_0000h	yes	no
ACPI EC3	5	50h	0000	0000_0000h	yes	no
ACPI EC4	6	54h	0000	0000_0000h	yes	no
ACPI PM1	7	58h	0000	0000_0000h	yes	no
Port 92-Legacy (Fast Keyboard)	8	5Ch	0092	0092_0000h	yes	yes
UART 0	9	60h	0000	0000_0000h	yes	yes
UART 1	A	64h	0000	0000_0000h	yes	yes
EMI 0	10	68h	0000	0000_0000h	yes	no
EMI 1	11	6Ch	0000	0000_0000h	yes	no
EMI 2	12	70h	0000	0000_0000h	yes	no
Real Time Clock	14	7C	0000	0000_0000h	yes	no
Port 80 BIOS Debug Port 0	20	74h	0000	0000_0000h	yes	yes

TABLE 5-1: HOST LOGICAL DEVICES ON MEC172X ESPI (CONTINUED)

Logical Devices	Logical Device Number (hex)	Configuration Register Bank			eSPI I/O Runtime Access	eSPI I/O Configuration Access
		Host Config Index	Default eSPI I/O Host Address	Reset Default		
Port 80 BIOS Debug Port 1	21	78h	0000	0000_0000h	yes	yes
32 Byte Test Block	2F	8Ah	0000	0000_0000h	yes	no
Glue	F	8Ch	0000	0000_0000h	yes	no

Note 5-1 Logical Devices EMI 0,EMI 1,EMI 2, ACPI EC0, ACPI EC1, ACPI EC2, ACPI EC3, ACPI EC4, ACPI PM1, UART 0, UART 1, Mailbox Interface, Port 80 BIOS Debug Port 0 and Port 80 BIOS Debug Port 1 Base Address Registers (BARs) must be located within the Generic Decode Ranges of the Chipset. For example, see Section 8.0, "Intel PCH eSPI I/O Decode Registers Initialization".

5.1 eSPI Logical Device Activation

The eSPI Activate Register controls the eSPI device itself. The Host can shut down the eSPI Logical Device by cleaning the Activate bit, but it cannot restart the eSPI interface, since once the eSPI interface is inactive the Host has no access to any registers on the device. The Embedded Controller can set or clear the Activate bit at any time.

This register should be configured by EC firmware before the EC releases RSMRST# and permits eSPI_RESET# to be de-asserted.

The format for the eSPI Activate Register is shown in Table 5-2, "eSPI Activate Register".

TABLE 5-2: ESPI ACTIVATE REGISTER

Offset	30h			
Bits	**Description**	**Type**	**Default**	**Reset Event**
7:1	RESERVED	RES	-	-
0	ACTIVATE 1= Activate When this bit is 1, the eSPI Logical Device is powered and functional. 0= Deactivate When this bit is 0, the logical device is powered down and inactive. Except for the eSPI Activate Register itself, clocks to the block are gated and the eSPI Logical Device will permit the main oscillator to be shut down.	R/W	0b	RESET_SYS

6.0 MEC172x eSPI IRQ Assignment Table

The section describes the Host IRQ assignment to support for the MEC172x eSPI Logical Devices in Table 6-1, "MEC172x eSPI IRQ Assignment Table".

TABLE 6-1: MEC172x eSPI IRQ Assignment Table

Host Config Index	Instance Name	Instance Number	Interrupt Source	Default Value (Note 6-1)
ACh	Mailbox Interface	0	MBX_Host_SIRQ	FFh
ADh	Mailbox Interface	0	MBX_Host_SMI	FFh
AEh	8042 Emulated Keyboard Controller	0	KIRQ	FFh
AFh	8042 Emulated Keyboard Controller	0	MIRQ	FFh
B0h	ACPI EC	0	EC_OBF	FFh
B1h	ACPI EC	1	EC_OBF	FFh
B2h	ACPI EC	2	EC_OBF	FFh
B3h	ACPI EC	3	EC_OBF	FFh
B4h	ACPI EC	4	EC_OBF	FFh
B5h	UART	0	UART	FFh
B6h	UART	1	UART	FFh
B7h	EMI	0	Host Event	FFh
B8h	EMI	0	EC-to-Host	FFh
B9h	EMI	1	Host Event	FFh
BAh	EMI	1	EC-to-Host	FFh
BBh	EMI	2	Host Event	FFh
BCh	EMI	2	EC-to-Host	FFh
BDh	RTC	0	RTC	FFh
BEh	EC	0	EC_IRQ	FFh

Note 6-1 The default value of FFh assigns no IRQ level to the interrupt, and does not propagate it.

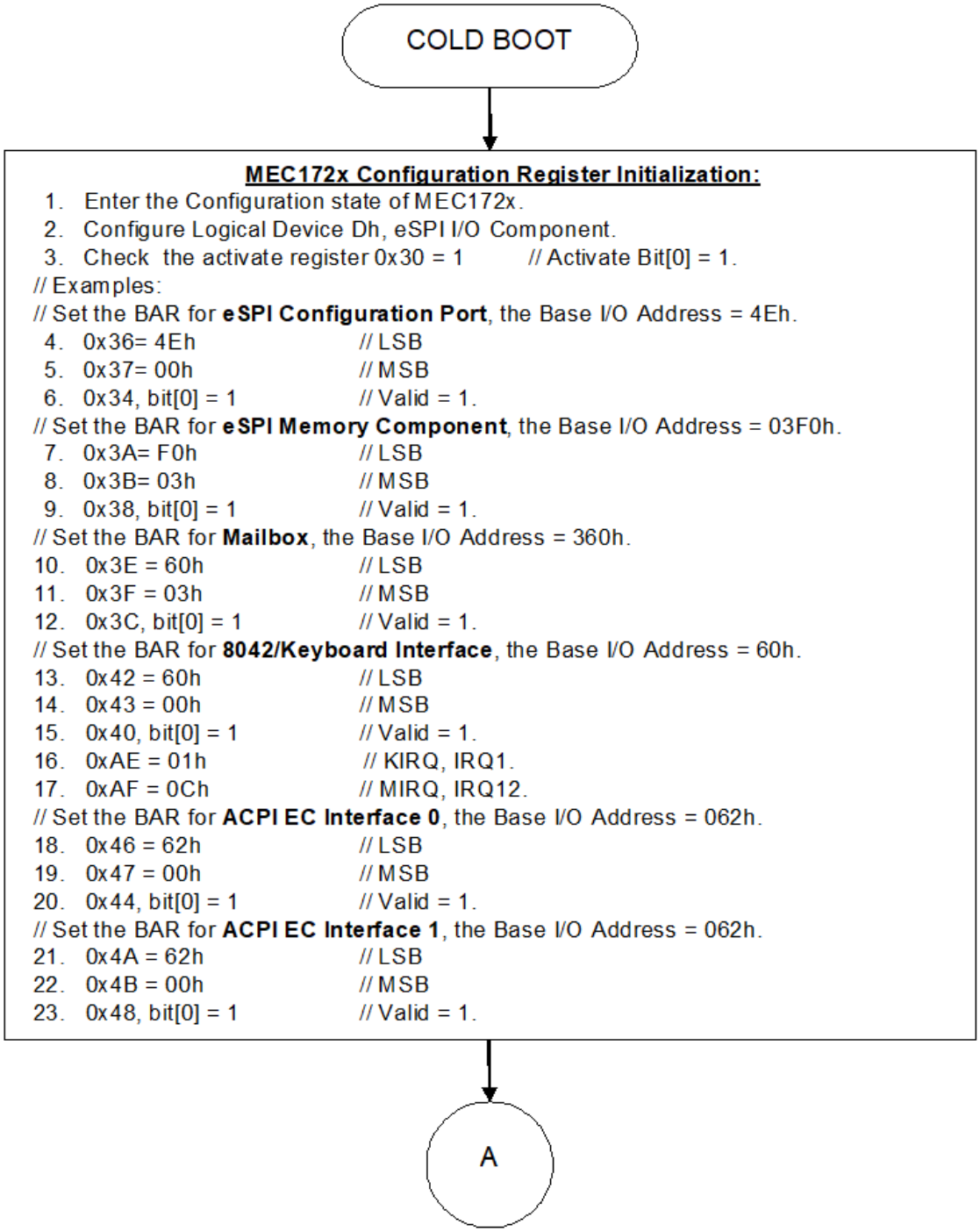
7.0 Super I/O Initialization In Early POST - eSPI Interface

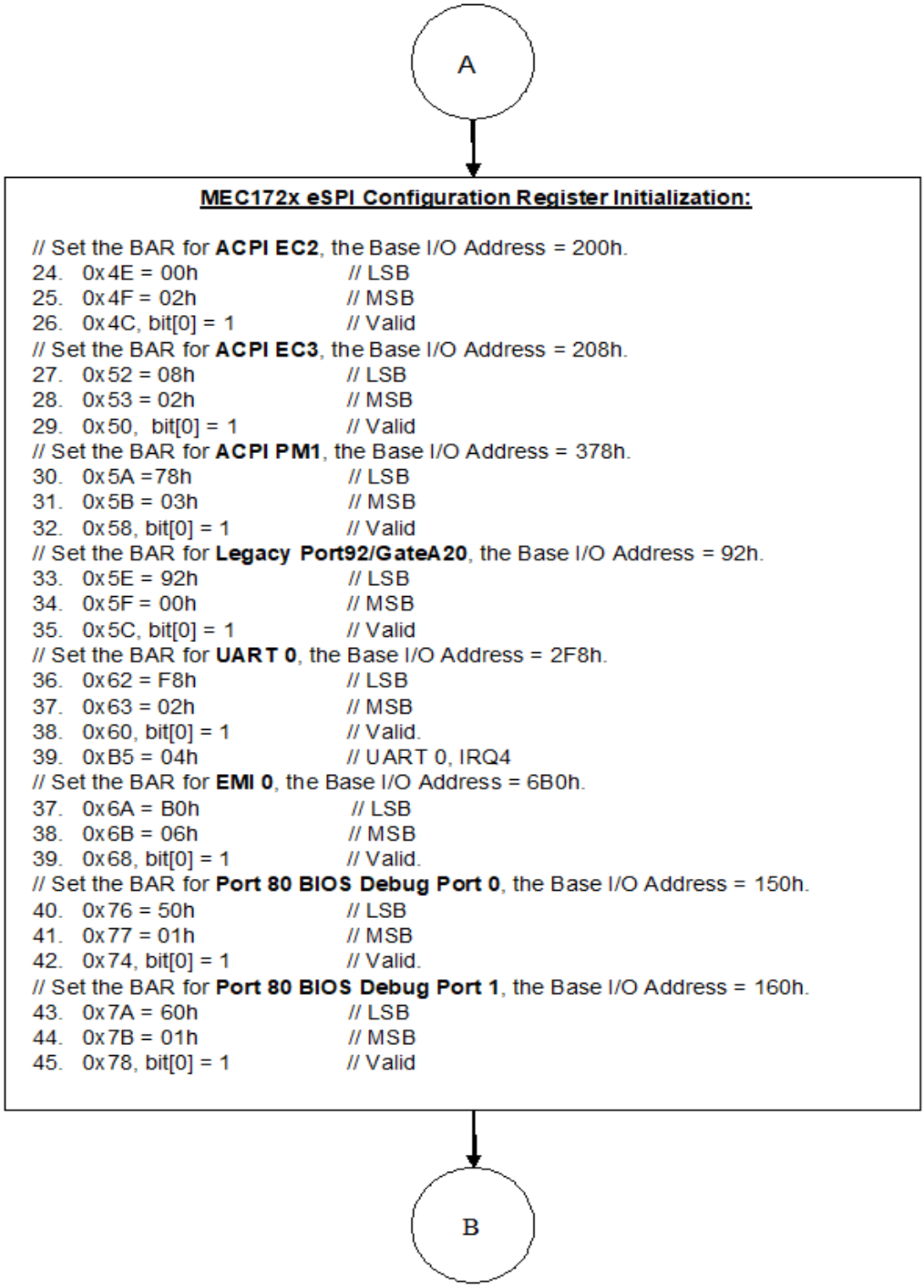
The section describes the Host through the eSPI interface to handle the Super I/O initialization in early POST.

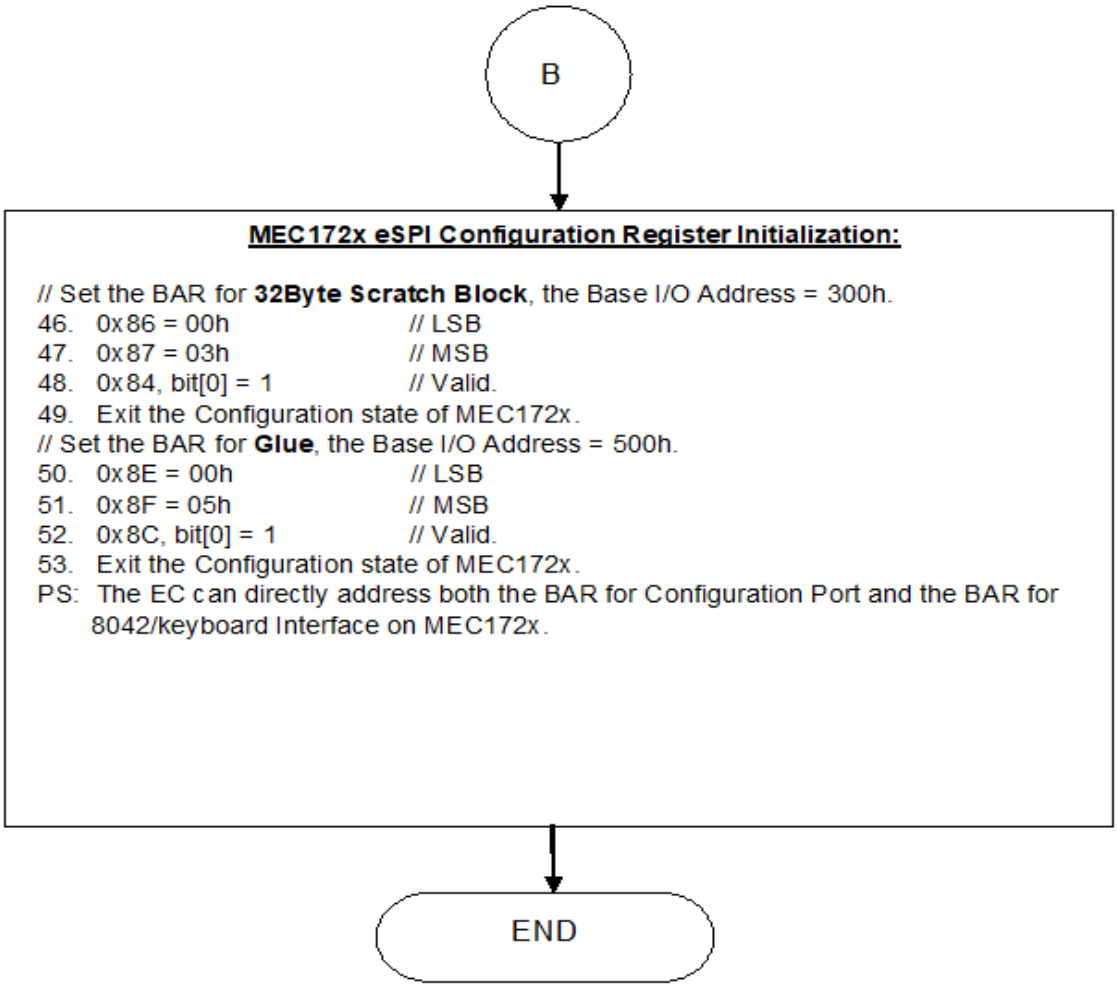
7.1 eSPI Configuration Registers initialization- Logical Device Dh Chart and Description

The following three figures show the process for MEC172x eSPI configuration registers initialization.

FIGURE 7-1: MEC172X CONFIGURATION REGISTERS INITIALIZATION - PART I




A
MEC172x eSPI Configuration Register Initialization:
// Set the BAR for ACPI EC2, the Base I/O Address = 200h.
24. 0x4E = 00h // LSB
25. 0x4F = 02h // MSB
26. 0x4C, bit[0] = 1 // Valid
// Set the BAR for ACPI EC3, the Base I/O Address = 208h.
27. 0x52 = 08h // LSB
28. 0x53 = 02h // MSB
29. 0x50, bit[0] = 1 // Valid
// Set the BAR for ACPI PM1, the Base I/O Address = 378h.
30. 0x5A =78h // LSB
31. 0x5B = 03h // MSB
32. 0x58, bit[0] = 1 // Valid
// Set the BAR for Legacy Port92/GateA20, the Base I/O Address = 92h.
33. 0x5E = 92h // LSB
34. 0x5F = 00h // MSB
35. 0x5C, bit[0] = 1 // Valid
// Set the BAR for UART 0, the Base I/O Address = 2F8h.
36. 0x62 = F8h // LSB
37. 0x63 = 02h // MSB
38. 0x60, bit[0] = 1 // Valid.
39. 0xB5 = 04h // UART 0, IRQ4
// Set the BAR for EMI 0, the Base I/O Address = 6B0h.
37. 0x6A = B0h // LSB
38. 0x6B = 06h // MSB
39. 0x68, bit[0] = 1 // Valid.
// Set the BAR for Port 80 BIOS Debug Port 0, the Base I/O Address = 150h.
40. 0x76 = 50h // LSB
41. 0x77 = 01h // MSB
42. 0x74, bit[0] = 1 // Valid.
// Set the BAR for Port 80 BIOS Debug Port 1, the Base I/O Address = 160h.
43. 0x7A = 60h // LSB
44. 0x7B = 01h // MSB
45. 0x78, bit[0] = 1 // Valid
B



Note: Both the **Activate bit** in Activate Register offset 30h and the **Valid bit** in BAR control different functionality, and do not affect each other.

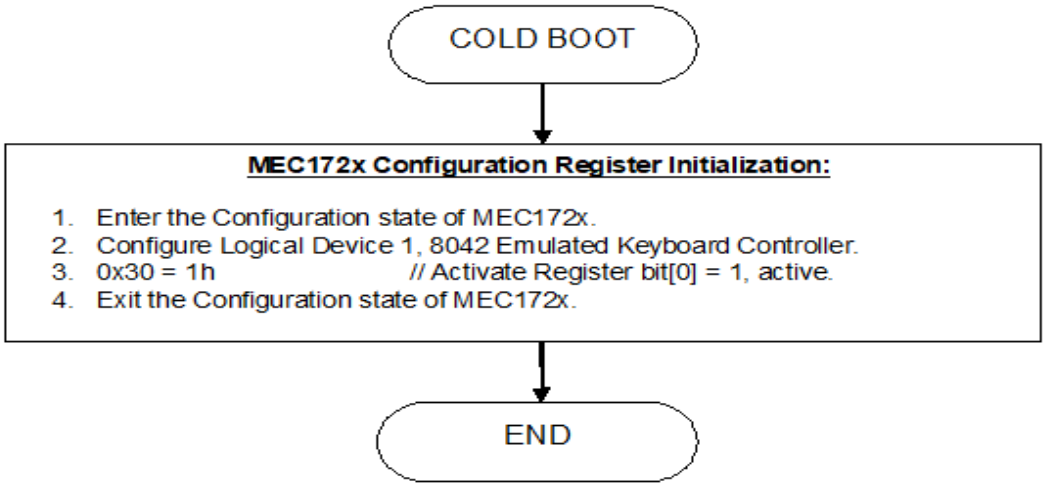
- Activate bit = 1, block is powered and functional. (In fact, not really powered, should be gated.)
- Valid bit = 1, the MEC172x chip I/O address claiming is enabled. See the Section 3.4.1.1,"I/O Base Address Configuration Register Format in the Microchip "eSPI Controller with SAFS Support, Version 1.3" Specification.

Note: Bits[31:16] eSPI Host Address bit field in the Base Address register for Logical Device Dh (eSPI I/O Configuration Port) must be written LSB then MSB. This particular register has a shadow that lets the Host come in and write to the lower byte of the 16-bit address, and the resulting 16-bit eSPI Host address field does not update. Writing to the upper byte triggers a full 16-bit field update.

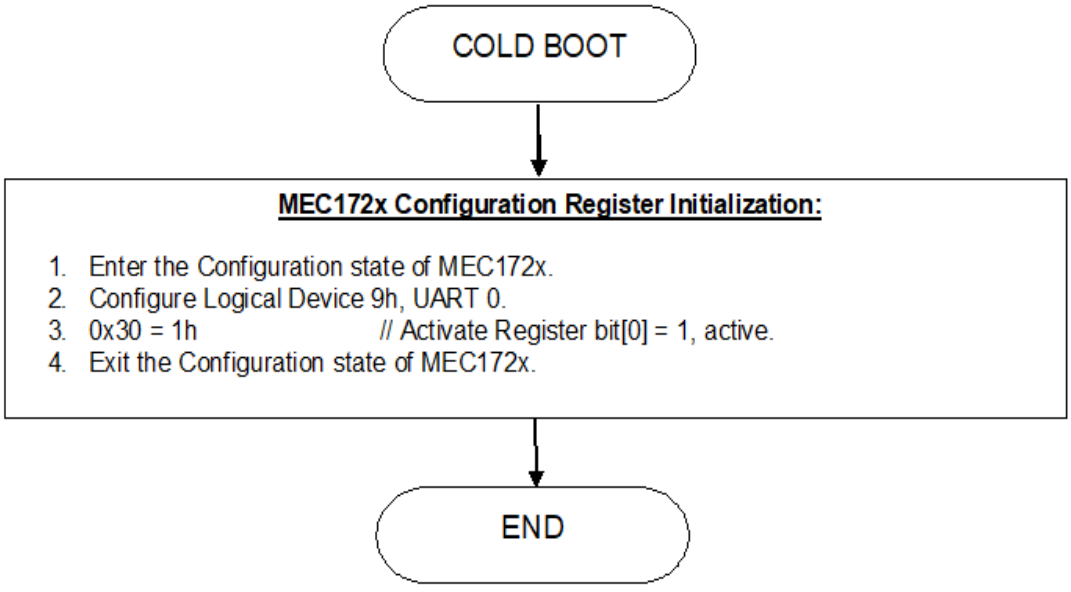
BIOS must set both bits to activate this module and make it functional. The following is the recommended sequence:

1. Configure correct I/O address in BAR if needed.
2. Set Valid bit in BAR.
3. Set Activate bit in the Activate register if available.

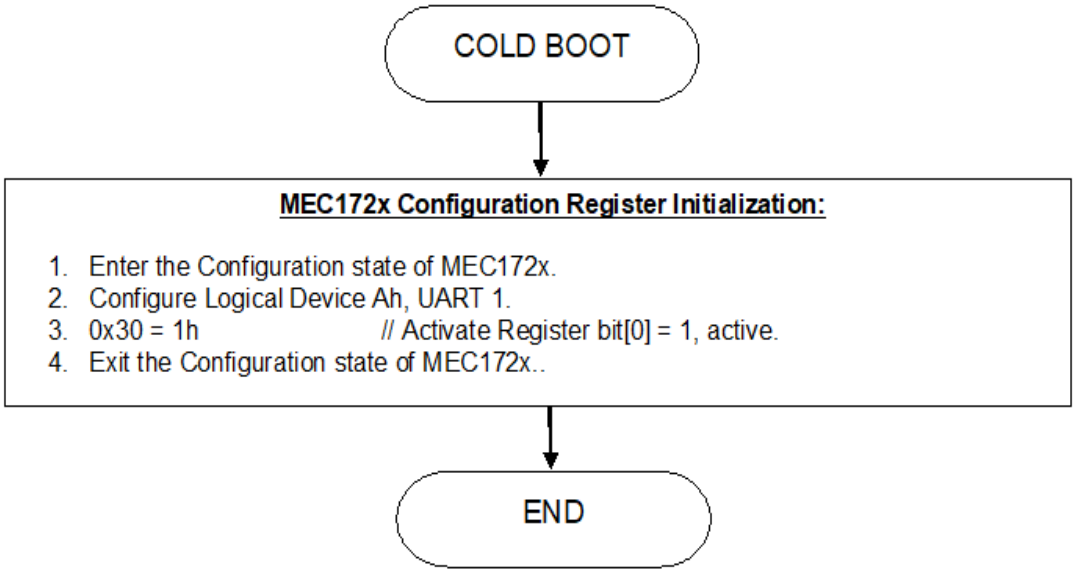
7.2 8042 Emulated Keyboard Controller - Logical Device 1 Chart and Description



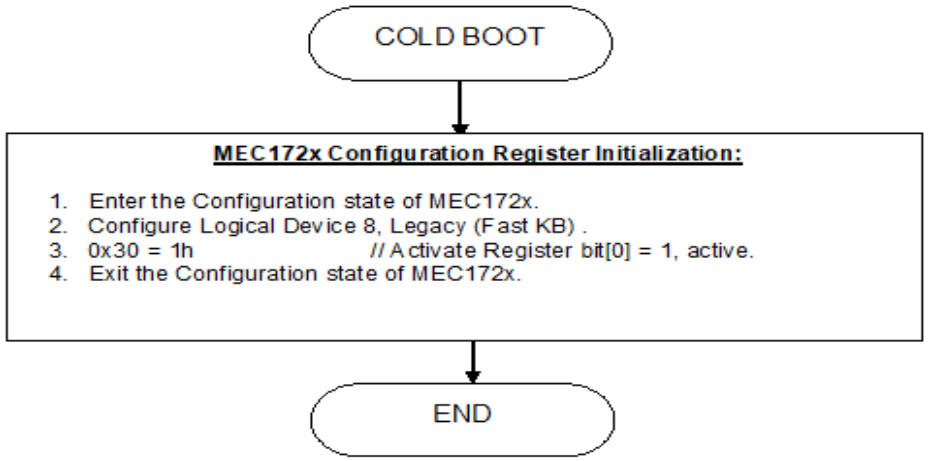
7.3 UART 0 - Logical Device 9h Chart and Description



7.4 UART 1 - Logical Device Ah Chart and Description



7.5 Legacy (Fast KB) - Logical Device 8 Chart and Description



8.0 INTEL PCH ESPI I/O DECODE REGISTERS INITIALIZATION

This section provides the initialization of Intel PCH Enhanced SPI Interface (D31:F0) I/O Decode registers to support MEC172x SIO devices in cold booting.

8.1 eSPI I/O Decode Ranges Decoding

Setup “ESPI I/O Decode Ranges”, PCR[DMI] + 2770h [15:0] to the same value program in ESPI PCI offset 80h (Note 8-1).

Note 8-1 See the Section 2.1.7, “I/O Decode Ranges and I/O Enables (ESPI_IOD_IOE) - Offset 80h in the Intel doc. #545845_SKL_PCH_EDS_V2_Rev_1_0.pdf for the details.

8.2 eSPI I/O Enables Decoding

Setup “ESPI I/O Enables”, PCR[DMI] + 2774h [15:0] to the same value program in ESPI PCI offset 82h (Note 8-2).

Note 8-2 Bits[15:10]of source decode register is Read-Only. The I/O ranges are indicated by the Enables field in EPI PCI offset 82h [13:10] is always forwarded by DMI to subtractive agent for handling.

8.2.1 I/O DECODE RANGES AND I/O ENABLES (ESPI_IOD_IOE) - OFFSET 80H = 3F030010H

- Bit[29] = 1 // Microcontroller Enable #2 (ME2): Enables decoding of I/O locations 4Eh and 4Fh.
- Bit[28] = 1 // Super I/O Enable (SE): Enables decoding of I/O locations 2Eh and 2Fh.
- Bit[27] = 1 // Microcontroller Enable #1 (ME1): Enables decoding of I/O locations 62h and 66h.
- Bit[26] = 1 // Keyboard Enable (KE): Enables decoding of the keyboard I/O locations 60h and 64h.
- Bit[25] = 1 // High Gameport Enable (HGE): Enables decoding of I/O locations 208h and 20Fh.
- Bit[24] = 1 // Low Gameport Enable (LGE): Enables decoding of I/O locations 200h and 207h.
- Bit[17] = 1 // Com Port B Enable (CBE): Enables decoding of the COMB range. Range is selected by bits[6:4].
- Bit[16] = 1 // Com Port A Enable (CAE): Enables decoding of the COMA range. Range is selected by bits[2:0].
- Bits[6:4] = 001b // ComB Range (CB): Enables decoding of I/O locations 2F8h - 2FFh (COM2).
- Bits[2:0] = 000b // ComA Range (CA): Enables decoding of I/O locations 3F8h - 3FFh (COM1).

8.3 eSPI Generic I/O Range Decoding

Setup “eSPI Generic I/O Range #1~#4”, PCR[DMI] + 2730h~273Fh to the same value program in ESPI PCI offset 84h~93h.

8.3.1 ESPI GENERIC I/O RANGE #1 (ESPI_LGIR1) - OFFSET 84H = 007C0301H

- Bits[23:18] = 7Ch // Address [7:2] Mask (ADDR_MASK): A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
- Bits[15:2] = 030h // Address [15:2] (ADDR): DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
- Bit[0] = 1 // ESPI Decode Enable: The ESPI Generic I/O Range #1 is enabled for decoding to ESPI.

8.3.2 ESPI GENERIC I/O RANGE #2 (ESPI_LGIR2) - OFFSET 88H = 007C0681H

- Bits[23:18] = 7Ch // Address [7:2] Mask (ADDR_MASK): A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
- Bits[15:2] = 068h // Address [15:2] (ADDR): DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
- Bit[0] = 1 // ESPI Decode Enable: The ESPI Generic I/O Range #2 is enabled for decoding to ESPI.

8.3.3 ESPI GENERIC I/O RANGE #3 (ESPI_LGIR3) - OFFSET 8CH = 007C0151H

- Bits[23:18] = 7Ch // Address [7:2] Mask (ADDR_MASK): A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
- Bits[15:2] = 015h // Address [15:2] (ADDR): DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
- Bit[0] = 1 // ESPI Decode Enable: The ESPI Generic I/O Range #3 is enabled for decoding to ESPI.

8.3.4 ESPI GENERIC I/O RANGE #4 (ESPI_LGIR4) - OFFSET 90H = 000C0361H

- Bits[23:18] = 0Ch // Address [7:2] Mask (ADDR_MASK): A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
- Bits[15:2] = 036h // Address [15:2] (ADDR): DWord-aligned address. Note that PCH does not provide decode down to the word or byte level.
- Bit[0] = 1 // ESPI Decode Enable: The ESPI Generic I/O Range #4 is enabled for decoding to ESPI.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003642A (09-01-20)	Document Release	

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
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CUSTOMER CHANGE NOTIFICATION SERVICE

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- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at: http://www.microchip.com/support

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
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