AN3166

Migrating from SAM9x5 to SAM9X60

Scope

This application note describes the hardware and software changes necessary to migrate a SAM9x5-based design to a SAM9X60 device. The SAM9X60 device provides increased performance compared to SAM9x5.

The changes listed in this document should be performed on the SAM9X60 device for proper operation. Other system changes may be required to accommodate new speeds or capabilities.

Additional information on the devices is available in the respective data sheets. See Reference Documents.

Note: In this document "SAM9x5" refers to any of the following products:

- SAM9G15
- SAM9G25
- SAM9G35
- SAM9X25
- SAM9X35

Reference Documents

The following documents are available on http://www.microchip.com.

Document Type	Document Title	Literature Number
Data sheet	SAM9X60	DS60001579
Data sheet	SAM9G15	11052
Data sheet	SAM9G25	11032
Data sheet	SAM9G35	11053
Data sheet	SAM9X25	11054
Data sheet	SAM9X35	11055

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1. SAM9x5 vs. SAM9X60 Feature Summary

The following table summarizes the differences between SAM9x5 and SAM9X60 features.

Table 1-1. SAM9x5 vs. SAM9X60 Features

Item	SAM9x5	SAM9X60	Comments
System			
Core/Bus frequency	400/133 MHz	600/200 MHz	–
L1 cache size	16 Kbytes I + 16 Kbytes D	32 Kbytes I + 32 Kbytes D	–
SRAM size	32 Kbytes	64 Kbytes + 4 Kbytes for OTP emulation	–
OTP memory	–	• 11-Kbyte OTP • Area for user's certificates, keys and configuration • Disable JTAG OTP bit • Emulation mode (see SRAM)	23 Kbytes allocated to user
ROM boot	No security/encryption features	Secure boot with encryption, certificates and key management (see OTP)	–
Power supplies	1.0V core voltage	• 1.1V core voltage • 2.5V regulator added • VDDQSPI segment	For PLLs and oscillators
System controller, clocks, power management	• 32 KHz RC can be stopped • 12 to 16 MHz crystal • 12 MHz required for USB operations • 400 to 800 MHz PLLs • Peripheral I/Os are clocked at MCK	• 32 KHz RC always on • 12 to 48 MHz crystal • Main RC calibration • 32 KHz RC calibration • More frequencies can fit USB operation; PLLs are fractional • 600 to 1200 MHz PLLs with spread spectrum • Generic clocks available for most peripheral I/Os • Clocks monitoring • ULP1 added, power consumption improved and wake-up time reduced • Separated pins for reset input (NRST) and reset output (NRST_OUT)	Safety for WDT, RSTC, etc. EMI/EMC improvement
DMA	2x 8-channel DMAs	1x 16-channel DMA	–
DDR controller	External resistors needed for PCB impedance matching	DDR I/Os with calibration for impedance matching, additional control signal	Reduced BOM cost and board space
NAND Flash	16-bit	8-bit only	–
Special Function Register	Memory mapped in Matrix section	Memory mapped in SFR section	–
Peripheral Multiplexing on I/O lines	–	Compatible 7 lines added Peripherals added	–
Peripheral Upgrades			
eMMC	HSMCI, eMMC 4.1	SDMMC, eMMC 4.51	

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Item	SAM9x5	SAM9X60	Comments
Serial	USART0-2 SPI0-1 TWI0-2 UART0-1	FLEXCOM0-2 FLEXCOM4-5(*) FLEXCOM6-8 FLEXCOM9-10 FLEXCOM3-11-12 added (*)Some FLEXCOMs include extra IOSETs.	Some FLEXCOMs enable USART, SPI and TWI functions, or only UART and TWI
USB	2x HS + 1x FS transceivers 4-Kbyte DPRAM with dynamic allocation	3x HS transceivers External Full Speed resistors removed 16-Kbyte DPRAM; each end point has its own memory area	–
Soft Modem (SMD)	Embedded	Removed	–
LCD controller	4 layers: • Base • Overlay • High end • HW cursor 800x600 pixel resolution	4 layers: • Base • Overlay1 • Overlay2 • High end 1024x768 pixel resolution	–
2D graphics (GFX2D)	–	Added	–
ADC	10 bits	12 bits Internal triggers	–
64-bit Timer (PIT64B)	–	Added	–
QSPI	–	4-bit QSPI added with dedicated power supply	SDR and DDR support; eXecution In Place (XIP)
I2SMCC	–	Added	–
CLASSD	–	Added	–
Encryption engines (TDES, AES, SHA, TRNG)	–	Added	–
Packages	BGA217, 15x15 mm^2, 0.8 mm pitch BGA247, 10x10 mm^2, 0.5 mm pitch	BGA196 11x11 mm^2 0.65 mm pitch for SiP with 64-Mbit SDRAM BGA228, 11x11 mm^2, 0.65 mm pitch BGA233 14x14 mm^2 0.8 mm pitch for SiP with 512-Mbit and 1-Gbit DDR2 SDR-SDRAM and DDR2-SDRAM SiP added	Accommodates 4-layer PCBs

2. PCB Migration

This section describes the hardware changes needed to migrate from SAM9x5 to SAM9X60. These changes are required in all systems.

2.1 Packages and Pinout

SAM9x5 and SAM9X60 packages differ. SAM9X60 BGA228 is designed to accommodate low-cost 4-layer PCBs when DDR2 is used.

Due to peripheral upgrades, some signals are removed or added in the pinout.

Table 2-1. Packages and Pinout

Peripheral	Removed from SAM9x5	Added on SAM9X60
USB	DFSDM/HFSDMA, DFSDP/HFSDPA HFSDMB, HFSDPB HFSDMC, HFSDPC	HHSDMC/HHSDPC
SMD	DIBN, DIBP	–
Boot ROM	BMS	–
DDRC	–	DDR_VREF, DDR_CAL
PIO lines	–	7 IOs (PIOB19 to PIOB25) for extra functions (QSPI, I2SMCC)

2.2 Power Supplies

Technology upgrade from 90 nm to 40 nm requires different power supplies.

Table 2-2. SAM9x5 vs. SAM9X60 Power Supplies

Power Rail	SAM9x5	SAM9X60
VDDCORE VDDUTMIC	0.9-1.1V, 1.0V typical	1.0-1.2V, 1.1V typical Full CPU speed requires VDDCORE min = 1.1V
VDDPLLA	0.9-1.1V, 1.0V typical	VDDOUT25 replaces VDDPLLA. VDDOUT25 is the output of an internal 2.5V LDO and must be connected to an external decoupling capacitor.
VDDOSC	1.65-3.6V	2.7-3.6V

Figure 2-1. Typical Power Supply Implementations

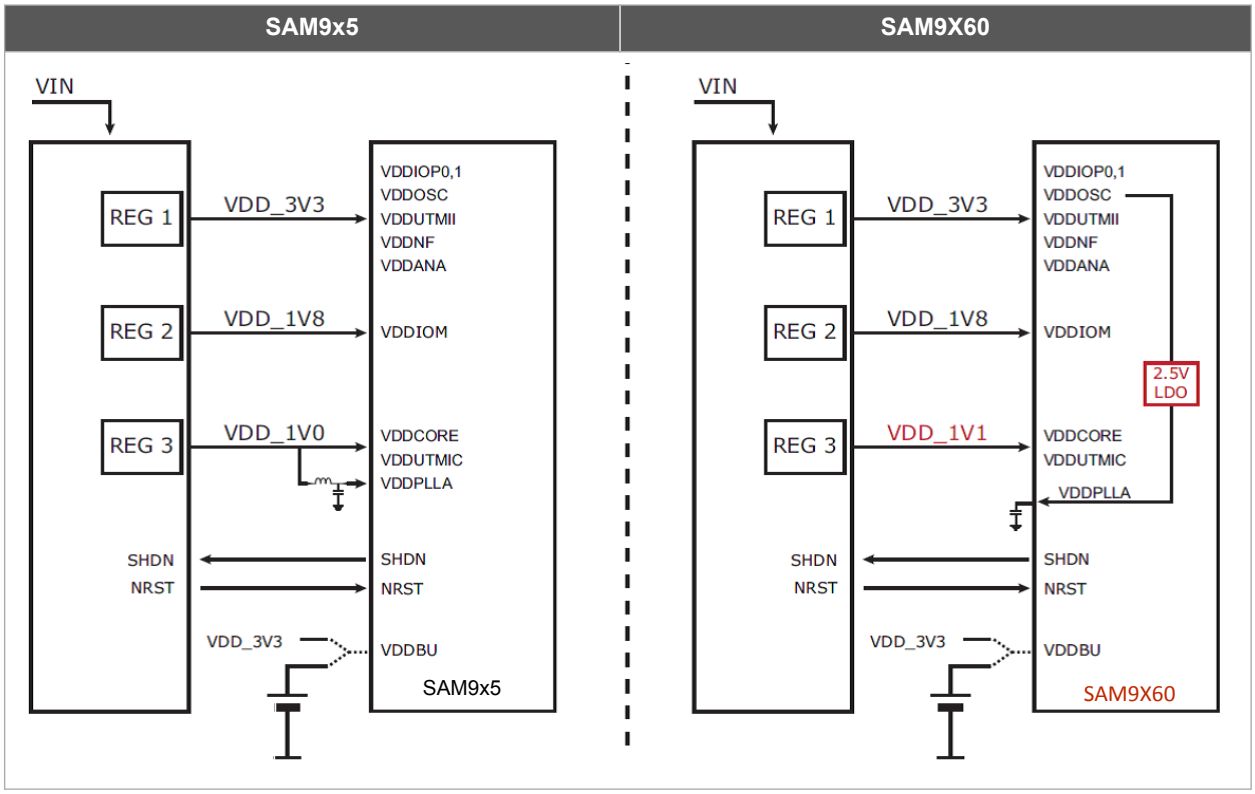
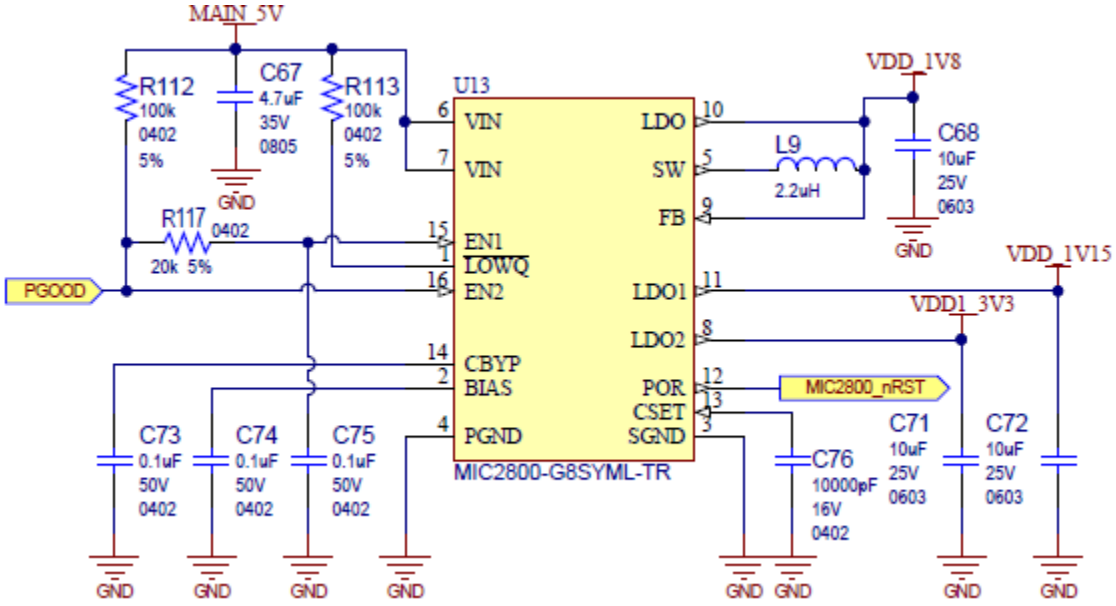


Figure 2-2. Recommended Implementation for Full CPU Speed, VDDCORE = 1.15V on SAM9X60

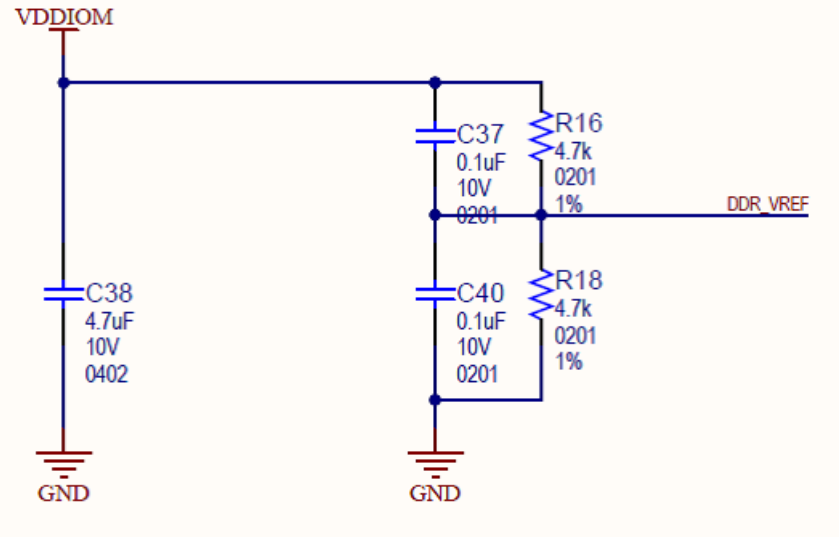


SAM9X60 includes additional power lines to support new features and new peripheral versions.

Table 2-3. SAM9X60 New Power Lines

Power Rail	SAM9x5	SAM9X60
DDR_VREF	–	Must follow VDDIOM/2
VDDQSPI	–	1.7-3.6V, 1.8V or 3.3V typical

Figure 2-3. Recommended DDR_VREF Generation on SAM9X60



2.3 Power Sequences

New simplified power-up and power-down sequences apply on SAM9X60. Refer to the SAM9X60 data sheet for more details.

2.4 Clocks

The SAM9X60 crystal oscillator supports a wider range of external crystals. Refer to the SAM9X60 data sheet for detailed electrical recommendations.

Table 2-4. SAM9x5 vs. SAM9X60 Crystal Clocks

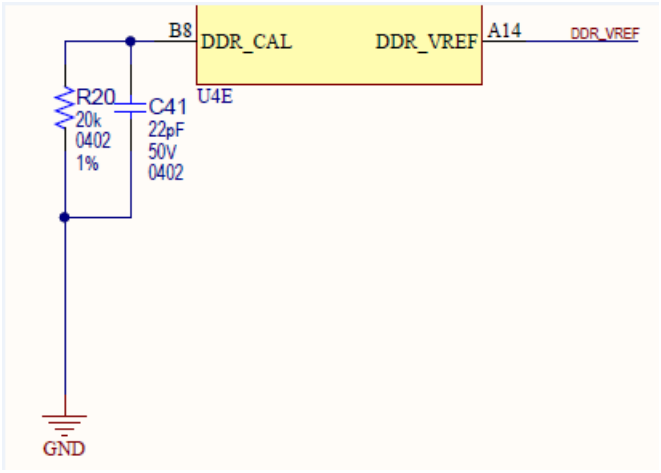
SAM9x5	SAM9X60
12 to 16 MHz crystal	12 to 48 MHz crystal

Note: The engineering sample ROM code has crystal detection limitations, so only a 24 MHz crystal must be used if a Non-Volatile Memory (NVM) is programmed via USB.

2.5 DDRC

The SAM9X60 device embeds a DDR PHY interface with calibrated output impedance. Compared to SAM9x5 designs, the serial resistors can be removed from the PCB DDR I/O lines. Calibration is done using a resistance connected to the DDR_CAL signal. Refer to the SAM9X60 data sheet for details.

Figure 2-4. SAM9X60 Recommended DDR_CAL and DDR_VREF



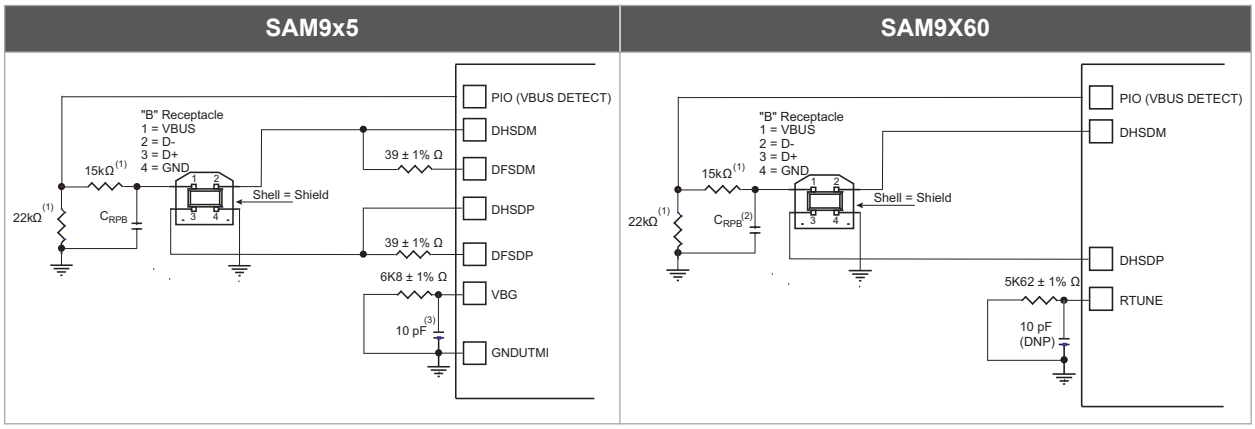
2.6 NAND Flash Memory

The PMECC that computes the ECC supports only 8-bit NAND Flash memories, so using 16-bit NAND Flash memories for new designs is not recommended.

2.7 USB

On SAM9X60, Full Speed and High Speed signals are merged. Resistors on Full Speed signals are integrated into the USB peripherals. No external resistors are needed. The capacitor appears on the schematic but it is optional. It can be added in harsh environments.

Figure 2-5. Typical USB Implementations



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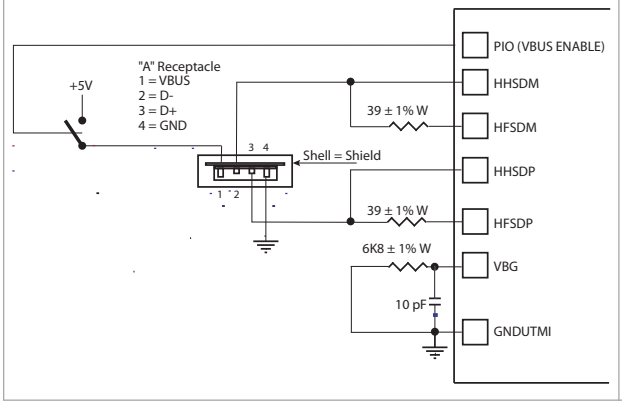
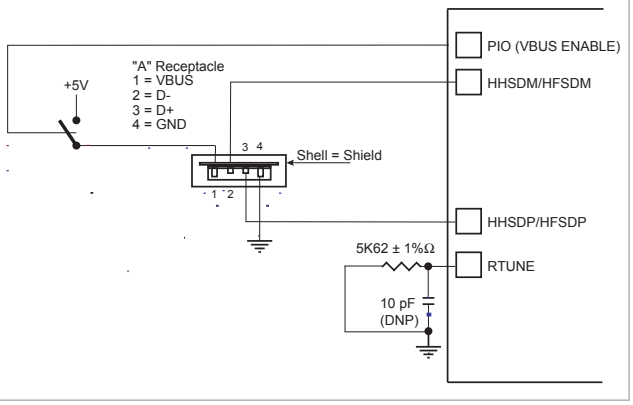
SAM9x5	SAM9X60
	

3. Peripheral Multiplexing on I/O Lines

Peripheral multiplexing on I/O lines is fully compatible: each SAM9x5 peripheral has an equivalent on SAM9X60.

SAM9X60 features new peripherals on existing lines, and new peripherals on new lines.

Table 3-1. Peripheral Enhancements and Additions

PIO Line	SAM9x5 Function	SAM9x5 Peripheral ID	SAM9X60 Function	SAM9X60 Peripheral ID
–	USART0	5	FLEXCOM0(1)	5
–	USART1	6	FLEXCOM1(1)	6
–	USART2	7	FLEXCOM2(1)	7
–	SPI0	13	FLEXCOM4(1)(2)	13
–	SPI1	14	FLEXCOM5(1)(2)	14
–	TWI0	9	FLEXCOM6(3)	9
–	TWI2	11	FLEXCOM8(3)	11
PA24-27	–	–	CLASSD	42
PB19-23	–	–	I2SMCC	34
PB19-24	–	–	QSPI	35
PB19-20	–	–	FLEXCOM11(3)	32
PB21-22	–	–	FLEXCOM12(3)	33
–	TWI1	10	FLEXCOM7(3)	10
–	UART0	15	FLEXCOM9(3)	15
	UART1	16	FLEXCOM10(3)	16
PC22-26, PC30	–	–	FLEXCOM3(1)	8

Note:

1. This fully-featured FLEXCOM enables USART, SPI and TWI.
2. Other IOSETs are available for some signals.
3. This FLEXCOM reduced to two wires enables UART and TWI.

4. Software Migration

This section describes the software changes that are likely to be required to migrate from SAM9x5 to SAM9X60. For any software samples, refer to Linux® or software package deliveries.

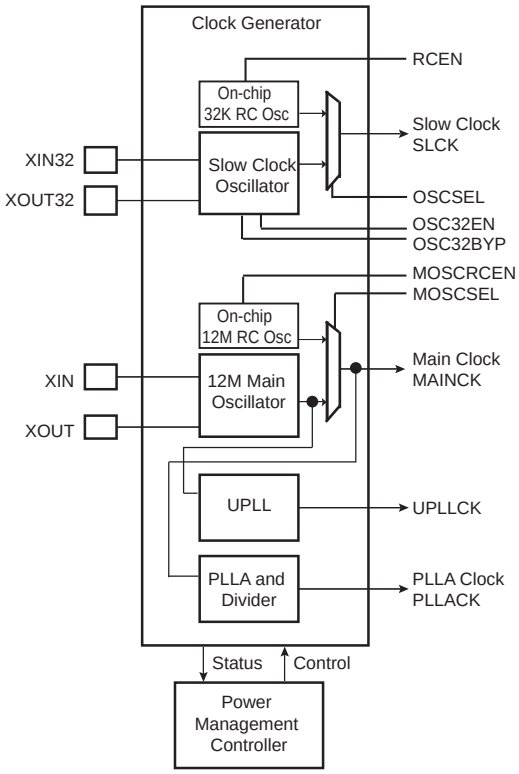
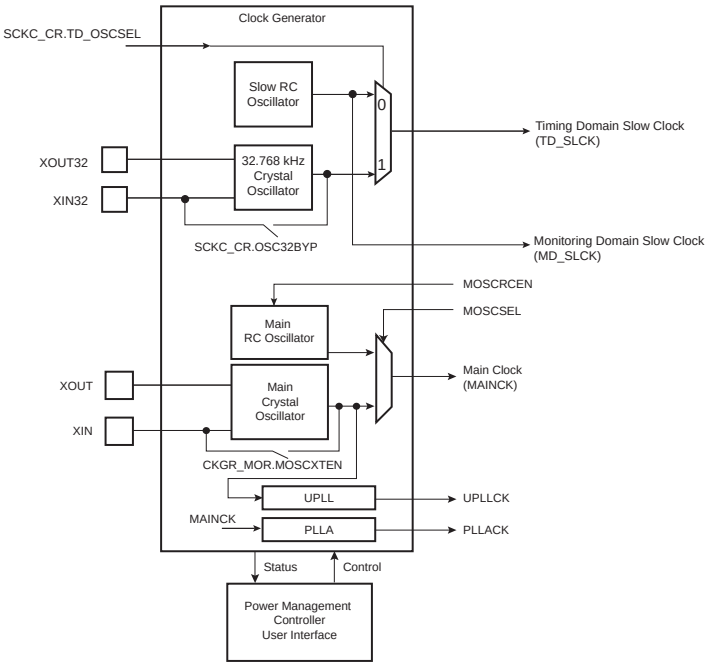
4.1 Core/Bus Frequency

Updated any timings or delay calculations.

4.2 Clocks

SAM9x5 and SAM9X60 support different crystals and manage PLLs differently. SAM9X60 provides generic clocks for most peripherals. Power Management Controller interfaces differ also, so software modifications are required.

Table 4-1. SAM9x5 vs. SAM9X60 Clocks

SAM9x5	SAM9X60
Clock Settings	
32 KHz RC can be stopped 12 to 16 MHz crystal	32 KHz RC always on 12 to 48 MHz crystal
	 **Note:** The engineering sample ROM code has crystal detection limitations, so only a 24 MHz crystal must be used if a Non-Volatile Memory (NVM) is programmed via USB.

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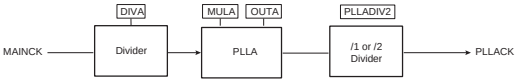
SAM9x5	SAM9X60
	Use the internal 32 kHz RC oscillator to clock safely peripherals that do not need accuracy: • Watchdog timer • APMC • Reset controller • Shutdown controller Only the RTC is connected to the external 32 KHz oscillator.
Clock Setting Registers	
CKGR_MOR sets the main oscillator. PMC_MCKR sets CPU and MCK clocks.	CKGR_MOR includes additional bits: • ULP1 enables ULP1 low-power mode. • XT32KFME enables 32 KHz crystal frequency monitor. • BMCKIC enables MCK monitoring. • PMC_OCR performs Main RC calibration. • PMC_MCKLIM programs MCK monitor limits. • PMC_CPU_CKR sets CPU and MCK clocks.
PLL Settings	
400 to 800 MHz PLLs PLLs are not fractional. PLLA clock ouput is: PLLACK = MAINCK / DIVA * MULA  UPLL requires a 12 MHz crystal to generate 12x40 = 480 MHz frequency.	600 to 1200 MHz PLLs PLLs are fractional. 12 MHz is not required to ensure USB clock accuracy. The COREPLLCK operating frequency is defined as: $f_{COREPLLCK} = f_{ref}\left(MUL + 1 + \frac{FRACR}{2^{22}}\right)$ The PLLA clock frequency is defined by the following formula: $f_{PLL\ Clock} = \frac{f_{COREPLLCK}}{(DIVPMC + 1)}$ The UPLL clock frequency is defined by the following formula: $f_{PLL\ Clock} = \frac{f_{COREPLLCK}}{2}$ Spread spectrum is embedded.

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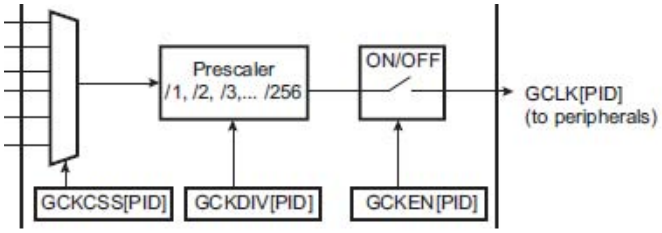
SAM9x5	SAM9X60
PLL Setting Registers	
CKGR_PLLAR and PMC_PLLICPR set PLLA. PMC_USB sets USB clock.	PMC_PLL_CTRL0, PMC_PLL_CTRL1 and PMC_PLL_ACR configure PLLs. PMC_PLL_SSR sets the spread spectrum. PMC_PLL_UPDT applies the modification in a glitch-free manner to the selected PLLs. ID = 0 for system PLL (former PLLA) ID = 1 for USB PLL PMC_USB sets USB clock.
Peripheral Clock Settings	
PMC_PCR enables and disables a peripheral using its identifier (PID). Alternatively, PMC_PCER and PMC_PCDR can be used to enable and disable a peripheral using the PID. The peripheral clock status is shown in PMC_PCSR.	Only PMC_PCR can be used. The peripheral clock status is shown in PMC_PCR, or alternatively in PMC_CSRx.
Generic Clock Settings	
No generic clock is available.	A generic clock is available for most (serial) peripherals, making it possible to use: • a lower frequency for baud rates than for the peripheral clock, • serial baud rates that are not synchronous with the system clock, nor with other serial baud rates. Source, divider and enable are selectable in PMC_PCR.  The generic clock status is shown in PMC_PCR, alternatively in PMC_GCSRx. Peripherals supporting the generic clocks are listed in the datasheet, in table Peripherals Identifiers.

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SAM9x5	**SAM9X60**
Programmable Clock Settings	
PMC_SCER and PMC_SCDR enable/disable PCKs.	Bitfield size is different. PMC_SCER and PMC_SCDR enable/disable PCKs.

4.3 Power Management - ULP1

SAM9X60 introduces Ultra-Low Power 1 (ULP1) mode. In this mode, all clocks in the system are fed with the main clock (internal fast 12 MHz RC oscillator) and the main crystal is disabled. Power consumption is lower than ULP0 and wake-up time is far shorter (a few µs vs. a few ms in ULP0). The system wakes up with a programmable event (RTC/RTT alarm, USB Resume, Wake-On-LAN, WKUP1..13 lines).

One major use case for ULP1 is the support of USB device Suspend mode. In such applications, the MPU is powered by the USV VBUS rail. The total power allocated to a USB power system is 12.5 mW at 5V.

If USB Host applications are used, the suspend control of the USB PHYs must be implemented in the Special Function Registers (SFR), as they are not managed by the EHCI/OHCI peripherals.

ULP1 is controlled with bit PMC_MOR.ULP1.

4.4 Matrix

Due to architecture upgrade and peripheral modifications, SAM9x5 and SAM9X60 master/slave tables differ. Matrix configuration software updates are required accordingly. Refer to the SAM9X60 data sheet for more details.

4.5 SRAM and L1 Cache Sizes

SRAM size is doubled to 64 Kbytes and I + D L1 cache sizes are doubled to 32 + 32 Kbytes. Modify cache management routines accordingly.

4.6 DMA

DMA is updated to a more featured version. Two 8-channel DMAs are replaced by one 16-channel DMA. Update software accordingly.

4.7 USB Device

USB device DPRAM is now 16,448 bytes, versus 4 Kbytes on SAM9x5. No dynamic allocation is needed; each endpoint has its own dedicated area in DPRAM.

4.8 Graphics

The LCD controller is improved. The hardware cursor layer is replaced by an overlay. Resolution is better (1024x768 vs. 800x600). Update software accordingly.

SAM9X60 introduces GFX2D, a new peripheral performing memory data move operations. Software is to be developed in order to support GFX2D and allow better performances for graphic operations. GFX2D peripheral identifier (PID) is 36.

4.9 Serial

Any SAM9x5 serial link such as USART, UART, SPI or I^2C is updated to a FLEXCOM. Each FLEXCOM includes all serial features. As the software for USART, SPI and TWI are compatible, to work properly on SAM9X60 the only

modification consists in selecting the mode (USART, SPI, TWI) in the FLEX_MR register. Note that the FLEXCOM SPI function does not embed all SPI Chip Selects. NPCS1, NPCS2 and NPCS3 are no longer supported. Update software accordingly.

FLEXCOM3, FLEXCOM11 and FLEXCOM12 are added with respective PIDs 8, 31 and 32.

The SAM9X60 device features a 4-bit QSPI peripheral (PID 35). The QSPI clock is enabled and disabled using bits PMC_SCER.QSPICLK and PMC_SCDR.QSPICLK, respectively.

4.10 DDRC

Due to the following upgrades, the whole DDR controller initialization must be modified.

1. Different controllers are used: SAM9x5 embeds one DDR controller that supports DDR2-SDRAM and SDR-SDRAM, while SAM9X60 embeds two separate controllers:
   - A multiport DDR controller to support DDR2-SDRAM and LPDDR1-SDRAM
   - An SDRAM controller to support SDR-SDRAM and LPSDR-SDRAM
2. On SAM9X60, SDR-SDRAM calibration is done automatically once at the initialization phase. DDR2-SDRAM and LPDDR1-SDRAM calibrations can be done at any time using the MPDDRC I/O Calibration register (MPDDRC_IO_CALIBR).

4.11 ADC

10-bit ADC is replaced by 12-bit ADC with more integration features, mainly PWM event and TC output internal triggers and PWM fault input drive. Update software accordingly.

Refer to the SAM9X60 data sheet for more details.

4.12 SDMMC

SDMMC is an evolution of HSMCI with a modified user interface. Features are upgraded and require software modification.

4.13 Audio

Multichannel I^2S and CLASSD are added to existing SSC. Respective PIDs are 34 and 42.

Refer to 3. Peripheral Multiplexing on I/O Lines and to the SAM9X60 data sheet for more details.

4.14 Security

Security peripherals (TDES, AES, SHA, TRNG and Secure Boot) are added in SAM9X60. Respective PIDs are 40, 39, 41 and 38.

An OTP area is available to store user's certificates, keys and configuration.

A "disable JTAG" OTP bit is added to configuration bits.

An OTP Emulation mode is embedded to ease development. Use OTP with stable software only.

Refer to the SAM9X60 data sheet for more details.

4.15 ROM Code

The SAM9X60 ROM code features a secure bootloader supporting code integrity check, code authentication and code encryption.

A boot sequence register is added to define the NVM boot order. The boot select controller (BSC) is a 32-bit register in OTP. It is a scratchpad used by the boot program to store and read the bootable media location. It features a 16-bit write protection key on the MSBs and a 16-bit scratchpad on the LSBs.

Refer to the SAM9X60 data sheet for more details.

5. Fixed SAM9x5 Errata

The following SAM9x5 errata are fixed in SAM9X60. For further details on each erratum, refer to the SAM9x5 data sheets.

- EBI: Data lines are Hi-Z after reset
- RSTC: Reset during SDRAM accesses
- SMC: SMC DELAY I/O registers are write-only
- UHPHS/UDPHS: Bad Lock of the USB High speed transceiver DLL
- LCDC: LCDC PWM is not usable
- RTC: Interrupt Mask Register cannot be used
- SSC swaps channels in underrun/overrun conditions

6. Revision History

6.1 DS00003166A - 10/2019

First issue.

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