AN1865

MEC140x System BIOS Porting Guide

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INTRODUCTION

This document provides BIOS engineers a quick reference to port System BIOS in support of these MEC140x I/O devices: EMI 0, 8042 Emulated Keyboard Controller, ACPI EC0, ACPI EC1, ACPI EC2, ACPI EC3, ACPI PM1, Legacy Port92/GateA20, UART 0, Mailbox Interface, LPC Interface (Configuration Port), Port 80 BIOS Debug Port 0, Port 80 BIOS Debug Port 1.

References

The following document should be referenced when using this application note. Please contact your MCHP representative for availability.

- MEC140x Data Sheet (09-24-14) or current

1.0 Contents

This guide consists of the following sections:

1.1 Terminology

This document contains the following terms, defined here for the purpose of convenience and general agreement:

TABLE 1-1: TERMS

Term	Description
System Host	Refers to the external CPU that communicates with this device via the LPC Interface.
Logical Devices	Logical Devices are LPC accessible features that are allocated a Base Address and range in LPC I/O address space.
Runtime Register	Registers are directly I/O accessible by the System Host via the LPC interface.
Configuration Registers	Registers that are only accessible in CONFIG_MODE.
EC_Only Registers	Registers that are only accessible by the System Host. They are only accessible by an internal embedded controller.
ACPI_EC	The EC host corresponding to the ACPI specification interface to the EC.
ACPI_OS	The LPC host corresponding to the ACPI specification interface to the “System Host Interface to OS”. ACPI_OS terminology is not meant to distinguish the ACPI System Management from Operating System, but to point to the hardware path upstream towards the CPU.

2.0 OBTAINING THE MEC140X CONFIGURATION BASE ADDRESS

Logical devices are configured through three Configuration Access Ports (CONFIG, INDEX and DATA) (see Table 2-1, "MEC140x Configuration Access Ports"). The BIOS uses these ports to initialize the logical devices at POST.

The Base Address of the Configuration Access Ports is determined by the Base Address Register (BAR) that corresponds to Logical Device Ch, the LPC Interface CR60h-CR63h. The default I/O address is 2Eh and 2Fh.

The BAR (Section 6.2, "Base Address Registers," on page 7) of Configuration Port can be relocated through the Configuration Registers for LDN Ch (LPC Interface) 60h-63h, the bit[15]: Valid must be “1”.

TABLE 2-1: MEC140X Configuration Access Ports

Port Name	Relative Address	Type	Port Name
CONFIG PORT	Configuration Access Ports Base Address + 0	Write	CONFIG PORT
INDEX PORT	Configuration Access Ports Base Address + 0	Read/Write	INDEX PORT
DATA PORT	Configuration Access Ports Base Address + 1		DATA PORT

2.1 Example: Relocating the BAR of Logical Device 0Ch to 4Eh

The following is a configuration register programming example written in Intel 8086 assembly language.

```
;--------------------------.
; Enter Configuration State |
;--------------------------'
MOV       DX, 02Eh ; Config_Port_Base_Address
MOV       AX, 055h ; Config Entry Key
OUT       DX, AL
;------------------------.
; Configure Base Address,|
; Logical Device C       |
;------------------------'
MOV       DX, 02Eh ; Config_Port_Base_Address
MOV       AL, 07h
OUT       DX, AL   ; Point to Logical Device Number Register
MOV       DX, 02Fh ; Config_Port_Base_Address+1
MOV       AL, 0Ch
OUT       DX, AL   ;Point to Logical Device C
;-------------------------------------------------------------------------.
; Configure both CR62 and CR63 to relocate the Base Address Register to 4Eh|
;-------------------------------------------------------------------------.
MOV       DX, 02Eh ; Config_Port_Base_Address
MOV       AL, 062h ; CR62
OUT       DX, AL   ; Point to Base Address Register
MOV       DX, 02Fh ; Config_Port_Base_Address+1
;-------------------------------------------------------.
;Read the LPC I/O Configuration Register Port (IOCR-Port)|
;-------------------------------------------------------.
IN        AL,DX    ; (Optional)It should be 2Eh

MOV       AL, 04Eh
OUT       DX, AL   ; Update CR62

MOV       DX, 02Eh ; Config_Port_Base_Address
MOV       AL, 063h ; CR63
OUT       DX, AL   ; Point to CR63
MOV       DX, 02Fh ; Config_Port_Base_Address+1
MOV       AL, 00h
OUT       DX, AL   ; Update CR63

;--------------------------.
; Exit Configuration State |
;--------------------------'
MOV       DX, 02Eh ; Config_Port_Base_Address
MOV       AX, 0AAh ; Config Exit Key
OUT       DX, AL
```

Note: If you want to relocate the BAR of Logical Device 0Ch to 164Eh, use the example initialization to configure CR63 to 16h.

3.0 HOST LOGICAL DEVICES

The Logical Devices physically located in the MEC140x are identified in Table 3-1, "Host Logical Devices on MEC140x" and Table 4-1, "Basechip Logical Devices". The base addresses of logical devices with registers located in LPC I/O space, including the Keyboard Controller, can be moved through the configuration registers located in the LPC Interface Configuration Register Space.

TABLE 3-1: Host Logical Devices on MEC140X

Logical Device Number	Logical Devices	LPC I/O Runtime Access	LPC I/O Configuration Access
0h	EMI 0	yes	no
1h	8042 Emulated Keyboard Controller	no	yes
3h	ACPI EC 0	yes	no
4h	ACPI EC 1	yes	no
5h	ACPI PM 1	yes	no
6h	Legacy Port92/GateA20	yes	yes
7h	UART 0	yes	yes
9h	Mailbox Interface	yes	no
Ah	ACPI EC 2	yes	no
Bh	ACPI EC 3	yes	no
Ch	LPC Interface (Configuration Port)	yes	yes
15h	Port 80 BIOS Debug Port 0	yes	yes
16h	Port 80 BIOS Debug Port 1	yes	yes

4.0 BASECHIP LOGICAL DEVICES

Logical devices described in this section are peripherals that are located on the MEC140x basechip and are accessible to the Host over the LPC bus.

Each logical device on the MEC140x can have a set of Runtime Registers and a set of Configuration Registers. The difference between Runtime and Configuration registers is that the Host can access Runtime Registers by a direct I/O address, while it can only access Configuration Registers through a configuration port.

Note: The Embedded Controller (EC) can access all Configuration Registers and all Runtime Registers directly.

The Logical Device Numbers for the Logical Devices resident in the MEC140x are listed in Table 8-2, "MEC140x Configuration Register Map".

TABLE 4-1: Basechip Logical Devices

Logical Device Number	Logical Device	Logical Device Configuration Register Map in Table 8-2 on page 13
0h	EMI 0	Configuration Registers for LDN 0h (EMI 0)
1h	8042 Emulated Keyboard Controller	Configuration Registers for LDN 1h (Keyboard Controller (8042))
3h	ACPI EC 0	Configuration Registers for LDN 3h (ACPI EC Channel 0)
4h	ACPI EC 1	Configuration Registers for LDN 4h (ACPI EC Channel 1)
5h	ACPI PM 1	Configuration Registers for LDN 5h (ACPI PM 1)
6h	Legacy Port92/GateA20	Configuration Registers for LDN 6h (Legacy Port92/GateA20)
7h	UART 0	Configuration Registers for LDN 7h (UART 0)
9h	Mailbox Interface	Configuration Registers for LDN 9h (Mailbox Interface)
Ah	ACPI EC 2	Configuration Registers for LDN Ah (ACPI EC Channel 2)
Bh	ACPI EC 3	Configuration Registers for LDN Bh (ACPI EC Channel 3)
Ch	LPC Interface (Configuration Port)	Configuration Registers for LDN Ch (LPC Interface)
15h	Port 80 BIOS Debug Port 0	Configuration Registers for LDN 15h (Port 80 BIOS Debug Port 0)
16h	Port 80 BIOS Debug Port 1	Configuration Registers for LDN 16h (Port 80 BIOS Debug Port 1)

Note: Logical Devices EMI 0, ACPI EC0, ACPI EC1, ACPI EC2, ACPI EC3, ACPI PM1, UART 0, Mailbox Interface, Port 80 BIOS Debug Port 0 and Port 80 BIOS Debug Port 1 Base Address Registers (BARs) must be located within the Generic Decode Ranges of the Chipset. For example, see Section 11.0, "Intel LPC Interface Bridge Register Initialization", items 4 through 7.

5.0 CONFIGURATION REGISTER PROGRAMMING

The MEC140x contains the Global Configuration Registers CR07-CR2F and the Logical Device Configuration registers. After the MEC140x device enters the Configuration State, the Configuration Registers can be programmed by first writing the register index number (0x07 - 0x2F) to the Configuration Select Register (CSR) through the INDEX PORT and then writing or reading the Configuration Register contents through the DATA PORT. The Configuration Register access remains enabled until the Configuration State is explicitly exited.

CONFIGURATION SEQUENCE

To program the configuration registers, the following sequence must be followed:

1. Enter Configuration State.
2. Configure the Configuration Registers.
3. Exit Configuration State.

5.1 Entering the Configuration State

The INDEX and DATA ports are effective only when the chip is in the Configuration State. The device enters the Configuration State when the Config Entry Key is successfully written to the CONFIG PORT.

Config Entry Key = < 55h>

5.2 Configuring the Configuration Registers

Configuration registers are accessed in two steps:

1. Write the index of the Logical Device Number Configuration Register (that is, 07h) to the INDEX PORT and then write the number of the desired logical device to the DATA PORT.
2. Write the address of the desired configuration register within the logical device to the INDEX PORT and then write or read the configuration register through the DATA PORT.

Note:	If accessing the Global Configuration Registers, step (1) is not required.

1. Any write to an undefined or reserved configuration register is terminated normally on the LPC bus without any modification of state in the basechip or companion device. Any read to an undefined or reserved configuration register returns FFh.

5.3 Exiting the Configuration State

The device exits the Configuration State when the following Config Exit Key is successfully written to the CONFIG PORT address.

Config Exit Key = < AAh>

5.4 Configuration Register Programming Example

Please see Section 2.1, "Example: Relocating the BAR of Logical Device 0Ch to 4Eh" to access the configuration registers.

6.0 CONFIGURING RUNTIME REGISTER ADDRESSES

6.1 Runtime Registers

Runtime Registers are registers that are accessible to the Host within the Host I/O address space. Runtime registers all reside within the first 256 bytes of a 1K Logical Device address frame. The Host accesses these registers with 8-bit LPC I/O accesses. The Host I/O addresses are determined by a block of Base Address Registers located in the LPC Logical Device. The Embedded Controller can access all the Runtime Registers as well.

6.2 Base Address Registers

Each Logical Device has a Base Address Register (BAR). These BARs are located in blocks of configuration registers in Logical Device 0Ch. On every LPC bus I/O access all Base Address Registers are checked in parallel and if any matches the LPC I/O address the MEC140x device claims the bus cycle.

Note 6-1 Software should ensure that no two BARs map the same LPC I/O address.

Each BAR is 32-bits wide. The format of each BAR is summarized in Table 6-1, "I/O Base Address Register Format".

TABLE 6-1: I/O BASE ADDRESS REGISTER FORMAT

BYTE3 BIT	D31	D30	D29	D28	D27	D26	D25	D24
BIT NAME	LPC Host Address, most significant bits							
BYTE2 BIT	D23	D22	D21	D20	D19	D18	D17	D16
BIT NAME	LPC Host Address, least significant bits							
BYTE1 BIT	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	Valid	Device	Frame					
BYTE0 BIT	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Mask							

6.2.1 MASK

These 8 bits are used to mask off address bits in the address match between an LPC I/O address and the Host Address field of BARs, as described in Section 4.8.2.1, “I/O Transactions” of the latest MEC140x data sheet. A block of up to 256 8-bit registers can be assigned to one base address.

6.2.2 FRAME

These 6 bits are used to specify a logical device frame number within a bus. This field is multiplied by 400h to provide the frame address within the peripheral bus address. Frame values for frames corresponding to logical devices that are not present on the device are invalid.

6.2.3 DEVICE

This bit combined with FRAME constitute the Logical Device Number. DEVICE identifies the physical location of the logical device. This bit should always be set to 0.

6.2.4 VALID

If this bit is 1, the BAR is valid and participates in LPC matches. If it is 0, this BAR is ignored.

6.2.5 HOST_ADDRESS

These 16 bits are used to match LPC I/O addresses.

6.3 Logical Device IO_BAR Description

Table 6-2, "MEC140x I/O Base Address Registers Default Values", lists the IO Base Address Registers (IO_BAR) for all logical devices on the MEC140x base chip.

TABLE 6-2: MEC140X I/O BASE ADDRESS REGISTERS DEFAULT VALUES

LPC Offset	RESET Default	Bits [D31:D16] DEFAULTLPC I/O Host Address	Bits [D15] VALID	Bits [D14] DEVICE	Bits [D13:D8] FRAME (Note 6-3)	Bits [D6:D0] MASK (Note 6-4)	Description
60h	002E_0C01h	002Eh (Note 6-2)	0	0	C	1	Logical Device 0Ch: LPC Interface (Configuration Port)
64h	0000_000Fh	0000h	0	0	0	F	Logical Device 00: EMI 0
68h	0060_0104h	0060h	0	0	1	4	Logical Device 01h: 8042 Emulated Keyboard Controller
6Ch	0062_0304h	0062h	0	0	3	4	Logical Device 03h: ACPI EC 0
70h	0066_0407h	0066h	0	0	4	7	Logical Device 04h: ACPI EC 1
74h	0000_0507h	0000h	0	0	5	7	Logical Device 05h: ACPI PM 1
78h	0092_0600h	0092h	0	0	6	0	Logical Device 06h: Legacy Port92/ GateA20
7Ch	0000_0707h	0000h	0	0	7	7	Logical Device 07h: UART 0
80h	0000_0901h	0000h	0	0	9	1	Logical Device 09h: Mailbox Interface
84h	0000_0A07h	0000h	0	0	A	7	Logical Device 0Ah: ACPI EC 2
88h	0000_0B07h	0000h	0	0	B	7	Logical Device 0Bh: ACPI EC 3
8Ch	0000_1500h	0000h	0	0	15	0	Logical Device 15h: Port 80 BIOS Debug Port 0
90h	0000_1600h	0000h	0	0	16	0	Logical Device 16h: Port 80 BIOS Debug Port 1

Note 6-2 The default Base I/O Address of the Configuration Port can be relocated by programming the BAR register for Logical Device Ch (LPC/Configuration Port) at offset 60h.

Note 6-3 The FRAME and MASK fields for these legacy devices are not used to determine which LPC I/O addresses to claim. The address range match is maintained within the blocks themselves.

Note 6-4 The ACPI-ECx Mask bit field is a read/write bit field. All other MASK bit fields are read-only as defined in the register description.

6.4 DEVICE Memory Base Address Registers (DEV_MEM_BARS)

Some Logical Devices have a Memory Base Address Register. These Device Memory BARs are located in blocks of Configuration Registers in Logical Device 0Ch, in the AHB address range FF_33C0h through FF_33FFh.

Note 6-5 Software should insure that no two BARs map the same LPC memory address. If two BARs do map to the same address, the BAR_Conflict bit in the Host Bus Error Register is set when an LPC access targets the BAR Conflict address. An EC interrupt can be generated.

Each M-BAR is 48-bits wide. The format of each M-BAR is summarized in Table 6-3, "MEC140x Memory Base Address Register Format". An LPC memory request is translated by the M-BAR into an 8-bit read or write transaction on the AHB bus. The 32-bit LPC memory address is translated into a 24-bit AHB address

The Base Address Register Table is itself part of the AHB address space. It resides in the Configuration quadrant of Logical Device Ch, the LPC Interface.

TABLE 6-3: MEC140x Memory Base Address Register Format

BYTE5 BIT	D47	D46	D45	D44	D43	D42	D41	D40
BIT NAME	LPC Host Address Bits[31:24]							
BYTE4 BIT	D39	D38	D37	D36	D35	D34	D33	D32
BIT NAME	LPC Host Address Bits[23:16]							
BYTE3 BIT	D31	D30	D29	D28	D27	D26	D25	D24
BIT NAME	LPC Host Address Bits[15:08]							
BYTE2 BIT	D23	D22	D21	D20	D19	D18	D17	D16
BIT NAME	LPC Host Address Bits[07:00]							
BYTE1 BIT	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	Valid	Device	Frame					
BYTE0 BIT	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Mask							

Note 6-6 The field definitions are the same as Table 6-1, "I/O Base Address Register Format" except that the HOST_ADDRESS field LPC memory cycle address is 32-bit instead of the I/O cycle 16-bit.

6.5 MEC140x Memory Base Address Register Table

Table 6-4, "Device Memory Base Address Registers on MEC140X", lists the Base Address Registers for logical devices that have LPC memory access in the MEC140x.

- LPC Memory cycle access is controlled by LPC Memory Base Address Registers. LPC Memory BAR registers are located in LDN Ch (LPC Interface) at AHB base address FF_3300h starting at offset 3C0h.

TABLE 6-4: DEVICE MEMORY BASE ADDRESS REGISTERS ON MEC140X

				Base Address Register Bit Field Descriptions				
				Bits [D47:D16]	Bit [D15]	Bit [D14]	Bits [D13:D8]	Bits [D6:D0]
Offset	Logical Device Number (hex)	Logical Devices	Reset Default	Default LPC Mem Host Address	VALID	DEVICE	FRAME	MASK (Note 2)
C0h	0	EMI 0	0000_0000_000F	0000_0000	0	0	0	F
C6h	3	ACPI EC0	0000_0062_0304	0000_0062	0	0	3	4
CCh	4	ACPI EC1	0000_0066_0407	0000_0066	0	0	4	7
D2h	9	Mailbox Interface	0000_0000_0901	0000_0000	0	0	9	1
D8h	A	ACPI EC2	0000_0000_0A07	0000_0000	0	0	A	7
DEh	B	ACPI EC3	0000_0000_0B07	0000_0000	0	0	B	7

6.5.1 SRAM MEMORY BAR CONFIGURATION

In addition to mapping LPC Memory transactions into Logical Devices, Memory transactions can be mapped into internal address space, as configured by the SRAM Memory BARs. The LPC Host Controller also has access to the SRAM data via the SRAM Memory BARs. LPC Memory cycles are single byte read or writes that occur in a 32-bit address space. The LPC block will claim LPC memory cycles that match the programmed SRAM Memory BAR Register if the bit[7]:VALID bit in the SRAM Memory BAR Configuration is set to 1. No memory cycles will be claimed if this is cleared.

The LPC interface can claim up to a 4 KB block of memory addresses and map them to the internal address space. The location of the block of memory in the 32-bit internal space, as well as access to it, is controlled by the EC, using the SRAM Memory Host Configuration Register.

The firmware programs the base address of internal memory space in SRAM Memory Host Configuration Register, which is mapped to the LPC memory address programmed by the Host in the SRAM Memory BAR register. The firmware also programs the size of the memory to be accessed.

Please see Section, “Claiming LPC Memory Transactions,” of the latest MEC140X Data Sheet.

TABLE 6-5: SRAM MEMORY BAR CONFIGURATION REGISTERS

Configuration Register	Offset	Size	Notes
SRAM Memory BAR	A0h	32	
SRAM Memory BAR Configuration	A4h	32	

Note 1: See Section 4.9.4, “SRAM MEMORY BAR,” of the latest MEC140x Data Sheet.

2: See Section 4.9.5, “SRAM MEMORY CONFIGURATION,” of the latest MEC140x Data Sheet.

7.0 SERIRQ INTERRUPTS

The MEC140x can route Logical Device interrupts onto SERIRQ stream frames IRQ[0:15]. Routing is controlled by the SERIRQ Interrupt Configuration Registers. There is one SERIRQ Interrupt Configuration Register for each accessible SERIRQ Frame (IRQ); all 16 registers are listed in Table 7-2, "SERIRQ Interrupt Configuration Register Map". Each SERIRQ Interrupt Configuration Register controls a series of multiplexors that route to a single Logical Device interrupt. The format for each SERIRQ Interrupt Configuration Register is described in Table 7-1, "SERIRQ Interrupt Configuration Register Format". Each Logical Device can have up to two LPC SERIRQ interrupts. When the MEC140x is polled by the Host, each SERIRQ frame routes the level of the Logical Device interrupt (selected by the corresponding SERIRQ Interrupt Configuration Register) to the SERIRQ stream.

Note: Two Logical Devices cannot share a Serial IRQ.

The Host can access the SERIRQ Interrupt Configuration Registers with 8-bit accesses. The EC can access the SERIRQ Interrupt Configuration Registers as 32-bit, 16-bit across 8-bit boundary, or as individual 8-bit accesses.

TABLE 7-1: SERIRQ INTERRUPT CONFIGURATION REGISTER FORMAT

BYTE0 BIT	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	Select	Device	Frame					

Note: A SERIRQ interrupt is deactivated by setting an entry in the Table 7-2, "SERIRQ Interrupt Configuration Register Map" to FFh, which is the default reset value.

7.1 FRAME

These six bits select the Logical Device as the source for the interrupt.

Note: The LPC Logical Device (Logical Device Number 0Ch) can be used by the Embedded Controller to generate a Serial Interrupt Request to the Host under software control.

7.2 DEVICE

This field should always be set to 0 in order to enable a SERIRQ.

7.3 SELECT

If this bit is 0, the first interrupt signal from the Logical Device is selected for the SERIRQ vector. If this bit is 1, the second interrupt signal from the Logical Device is selected.

Note: The Keyboard controller is the only Logical Device on the MEC140x that has a second interrupt signal. Most Logical Devices require only a single interrupt and ignore this field as result.

7.4 SERIRQ Configuration Registers

A SERIRQ interrupt is deactivated by setting an entry in the Table 7-2, "SERIRQ Interrupt Configuration Register Map" to FFh, which is the default reset value.

TABLE 7-2: SERIRQ INTERRUPT CONFIGURATION REGISTER MAP

LPC Offset	Type	Reset	Configuration Register Name
40h	R/W	FFh	IRQ0
41h	R/W	FFh	IRQ1
42h	R/W	FFh	IRQ2
43h	R/W	FFh	IRQ3
44h	R/W	FFh	IRQ4
45h	R/W	FFh	IRQ5
46h	R/W	FFh	IRQ6

TABLE 7-2: SERIRQ INTERRUPT CONFIGURATION REGISTER MAP (CONTINUED)

LPC Offset	Type	Reset	Configuration Register Name
47h	R/W	FFh	IRQ7
48h	R/W	FFh	IRQ8
49h	R/W	FFh	IRQ9
4Ah	R/W	FFh	IRQ10
4Bh	R/W	FFh	IRQ11
4Ch	R/W	FFh	IRQ12
4Dh	R/W	FFh	IRQ13
4Eh	R/W	FFh	IRQ14
4Fh	R/W	FFh	IRQ15

7.5 MEC140X SERIRQ Routing

Each SIRQ Interrupt Configuration Register controls a series of multiplexers which route a single Logical Device interrupt.The following table defines the Serial IRQ routing for each logical device implemented in the chip.

TABLE 7-3: MEC140X **LOGICAL DEVICE SIRQ ROUTING TABLE**

SIRQ Interrupt Configuration Register			Logical Device Interrupt Source	
Select	**Device**	**Frame**	**Logical Device**	**Interrupt Source**
0	0	0Ch	LPC Interface (Configuration Port)	EC_IRQ
0	0	9	Mailbox Interface	MBX_Host_SIRQ
1	0	9	Mailbox Interface	MBX_Host_SMI
0	0	1	8042 Emulated Keyboard Controller	KIRQ
1	0	1	8042 Emulated Keyboard Controller	MIRQ
0	0	3	ACPI EC 0	EC_OBF
0	0	4	ACPI EC 1	EC_OBF
0	0	0Ah	ACPI EC 2	EC_OBF
0	0	0Bh	ACPI EC 3	EC_OBF
0	0	7	UART 0	UART
0	0	0	EMI 0	Host Event
1	0	0	EMI 0	EC-to-Host

8.0 LOGICAL DEVICE CONFIGURATION/CONTROL REGISTERS

A separate set of control and configuration registers exist for each Logical Device and is selected with the Logical Device # Register (07h). The Logical Devices are listed in Table 4-1, "Basechip Logical Devices", and the registers within each Logical Device are listed in Section 8.2, "Configuration Register Map".

8.1 Logical Device Activation

Many Logical Devices have a register, called Activate, that is used to activate the Logical Device. When a Logical Device is inactive, it is powered down. The format for the Activate Register is shown in Table 8-1, "Activate Register".

Activating a Logical Device does not cause the MEC140x to claim LPC addresses associated with the device. Address matching for all Logical Devices is enabled or disabled in the LPC Logical Device.

TABLE 8-1: ACTIVATE REGISTER

HOST OFFSET	BYTE0: 30h					8-bit	**HOST SIZE**	
POWER	VTR					00b	nSYS_RST **DEFAULT**	
BYTE0 BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TYPE	R	R	R	R	R	R	R	R/W
BIT NAME	Reserved							Activate

8.1.1 ACTIVATE

When this bit is 1, the logical device is powered and functional. When this bit is 0, the logical device is powered down and inactive.

8.2 Configuration Register Map

Table 8-2 shows the MEC140x Configuration register map. Logical Device numbers are in hexadecimal. All Logical Devices are accessible by both the Host and the EC. Logical Devices between 00h and 3Fh are located on the basechip.

TABLE 8-2: MEC140X CONFIGURATION REGISTER MAP

LPC CR Index	Type Note 8-1	Reset	Configuration Register Name
Configuration Registers for LDN 0h (EMI 0)			
-	-	-	None
Configuration Registers for LDN 1h (Keyboard Controller (8042))			
30h	R/W	00h on **nSYS_RST**	Activate Register
Configuration Registers for LDN 3h (ACPI EC Channel 0)			
-	-	-	None
Configuration Registers for LDN 4h (ACPI EC Channel 1)			
-	-	-	None
Configuration Registers for LDN 5h (ACPI PM 1)			
-	-	-	None
Configuration Registers for LDN 6h (Legacy Port92/GateA20)			
30h	R/W	00h on **nSYS_RST**	PORT92 Enable Register
Configuration Registers for LDN 7h (UART 0)			
30h	R/W	00h on **nSYS_RST**	Activate Register
F0h	R/W	00h on **nSYS_RST**	Configuration Select Register

TABLE 8-2: MEC140X CONFIGURATION REGISTER MAP (CONTINUED)

LPC CR Index	Type Note 8-1	Reset	Configuration Register Name
Configuration Registers for LDN 9h (Mailbox Interface)			
-	-	-	None
Configuration Registers for LDN Ah (ACPI EC Channel 2)			
-	-	-	None
Configuration Registers for LDN Bh (ACPI EC Channel 3)			
-	-	-	None
Configuration Registers for LDN 15h (Port 80 BIOS Debug Port 0)			
-	-	-	None
Configuration Registers for LDN 16h (Port 80 BIOS Debug Port 1)			
-	-	-	None
Configuration Registers for LDN Ch (LPC Interface)			
30h	R/W	00h on **nSYS_RST**	Activate Register
40h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ0 Configuration Register
41h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ1 Configuration Register
42h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ2 Configuration Register
43h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ3 Configuration Register
44h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ4 Configuration Register
45h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ5 Configuration Register
46h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ6 Configuration Register
47h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ7 Configuration Register
48h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ8 Configuration Register
49h	R/W	FFh on **nSIO_RESET**	SIRQ IRQ9 Configuration Register
4Ah	R/W	FFh on **nSIO_RESET**	SIRQ IRQ10 Configuration Register
4Bh	R/W	FFh on **nSIO_RESET**	SIRQ IRQ11 Configuration Register
4Ch	R/W	FFh on **nSIO_RESET**	SIRQ IRQ12 Configuration Register
4Dh	R/W	FFh on **nSIO_RESET**	SIRQ IRQ13 Configuration Register
4Eh	R/W	FFh on **nSIO_RESET**	SIRQ IRQ14 Configuration Register
4Fh	R/W	FFh on **nSIO_RESET**	SIRQ IRQ15 Configuration Register
50h - 5Fh	R/W	00h on **nSIO_RESET**	Reserved
60h - 63h	R/W / R	002E_0C01h on **nSIO_RESET**	BAR for Configuration Port
64h - 67h	R/W / R	0000_000Fh on **nSIO_RESET**	BAR for EMI 0
68h - 6Bh	R/W / R	0060_0104h on **nSIO_RESET**	BAR for 8042/Keyboard Interface
6Ch - 6Fh	R/W / R	0062_0304h on **nSIO_RESET**	BAR for ACPI EC 0
70h - 73h	R/W / R	0066_0407h on **nSIO_RESET**	BAR for ACPI EC 1
74h - 77h	R/W / R	0000_0507h on **nSIO_RESET**	BAR for ACPI PM 1
78h - 7Bh	R/W / R	0092_0600h on **nSIO_RESET**	BAR for Legacy Port92/GateA20

TABLE 8-2: MEC140X CONFIGURATION REGISTER MAP (CONTINUED)

LPC CR Index	Type Note 8-1	Reset	Configuration Register Name
7Ch - 7Fh	R/W / R	0000_0707h on **nSIO_RESET**	BAR for UART 0
80h - 83h	R/W / R	0000_0901h on **nSIO_RESET**	BAR for Mailbox Interface
84h - 87h	R/W / R	0000_0A07h on **nSIO_RESET**	BAR for ACPI EC 2
88h - 8Bh	R/W / R	0000_0B07h on **nSIO_RESET**	BAR for ACPI EC 3
8Ch - 8Fh	R/W / R	0000_1500h on **nSIO_RESET**	BAR for Port 80 BIOS Debug Port 0
90h - 93h	R/W / R	0000_1600h on **nSIO_RESET**	BAR for Port 80 BIOS Debug Port 1
C0h - C5h	R/W / R	0000_0000_000Fh on **nSIO_RESET**	Memory BAR for EMI 0
C6h - CBh	R/W / R	0000_0062_0304h on **nSIO_RESET**	Memory BAR for ACPI EC 0
CCh - D1h	R/W / R	0000_0066_0407h on **nSIO_RESET**	Memory BAR for ACPI EC 1
D2h - D7h	R/W / R	0000_0000_0901h on **nSIO_RESET**	Memory BAR for Mailbox Interface
D8h - DDh	R/W / R	0000_0000_0A07h on **nSIO_RESET**	Memory BAR for ACPI EC 2
DEh - E3h	R/W / R	0000_0000_0B07h on **nSIO_RESET**	Memory BAR for ACPI EC 3

Note 8-1 R/W / R means that some parts of a register are read/write and some parts are read-only.

9.0 GLOBAL CONTROL/CONFIGURATION REGISTERS [00H - 2FH]

The chip-level (global) registers reside in Logical Device 3Fh. The global registers are accessed in the configuration address range [00h - 2Fh] in all Logical Devices. There is no Activate associated with Logical Device 3Fh: the global configuration registers are always accessible.

As with all configuration registers, the Index Port is used to select a global configuration register in the chip. The Data Port is then used to access the selected register.

The Host can access all the global configuration registers at the offsets listed in Table 9-1, "Chip-Level (Global) Control/ Configuration Registers" through the Index Port and the Data Port.

TABLE 9-1: CHIP-LEVEL (GLOBAL) CONTROL/CONFIGURATION REGISTERS

Register	Offset	Description
CHIP (GLOBAL) CONTROL REGISTERS		
Reserved	00h - 06h	Reserved - Writes are ignored, reads return 0.
Logical Device Number	07h	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. **Note:** The Activate command operates only on the selected logical device.
Reserved	08h - 1Bh	Reserved - Writes are ignored, reads return 0.
Device Revision	1Ch	A read-only register which provides device revision information. Bits[7:0] = current revision when read
Device Sub ID	1Dh	Device Sub ID[7:0] Read-Only register which provides the device sub-identification. The value of this register is product dependent. See Table 9-2, "DEVICE IDENTIFICATION".
Device ID[7:0]	1Eh	Device ID[7:0] Read-Only register which provides Device ID LSB. The value of this register is product dependent. See Table 9-2, "DEVICE IDENTIFICATION".
Device ID[15:8]	1Fh	Device ID[15:8] Read-Only register which provides Device ID MSB. The value of this register is product dependent. See Table 9-2, "DEVICE IDENTIFICATION".
Legacy Identification	20h	Legacy Identification A read-only register which provides device identification to legacy and test software. This field is hard-coded to FEh, indicating this is a MIPs product with 16-bit Device ID offsets 1Eh & 1Fh.
Reserved	21h - 23h	Reserved.
Device Mode	24h	Bit [1:0] Reserved – writes ignored, reads return “0”. Bit[2] SerIRQ Mode = 0: Serial IRQ Disabled. = 1: Serial IRQ Enabled (Default). (Default). Bit [7:3] Reserved – writes ignored, reads return “0”.
Test	25h - 2Fh	Test These register locations are reserved for Microchip use. Modifying these locations may cause unwanted results.

9.1 Device Identification

TABLE 9-2: DEVICE IDENTIFICATION

Product	Device ID[15:0]	Device SUB ID[7:0]
MEC1404	0002h	10h
MEC1406	0004h	10h
MEC1408	0006h	10h

10.0 SUPER I/O INITIALIZATION IN EARLY POST

10.1 LPC Interface - Logical Device C Chart and Description

The following two figures show the process for MEC140x configuration registers initialization.

FIGURE 10-1: MEC140X CONFIGURATION REGISTERS INITIALIZATION - PART I

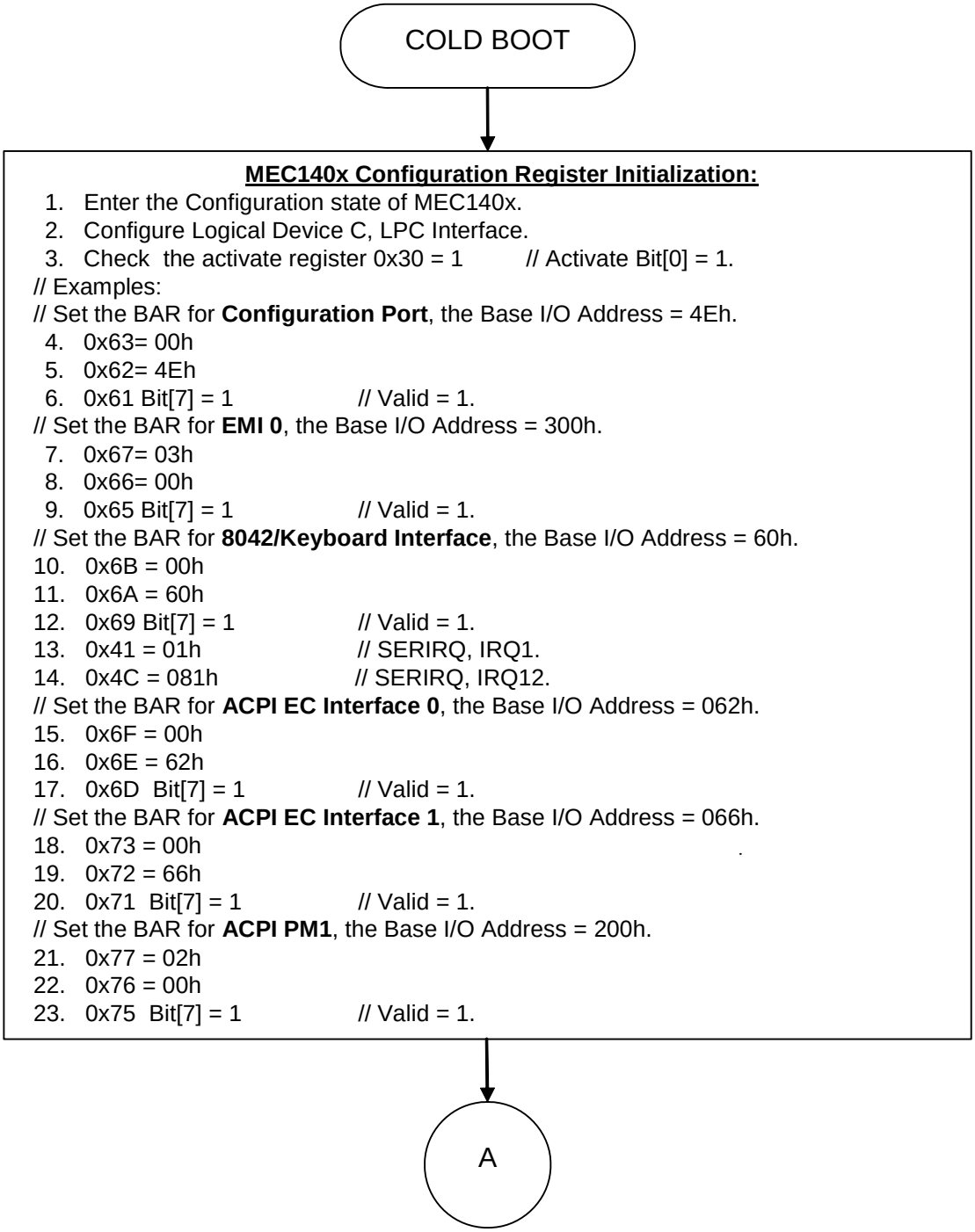
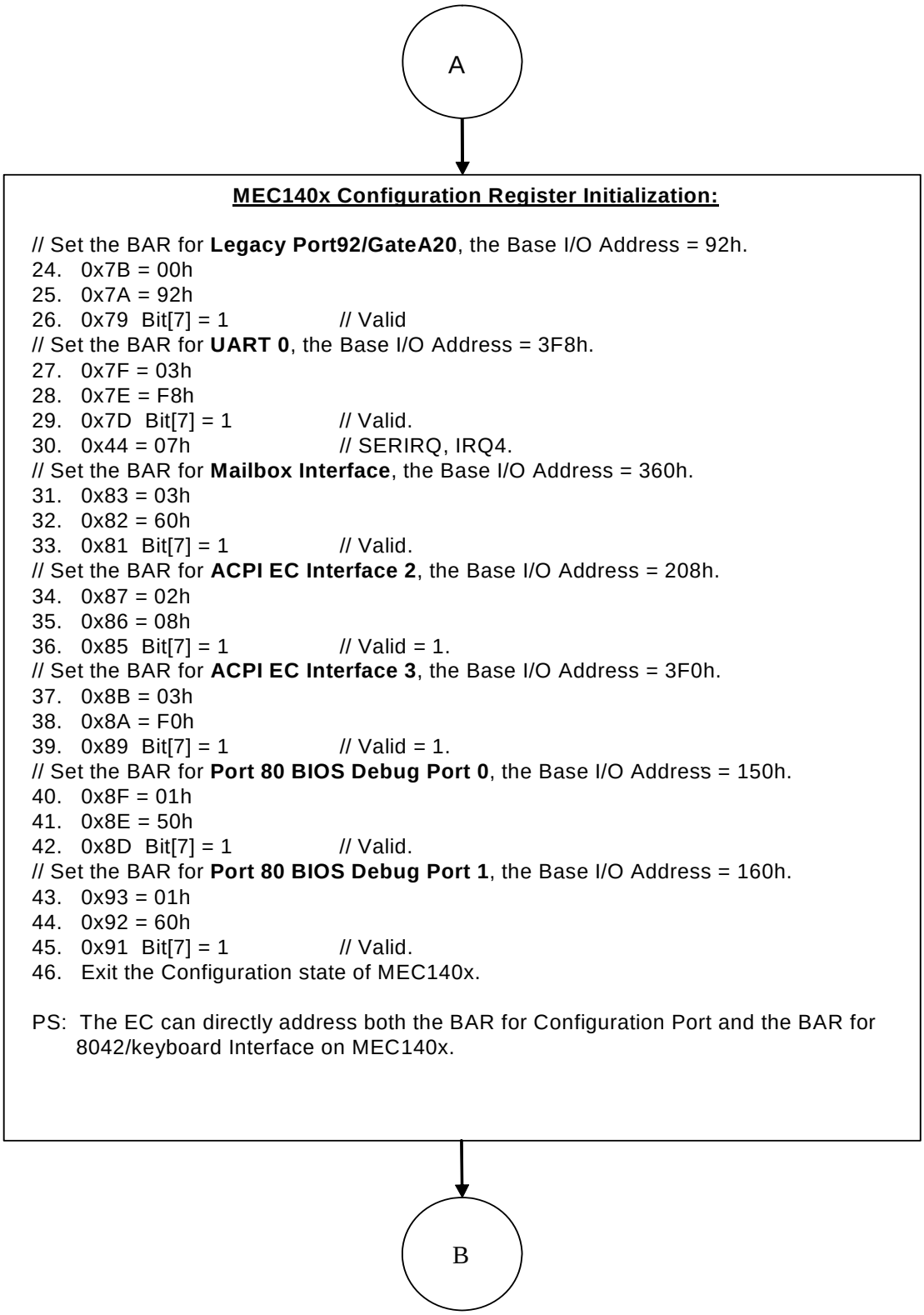


FIGURE 10-2: MEC140X CONFIGURATION REGISTERS INITIALIZATION - PART II



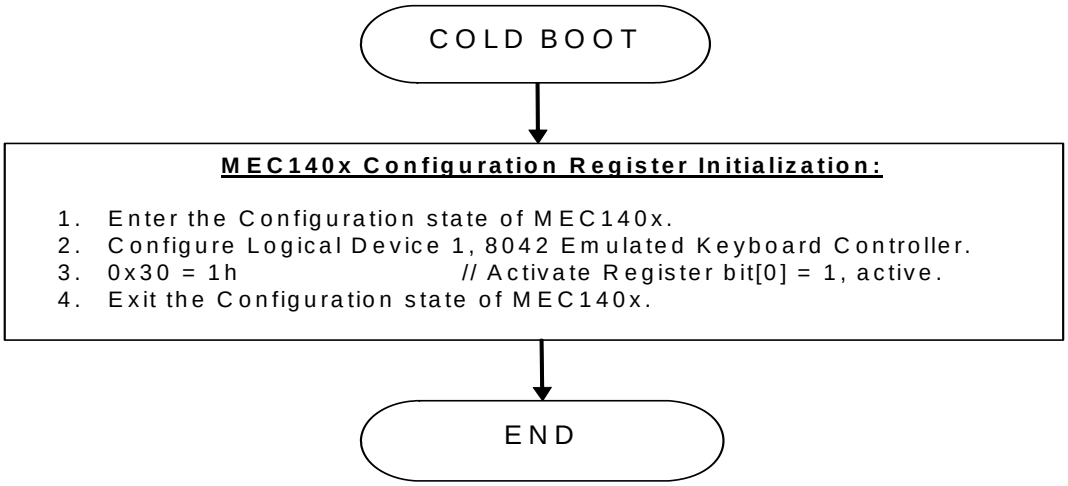
Note 10-1 Both the Activate bit in Activate Register offset 30h and the Valid bit in BAR control different functionality, and do not affect each other.

- Activate bit = 1, block is powered and functional. (In fact, not really powered, should be gated.)
- Valid bit = 1, the MEC140x chip I/O address claiming is enabled.

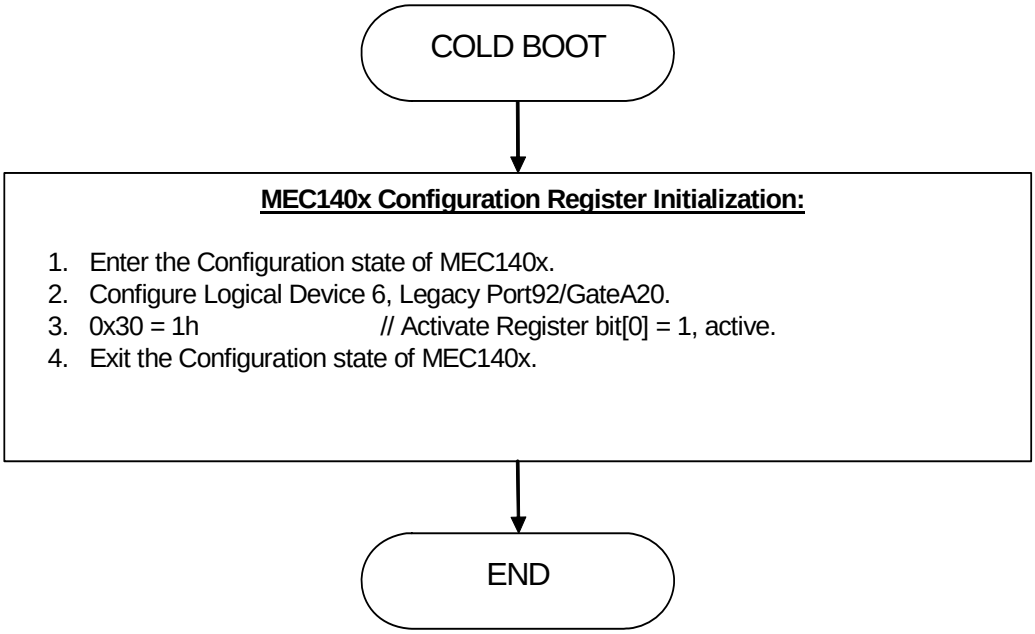
BIOS must set both bits to activate this module and make it functional. The following is the recommended sequence:

1. Configure correct I/O address in BAR if needed.
2. Set Valid bit in BAR.
3. Set Activate bit in the Activate register if needed.

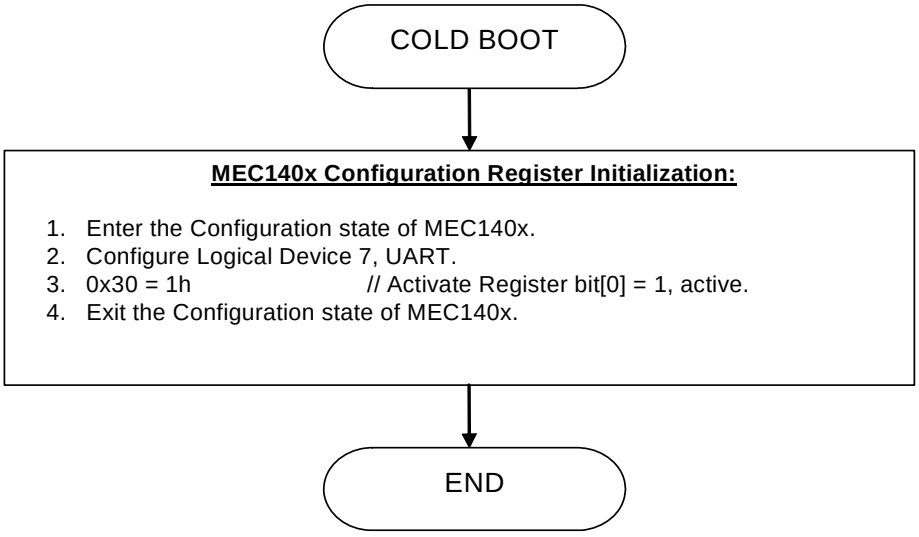
10.2 8042 Emulated Keyboard Controller - Logical Device 1 Chart and Description



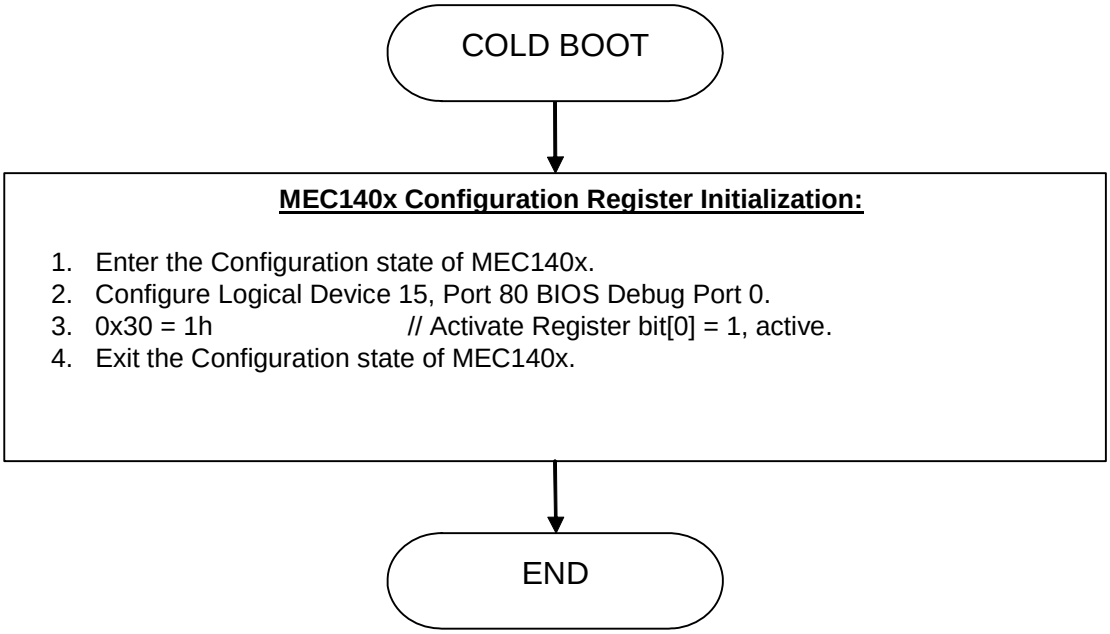
10.3 Legacy Port92/GateA20 - Logical Device 6 Chart and Description



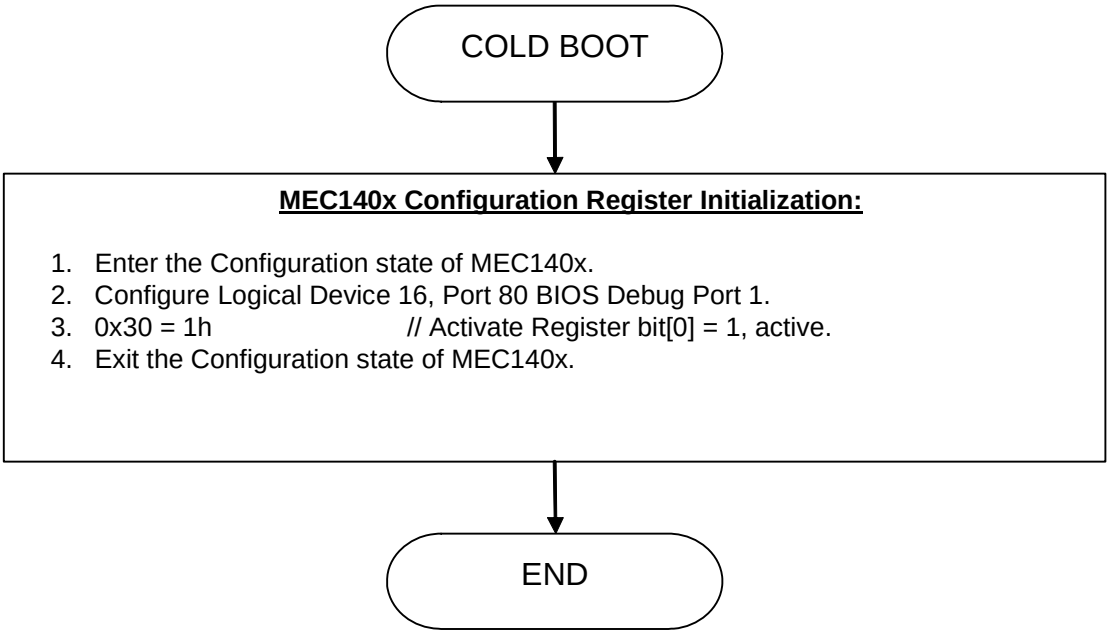
10.4 UART - Logical Device 7 Chart and Description



10.5 Port80 BIOS Debug Port 0 - Logical Device 15 Chart and Description



10.6 Port 80 BIOS Debug Port 1 - Logical Device 16 Chart and Description



11.0 INTEL LPC INTERFACE BRIDGE REGISTER INITIALIZATION

This section provides the initialization of the Intel LPC Interface Bridge registers (D31:F0) to support MEC140x SIO devices in cold booting.

1. LPC_I/O_DEC-I/O Decode Ranges Register 80h - 81h = 0010h

- FDD Decode Range Bit[12] = 0 // Enables the decoding of the I/O locations 3F0h - 3F5h, 3F7h (Primary) to the LPC interface.
- LPT Decode Range Bits[9:8] = 00 // Enables the decoding of the I/O locations 378h - 37Fh and 778h - 77Fh for the LPT Port.
- COMB Decode Range Bits[6:4] = 001 // Enables the decoding of the I/O locations 2F8h - 2FFh (COM2) for the COMB Port.
- COMA Decode Range Bits[2:0] = 000 // Enables the decoding of the I/O locations 3F8h - 3FFh (COM1) for the COMA Port.

2. LPC_I/O_DEC-I/O Decode Ranges Register 82h - 83h = 3F0Fh

- CNF2_LPC_EN Bit[13] = 1 // Enables the decoding of the I/O locations 4Eh and 4Fh to the LPC interface.
- CNF1_LPC_EN Bit[12] = 1 // Enables the decoding of the I/O locations 2Eh and 2Fh to the LPC interface.
- MC_LPC_EN Bit[11] = 1 // Enables the decoding of the I/O locations 62h and 66h to the LPC interface.
- KBC_LPC_EN Bit[10] = 1 // Enables the decoding of the I/O locations 60h and 64h to the LPC interface.
- GAMEH_LPC_EN Bit[9] = 1 // Enables the decoding of the I/O locations 208h and 20Fh to the LPC interface.
- GAMEL_LPC_EN Bit[9] = 1 // Enables the decoding of the I/O locations 200h and 207h to the LPC interface.
- FDD_LPC_EN Bit[3] = 1 // Enables the decoding of the FDD range to the LPC interface.
- LPT_LPC_EN Bit[2] = 1 // Enables the decoding of the LPT range to the LPC interface.
- COMB_LPC_EN Bit[1] = 1 // Enables the decoding of the COMB range to the LPC interface.
- COMA_LPC_EN Bit[0] = 1 // Enables the decoding of the COMA range to the LPC interface.

3. GEN1_DEC - LPC I/F Generic Decode Range 1 Register 84h - 87h = 007C0301h

- Generic I/O Decode Range Address [7:2] Mask Bits[23:18] = 7Ch
- Generic I/O Decode Range 1 Base Address (GEN1_BASE) Bits[15:2] = 030h
- Generic Decode Range 1 Enable (GEN1_EN) Bit[0] = 1 // Enable the GEN1 I/O range to be forwarded to the LPC I/F.

4. GEN2_DEC - LPC I/F Generic Decode Range 2 Register 88h - 8Bh = 000C0681h

- Generic I/O Decode Range Address [7:2] Mask Bits[23:18] = 0Ch
- Generic I/O Decode Range 2 Base Address (GEN2_BASE) Bits[15:2] = 068h
- Generic Decode Range 2 Enable (GEN2_EN) Bit[0] = 1 // Access to the GEN2 I/O range is forwarded to the LPC I/F.

5. GEN3_DEC - LPC I/F Generic Decode Range 3 Register 8C - 8Fh = 007C0151h

- Generic I/O Decode Range Address [7:2] Mask Bits[23:18] = 7Ch
- Generic I/O Decode Range 3 Base Address (GEN3_BASE) Bits[15:2] = 015h
- Generic Decode Range 3 Enable (GEN3_EN) Bit[0] = 1// Access to the GEN3 I/O range is forwarded to the LPC I/F.

6. GEN4_DEC - LPC I/F Generic Decode Range 4 Register 90h - 93h = 000C0361h

- Generic I/O Decode Range Address [7:2] Mask Bits[23:18] = 0Ch
- Generic I/O Decode Range 4 Base Address (GEN4_BASE) Bits[15:2] = 036h

Generic Decode Range 4 Enable (GEN4_EN) Bit[0] = 1 // Access to the GEN4 I/O range is forwarded to the LPC I/F.

APPENDIX A: REVISION HISTORY

TABLE A-1: APPLICATION NOTE REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001865A (12-03-14)	Document Release	

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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