
USB253x/USB46x4/USB3x13 Embedded Testing Modes

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INTRODUCTION

The Microchip USB253x/USB46x4/USB3x13 product lines are a family of feature-rich, low-power USB 2.0 hubs optimized for use in portable devices or embedded systems where high performance and minimal BOM costs are critical design requirements. The SMBus slave interface is a 2-pin protocol which can be used to customize the functionality of this family of USB hubs. The System on Chip (SoC) can use this interface to control the digital and USB lines for testing, configure custom functionality, and load custom firmware to unlock the various features of the embedded processor. Among these features is a USB compliance test mode designed to facilitate USB compliance testing when a USB253x/USB46x4/USB3x13 hub is applied within an embedded system.

This document includes the following topics:

- [Embedded Host Compliance Testing Modes Overview](#)
- [Test Mode Setup](#)
- [Test Mode Descriptions](#)

Audience

This document is written for developers who are familiar with USB and SMBus protocols as well as USB 2.0 compliance tests. The goal of this application note is to describe the USB253x/USB46x4/USB3x13 embedded test modes to help facilitate compliance testing within embedded designs.

EMBEDDED HOST COMPLIANCE TESTING MODES OVERVIEW

The “Embedded Host Compliance Testing Modes” feature is designed to allow the hub to be tested for USB compliance when the tester is unable to easily control testing modes through the upstream USB port. These test modes are enabled and controlled via a series of SMBus writes to the hub that are performed during configuration. After the test modes have been enabled during configuration, the hub can generate one of the following test patterns through any of its downstream ports:

- **TEST_SE0:** The hub’s downstream port drives SE0
- **TEST_J:** The hub’s downstream port enters high-speed J state
- **TEST_K:** The hub’s downstream port enters high-speed K state
- **TEST_PACKET:** The hub’s downstream port sends compliance test packets

TEST MODE SETUP

The following configuration steps must be performed to activate the “Embedded Host Compliance Testing Modes”. Refer to Application Note 26.18 entitled “SMBus Slave Interface for the USB253x/USB3x13/USB46x4” for in-depth information regarding the SMBus protocol as well as additional features that can be controlled via SMBus.

1. Pull-up the SMBus SCL and SDA lines to 3.3V and reset the hub to hold the device in the SoC configuration stage.
2. Using SMBus slave address 2D, write to the following test configuration register to select the desired test mode.

TABLE 1: CNTLP REGISTER (0x318C)

BIT	NAME	DESCRIPTION
7:6	Reserved	Always '0'
3:1	EMBEDTEST[2:0]	(000) - Default Operation - no test mode asserted (001) - TEST_SE0 - hub enters high-speed receive and drives SE0 on the hub's downstream port (010) - TEST_J - hub's downstream port enters high-speed J state (011) - TEST_K - hub's downstream port enters high-speed K state (100) - TEST_PACKET - send test packets on downstream port All others Reserved
0	Reserved	Always '0'

- Using SMBus slave address 2D, write to the following port configuration register to select the desired downstream USB test port.

TABLE 2: COM_TEST_PSEL REGISTER (0x600F)

BIT	NAME	DESCRIPTION
7	Reserved	Always '0'
6:4	SIG_GROUP[2:0]	Not used for this application. Default (000)
3:0	PORT_SEL[3:0]	(0000) - Upstream Port (0001) - Downstream Port 1 (0010) - Downstream Port 2 (0011) - Downstream Port 3 (0101) - Downstream Port 4 (0101) - Not Used (0110) - Not Used (0111) - Not Used (1000) - Common Block

- The selected test pattern will now be generated through the selected downstream port. The USB attachment command is not required. The device will exit test mode when reset.

TEST MODE DESCRIPTIONS

This section describes each test mode behavior. Screen captures of the four test modes are included to show what to expect when operating in each test mode. These oscilloscope screen images were captured from a USB4624 hub with probes connected to the D+ and D- pins on the selected downstream port.

TEST_SE0

This mode drives a single-ended zero (SE0, both D- and D+ pins low) on the selected port.

To enable TEST_SE0 on Downstream Port 1:

- Write 0x02 to configuration register 0x318C
- Write 0x01 to configuration register 0x600F

TEST_J

The TEST_J pattern asserts and holds the D+ pin high until the part is reset or the CNTLP register is modified. The magnitude of the D+ signal can be measured with respect to ground to verify compliance.

FIGURE 1: TEST_J WAVEFORM



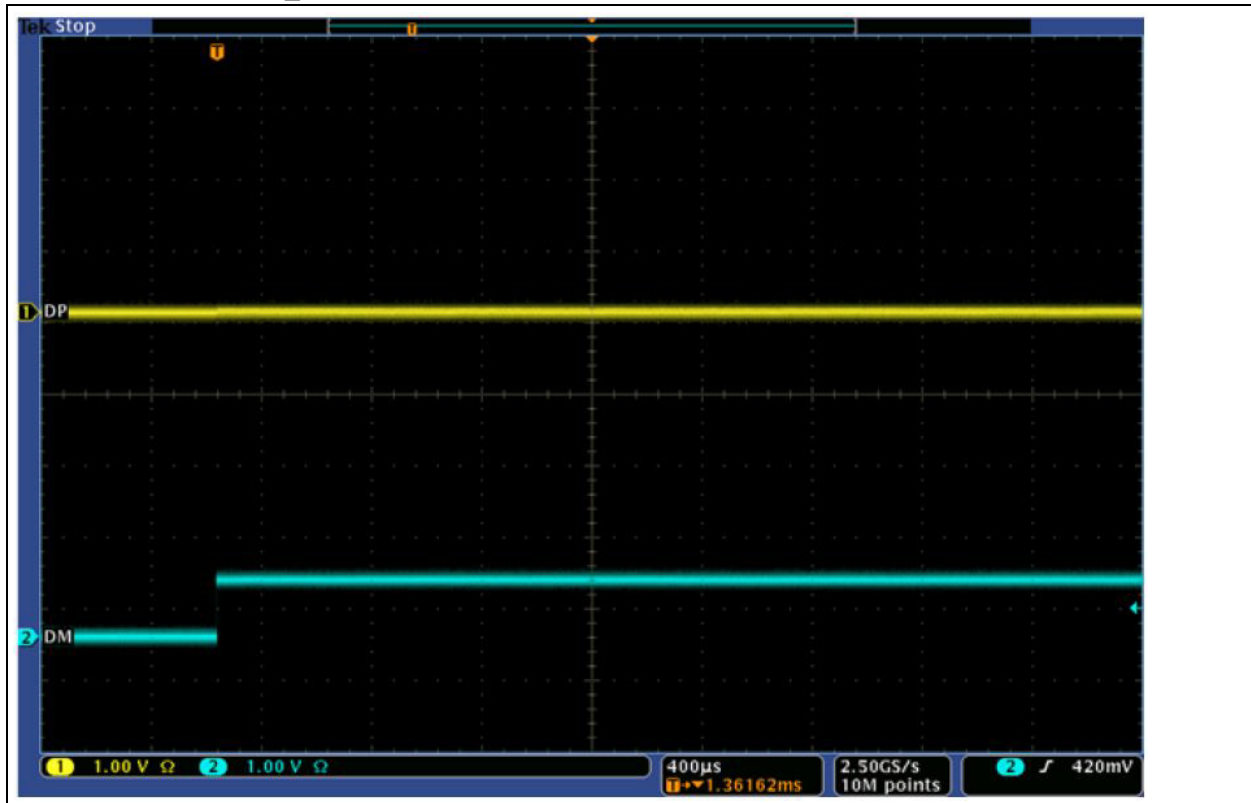
To enable TEST_J on Downstream Port 1:

- Write 0x04 to configuration register 0x318C
- Write 0x01 to configuration register 0x600F

TEST_K

The TEST_K pattern asserts and holds the D- pin high until the part is reset or the CNTLP register is modified. The magnitude of the D- signal can be measured with respect to ground to verify compliance.

FIGURE 2: TEST_K WAVEFORM



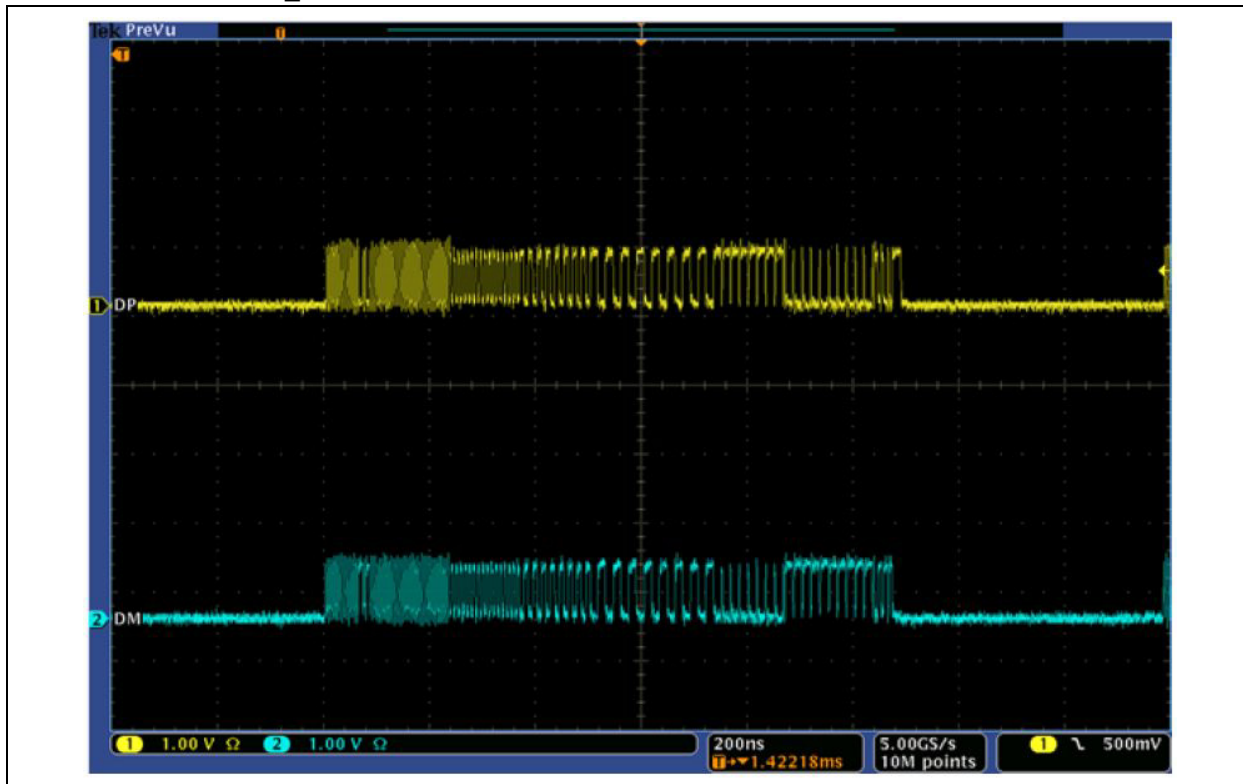
To enable TEST_K on Downstream Port 1:

- Write 0x06 to configuration register 0x318C
- Write 0x01 to configuration register 0x600F

TEST_PACKET

The TEST_PACKET pattern is used to verify that the Signal Eye, EOP Width, Rise and Fall time, and Signaling Rate all pass USB compliance. USB compliance tools are required to process this waveform and generate the Signal Eye plot. Figure 3 shows the TEST_PACKET waveform.

FIGURE 3: TEST_PACKET WAVEFORM



To enable TEST_PACKET on Downstream Port 1:

- Write 0x08 to configuration register 0x318C
- Write 0x01 to configuration register 0x600F

NOTES:

APPENDIX A: REFERENCES

The following documents should be referenced when using this application note. Contact your Microchip representative for availability.

- USB2532 Datasheet
- USB2533 Datasheet
- USB2534 Datasheet
- USB3613 Datasheet
- USB3813 Datasheet
- USB4604 Datasheet
- USB4624 Datasheet
- AN26.18 “Slave Interface for the USB253x/USB3x13/USB46x4”

APPENDIX B: REVISION HISTORY

Revision A (November 2013)

- Initial release of this document.

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