
ADC Channel Switching Effect on I/O Pins

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INTRODUCTION

The analog functionality on microcontrollers can create complex interactions with the digital portion of the circuitry and the running firmware. The application can have undesired interactions unless the analog features are understood. This technical brief will describe the most common I/O issues that arise when switching between ADC channels.

BACKGROUND

Digital logic is utilized in controlling the analog channel multiplexer (MUX). As an artifact of using digital logic to switch between analog (ADC) channels, signals from different device pins can momentarily be connected. Two unrelated I/O pins can become connected when the ADC input channels are switched. The I/O can connect for the amount of time it takes the signal to propagate through the MUX to trigger the ADC channel to change. This connection can last up to 40 ns, which is longer than the minimum rise and fall times of the I/O pin logic, causing a glitch on the connected pins. This is enough time to have an effect on the pins since the rise and fall times of the pins are 15 to 30 ns. The effects of the glitch can last longer than 40 ns due to the time it takes for the pins to change their state back to their prior level.

As an example, if switching between ADC inputs AN2 and AN5, RB4 and RC0 could become connected for the duration of the switching time. Having RB4 set as an input that is driven half way between logic-high and logic-low can cause the glitch to be seen on RC0 if it is set as an output. When the two connected pins are at the same logic level, the glitch is minimized to less than 10 mV. In the extreme case where both pins are at differing logic levels, the glitch can be above 160 mV.

Another source of glitches can arise from switching the channels of the ADC itself. These glitches can be seen externally if the ADC input channel is also an input to an active comparator or op amp on the device. Three different sources of glitches can occur. Switching ADC channels changes the voltage across the ADC sample and hold capacitor (cap), which can cause glitches due to the potential differences across the cap. Depending

on the external voltage level applied across the cap, the glitch can be positive or negative in nature. A second glitch can occur while the first glitch is recovering. This second glitch is due to the cap being disconnected from the pin electronics. The third glitch happens when the conversion is complete and the cap is re-connected to the pin electronics.

WORKAROUND

Digital Inputs

When using the I/O pins as digital input, there are a few choices to avoid the ADC channel switching issues. If the input pin is being polled, an option is not to switch ADC channels while in the polling loop. If polling is not used, then the input pin should not be checked for a state change right after issuing an ADC channel switch. Insert a NOP (no operation) instruction after the channel change, and then check the input for state change. The better option, if only dealing with a state change, is software debouncing the input. Check the input several times, counting up the number of times a particular state is registered. Once enough counts of the state change are recorded, then the state variable can be changed. This way, any ADC channel switching glitches get filtered out of the possible state change.

Digital Outputs

Using the digital pin as an output can cause spurious glitches to external circuitry during the ADC channel switching. The output pin, when driven high or low, can see a glitch corresponding to the opposite direction of the driven state. As an example, if the output is driven high, then a negative going glitch of up to 200 mV below the high state can appear on the pin. This glitch can last anywhere from 15 to 40 ns depending on the settling time of the switching logic.

The main ways to reduce or eliminate the issue are to reduce the energy in the glitch, make external circuits immune to the glitch, or to filter out the glitch entirely. First, try adding a resistor to the output pin to limit the current in the glitch so that it will not appreciably affect external circuits. External circuits that have Schmitt Trigger inputs would be immune to the glitch due to their inherent hysteresis. Another option is to filter out the glitch.

A low-pass RC filter on the output pin will reduce or even eliminate any glitches from reaching the external circuitry. Several factors need to be accounted for in choosing the R and the C component values of the filter. The RC time constant should be longer than the time period of the glitch ($t > 40$ ns) to filter out the glitch.

EQUATION 1: RC TIME CONSTANT

$$t = R \times C$$

It is recommended to be careful with the frequency response of the RC low-pass filter, so that it does not interfere with the external circuit. At a minimum, the cut-off frequency should be a decade higher frequency than the highest frequency signal that the application will output on that pin.

EQUATION 2: CUT-OFF FREQUENCY

$$f_c = \frac{1}{2\pi RC}$$

As an approximation, using the glitch rise and fall times of 15 to 40 ns (t_r) would give a frequency of interest in the range of 8 to 24 MHz (BW). This is a rough idea of the highest frequency component in the glitch based on the equation relating bandwidth to rise time.

EQUATION 3: BANDWIDTH TO RISE TIME RELATION

$$BW = \frac{0.35}{t_r}$$

Note: t_r = the 10-90% rise time of a square wave
BW = the bandwidth of the signal

CONCLUSION

Care should be taken when switching between ADC channels as the switching logic can inadvertently connect I/O pins. Using the recommendations above, most of the effects caused by channel switching can be mitigated. Modern MCUs with digital and analog components in close proximity can cause many previously unseen issues, but by following a few simple guidelines a robust application can be realized.

Analog Inputs

The first and second analog glitches can be reduced or eliminated by precharging the sample and the hold capacitor using the DAC. Set the DAC to a voltage level close to the expected voltage the ADC will sample to reduce the glitch. Charging the sample and the hold capacitor needs to be done before switching external ADC channels. If a close approximation of the voltage is known, then the DAC can be used to precharge the cap to a similar potential.

The third analog glitch is removed by switching the ADC to a different channel after the conversion is started, but before the conversion is complete. Start by selecting the conversion channel. Then start the conversion. Next, switch the ADC to the next channel to convert. Finally, the conversion completes and the process can be started over again.

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