DisplayPort Tx v2.1 User Guide

Introduction (Ask a Question)

DisplayPort Tx IP is designed for transmission of video for displays. It is targeted for the PolarFire® FPGA application implemented based on the Video Electronics Standards Association (VESA) DisplayPort Standard 1.4 protocol. Supports standard rates of 1.62, 2.7, 5.4, 8.1 Gbps for displays.

Summary (Ask a Question)

The following table provides a summary of the DisplayPort Tx IP characteristics.

Table 1. DisplayPort Tx IP Characteristics

Core Version	This document applies to DisplayPort Tx v2.1.
Supported Device Families	• PolarFire® SoC • PolarFire • RTG4™ • IGLOO® 2 • SmartFusion® 2
Supported Tool Flow	Requires Libero® SoC v11.8 or later releases.
Licensing	The core is license-locked for clear text RTL. It supports the generation of Encrypted RTL for the Verilog version of core with no license.

Features (Ask a Question)

DisplayPort Tx has the following key features:

- Support 2 or 4 lanes
- Support 6, 8, 10, 12, and 16 bits per component
- Support up to 8.1 Gbps per lane
- Support DisplayPort 1.4 protocol
- Only support a single video stream or SST mode, and the MST mode is not supported
- Audio transmission is not supported

Implementation of IP Core in Libero® Design Suite (Ask a Question)

IP core must be installed to the IP Catalog of the Libero SoC software. This is done automatically through the IP Catalog update function in the Libero SoC software, or the IP core is manually downloaded from the catalog. Once the IP core is installed in the Libero SoC software IP Catalog, the core is configured, generated, and instantiated within the SmartDesign tool for inclusion in the Libero project list.

Device Utilization and Performance (Ask a Question)

The following table lists the device utilization used for DisplayPort Tx.

Table 2. DisplayPort Tx Utilization

Device Details		Resources		Performance (MHz)	RAMs		Math Blocks	Chip Globals
Family	Device	LUTs	DFF		LSRAM	µSRAM		
PolarFire® SoC	MPFS250T	14283	10181	200	3	53	0	0
PolarFire	MPF300T	14283	10181	200	3	53	0	0

Important:

1. The data in this table is captured using typical synthesis and layout settings. CDR reference clock source was set to **Dedicated** with other configurator values unchanged.
2. Clock is constrained to 200 MHz while running the timing analysis to achieve the performance numbers.

Table of Contents

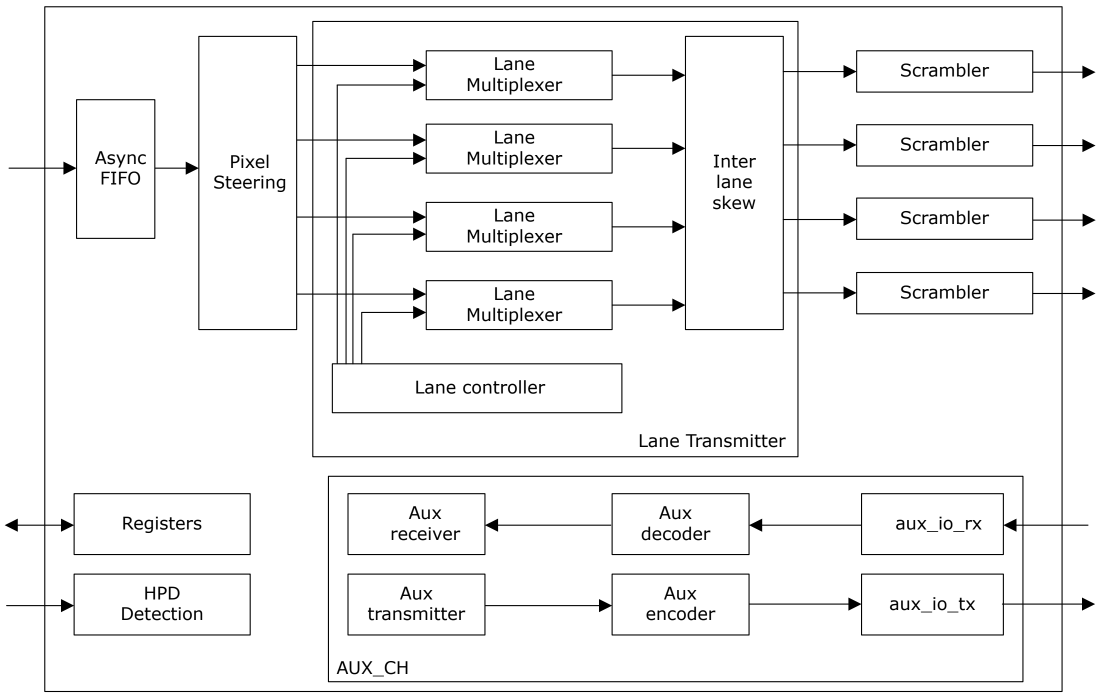
1. Functional Description (Ask a Question)

This section describes the implementation details of the DisplayPort Tx.

1.1 DisplayPort Tx IP Architecture (Ask a Question)

The following figure shows the DisplayPort Tx IP implementation.

Figure 1-1. DisplayPort Tx IP Implementation



As shown in the preceding figure, DisplayPort Tx IP includes the Pixel Steering module, Lane transmitter module, Scrambler module, and AUX_CH module.

Pixel Steering assigns input pixels to DisplayPort lanes. The lane transmitter module generates a video data stream with blank data or training data. Scrambler scrambles the lane transmission data. AUX_CH module transmits the AUX Request command to the DisplayPort Sink device or receives AUX Reply from the DisplayPort Sink device.

1.2 Video Stream Transmission (Ask a Question)

DisplayPort Tx IP supports RGB 4:4:4, and only supports a single video stream. After training is done and the video stream is ready, DisplayPort Tx IP start to transmit video stream. DisplayPort Source application software should configure the video stream attribute MSA and enable DisplayPort Tx IP video transmission. The VSC packet is not supported. DisplayPort Tx are using MISC0 and MISC1 in MSA for Pixel Encoding/Colorimetry Format Indication.

1.3 AUX Channel (Ask a Question)

DisplayPort Source device communicate DisplayPort Sink through an AUX Channel. Source device sending request transaction to the Sink device and the Sink device sending Reply transaction to Source Device. DisplayPort Tx implements the AUX transaction transmitter and receiver. For AUX transaction transmitter, DisplayPort Source application software provides all AUX transaction content bytes, DisplayPort Tx IP generate the transaction bitstream. For the AUX transaction receiver, DisplayPort Tx IP receive the transaction and extract all bytes to DisplayPort application software. The Link Policy Maker and Stream Policy Maker should be implemented in the DisplayPort application software.

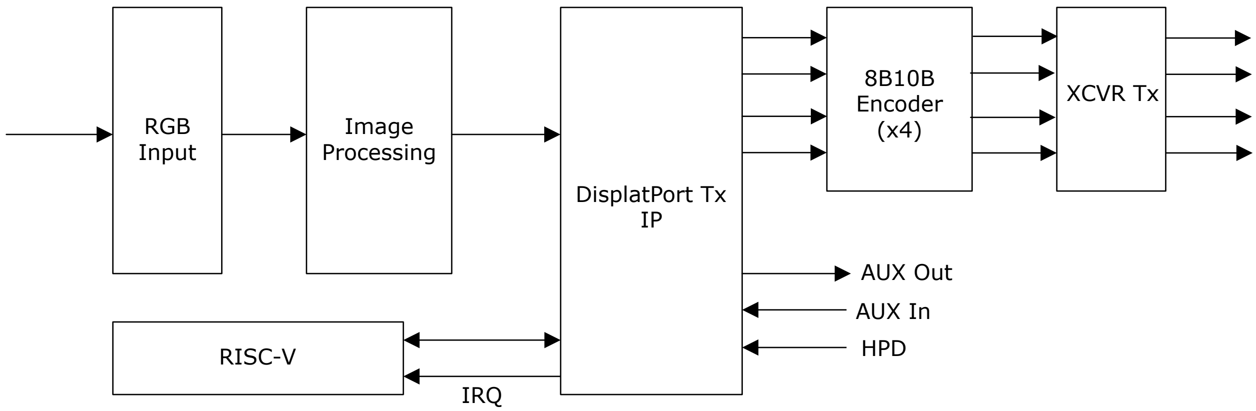
1.4 HPD (Ask a Question)

DisplayPort Tx IP detects Hot Plug Detect (HPD) assertion, de-assertion, and HPD interrupt event. It reports the HPD event through an interrupt. After HPD assertion, which means a DisplayPort monitor is connected, DisplayPort Source application software should start the training procedure.

2. DisplayPort Tx IP Application (Ask a Question)

The following figure shows the typical DisplayPort Tx IP application.

Figure 2-1. Typical application for DisplayPort Tx IP



As shown in the preceding figure, the RGB input module interface gets a video stream signal. The Image Processing module processes the video stream according to system requirements. It outputs the video stream to DisplayPort Tx IP. DisplayPort Tx IP outputs four lanes data to the 8B10B encoder. After 10B encoding, lanes' data are transmitted through Transceiver lanes.

Before video stream transmission, the DisplayPort Source application software which is running on RISC-V, controls DisplayPort Tx IP to finish training work with the attached DisplayPort Sink device. To do training and Link Policy Maker, all transactions are transmitted on the AUX Channel.

3. DisplayPort Tx Parameters and Interface Signals (Ask a Question)

This section discusses the parameters in the DisplayPort Tx GUI configurator and I/O signals.

3.1 Configuration Settings (Ask a Question)

The following table lists the description of the configuration parameters used in the hardware implementation of DisplayPort Tx. These are generic parameters and varied as per the requirement of the application.

Table 3-1. Configuration Parameter

Name	Default	Description
Number of bits per component	8	Supports 6, 8, 10, 12, and 16 bits per component
Number of Pixels	1	It defines the parallel pixel number on input video stream port
Number of Lanes	4	Supports two and four lanes

3.2 Inputs and Outputs Signals (Ask a Question)

The following table lists the input and output ports of DisplayPort Tx IP.

Table 3-2. Inputs and Outputs of DisplayPort Tx

Interface	Width	Direction	Description
vclk_i	1	Input	Video clock
vrst_n_i	1	Input	Low-active reset signal synchronized with vclk_i
dpclk_i	1	Input	DisplayPort IP working clock. It is DisplayPortLaneRate/40. For example, DisplayPort lane rate is 2.7 Gbps, dpclk_i is 2.7 Gbps/40 = 67.5 MHz.
dprst_n_i	1	Input	Low-active reset signal synchronized with dpclk_i
aux_clk_i	1	Input	AUX Channel clock. It is 100 MHz
aux_rst_n_i	1	Input	Low-active reset signal synchronized with aux_clk_i
pclk_i	1	Input	APB interface clock
prst_n_i	1	Input	Low-active reset signal synchronized with pclk_i
paddr_i	16	Input	APB address
pwrite_i	1	Input	APB write signal
psel_i	1	Input	APB select signal
penable_i	1	Input	APB enable signal
pwdata_i	32	Input	APB writing data
prdata_o	32	Output	APB reading data
pready_o	1	Output	APB reading data ready signal
async_mvid_i	24	Input	Mvid for asynchronous video clock mode, this signal should be synchronized with dpclk_i. This signal would be ignored for synchronous video clock mode.
int_o	1	Output	Interrupt signal to CPU
vsync_i	1	Input	VSYNC for input video stream. It should be synchronous with vclk_i.
hsync_i	1	Input	HSYNC for input video stream. It should be synchronous with vclk_i.
pixel_val_i	1	Input	Indicates the validation of pixels on pixel_data_i port, synchronous with vclk_i
pixel_data_i	3*Number of bits per component*Number of Pixels	Input	Input video stream pixel data. It could be 1 or 4 parallel pixels. It should be synchronous with vclk_i. For four parallel pixels, bit[95:72] for 1st pixel, bit[71:48] for 2nd pixel, bit[47:24] for 3rd pixel, and bit[23:0] for 4th pixel. 1st pixel is the latest pixel. For one parallel pixel, bit[23:16] is R, bit[15:8] is G, bit[7:0] is B
hpd_i	1	Input	HPD input signal

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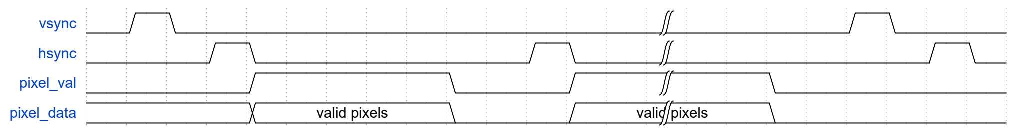
Interface	Width	Direction	Description
aux_tx_en_o	1	Output	AUX Tx data enable signal
aux_tx_io_o	1	Output	AUX Tx data
aux_rx_io_i	1	Input	AUX Rx data
dp_lane_k_o	16	Output	DisplayPort output lanes' data K indication. It is synchronous with dpclk_i. Bit[15:12] for Lane0, bit[11:8] for Lane1, bit[7:4] for Lane2, and bit[3:0] for Lane3.
dp_lane_data_o	128	Output	DisplayPort output lanes' data. It is synchronous with dpclk_i. Bit[127:96] for Lane0, bit[95:64] for Lane1, bit[63:32] for Lane2, and bit[31:0] for Lane3.

4. Timing Diagrams (Ask a Question)

The following figure shows the timing diagram of DisplayPort Tx. hsync_i signal is asserted for several cycles before each line. If there are n lines in a video frame, there are n hsync_i asserted. DisplayPort Tx IP generates the each lane k characters in dp_lane_k_o output port, bit[15:12] for lane 0, bit[11:8] for lane1, bit[7:4] for lane 2, bit[3:0] for lane 3 and it also generates the lane data in dp_lane_data_o output port, bit[127:96] for lane0, bit[95:64] for lane1, bit[63:32] for lane2 , bit[31:0] for lane3

Figure 4-1. DisplayPort Tx Timing Diagram



5. DisplayPort Tx IP Configuration (Ask a Question)

This section discusses the configuration of the DisplayPort Tx IP.

5.1 HPD Detection (Ask a Question)

DisplayPort Tx IP detects the input HPD signal to check the status of the attached DisplayPort Sink device. The HPD event is of the following three types:

- HPD assertion, it means DisplayPort Sink device is connected.
- HPD de-assertion, it means DisplayPort Sink device is disconnected.
- HPD interrupt, it means the DisplayPort Sink device's status has changed.

When the HPD event is detected and interrupt is enabled, DisplayPort Tx IP could output a pulse on the int_o port and indicates the interrupt type on interrupt register 0x0188.

5.2 Transmit AUX Request Transaction (Ask a Question)

To transmit a Native Writing AUX Request transaction using DisplayPort Tx application, perform the following steps:

1. Write all the writing bytes into register 0x010C, write one byte for each writing operation.
2. Write the DPCD address into register 0x0104.
3. Write (WritingBytesNum-1) into register 0x0108.
4. Write ((WritingBytesNum << 16) | (0x00000001 << 8) | 0x00000008) into registers 0x0100.

To transmit a Native Reading AUX Request transaction using DisplayPort Tx application, perform the following steps:

1. Write the DPCD address into register 0x0104.
2. Write (ReadingBytesNum-1) into register 0x0108.
3. Write ((0x00000000<<16) | (0x00000001<<8) | 0x00000009) into registers 0x0100.

To transmit a I2C-Over-AUX Writing Request transaction using DisplayPort Tx application, perform the following steps:

1. Write all the writing bytes into register 0x010C, write one byte for each writing operation.
2. Write the DPCD address into register 0x0104.
3. Write (WritingBytesNum-1) into register 0x0108.
4. Write ((WritingBytesNum << 16) | (0x00000001 << 8) | (MOT<<2) | 0x00000000) into registers 0x0100.

To transmit a I2C-Over-AUX Reading Request transaction using DisplayPort Tx application, perform the following steps:

1. Write the DPCD reading address into register 0x0104.
2. Write (ReadingBytesNum-1) into register 0x0108.
3. Write ((0x00000000<<16) | (0x00000001<<8) | (MOT<<2) | 0x00000001) into registers into 0x0100.

5.3 Receive AUX Reply Transaction (Ask a Question)

After sending an AUX Request transaction to the DisplayPort Sink device, DisplayPort Source application software should wait for the AUX Reply transaction. When the AUX Reply is arrived and interrupt is enabled, DisplayPort Tx IP could output an interrupt signal and record this event in the interrupt register.

To read the received AUX Reply transaction from DisplayPort Tx IP, perform the following steps:

1. Read register 0x012C to know AUX Reply transaction length AuxReplyByteNum.
2. Read register 0x0124 AuxReplyByteNum times to get all the AUX Reply Transaction bytes.

3. Software checks the Reply type by checking the first reading transaction byte bit [7:4], it could be AUX ACK, NACK, or AUX DEFER. Bit [3:0] is reserved.
4. If AuxReplyByteNum > 1, the followed bytes are reading data from the DPCD registers.

5.4 DisplayPort Lanes Training (Ask a Question)

At the first training stage, DisplayPort Tx IP should output TPS1 to get the attached DisplayPort Sink device to get LANEx_CR_DONE.

To enable TPS1 transmission, perform the following steps:

1. Write enabled lane number into register 0x0004, it could be enabled 4 lanes and 2 lanes.
2. Write 0x01 into register 0x0018 to enable TPS1.
3. Write 0x00 into register 0x0010 to disable scrambler.

At second training stage, according to the DisplayPort Sink device feature, DisplayPort Tx IP should output TPS2/TPS3/TPS4 to get the attached DisplayPort Sink device to get LANEx_EQ_DONE, LANEx_SYMBOL_LOCKED, and INTERLANE_ALIGN_DONE.

To enable TPS2/TPS3/TPS4 transmission, perform the following steps:

1. Write enabled lane number into register 0x0004. It could be enabled 4 lanes and 2 lanes.
2. To transmit TPS2, write 0x02 into register 0x0018 to enable TPS2. For TPS3, writing 0x03. For TPS4, writing 0x04.
3. For TPS2 and TPS3, write 0x00 into register 0x0010 to disable scrambler. For TPS4, write 0x01 to enable scrambler.

In the training procedure, before sending the TPS pattern, DisplayPort Source application software might need to configure Transceiver SI settings and the Transceiver rate. The Transceiver is not part of this IP, and the Transceiver settings configuration guide is not included in this user guide.

5.5 Video Stream Transmission (Ask a Question)

After training is completed, DisplayPort Tx IP transmits the video stream to the sink device. To enable video transmission, perform the following steps:

1. Enable scrambler, write 0x01 into register 0x0010.
2. Configure MSA, configure registers from address 0x00C0 to address 0x00EC.
3. Enable video transmission, write 0x01 into register 0x0000.

5.6 Register Definition (Ask a Question)

The following table shows the internal registers defined in DisplayPort Tx IP.

Table 5-1. DisplayPort Tx IP Registers

Address	Bits	Name	Type	Default	Description
0x0000	[0]	video_stream_enable	RW	0x0	Enable video stream transmission
0x0008	[2:0]	lane_number	RW	0x4	DisplayPort enabled lane number: 4, 2, or 1
0x0010	[0]	scrambler_enable	RW	0x0	Enable scrambler
0x0014	[0]	Interlane_skew_enable	RW	0x1	Enable Inter lane skew
0x0018	[2:0]	training_pattern_mode	RW	0x0	Training pattern type: 0: None, 1: TPS1, 2: TPS2, 3: TPS,. and 4: TPS4.
0x001C	[0]	enhanced_BS_enable	RW	0x0	Enable Enhanced BS transmission
0x00C0	[23:0]	MSA_Mvid	RW	0x0	MSA Mvid for synchronous video clock mode
0x00C4	[23:0]	MSA_Nvid	RW	0x0	MSA Nvid
0x00C8	[15:0]	MSA_HTotal	RW	0x0	MSA HTotal
0x00CC	[15:0]	MSA_VTotal	RW	0x0	MSA_VTotal

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Address	Bits	Name	Type	Default	Description
0x00D0	[15:0]	MSA_HStart	RW	0x0	MSA HStart
0x00D4	[15:0]	MSA_VStart	RW	0x0	MSA_VStart
0x00D8	[15]	MSA_HSync_Polarity	RW	0x0	MSA_HSync_Polarity
	[14:0]	MSA_HSync_Width	RW	0x0	MSA_HSync_Width
0x00DC	[15]	MSA_VSync_Polarity	RW	0x0	MSA_VSync_Polarity
	[14:0]	MSA_VSync_Width	RW	0x0	MSA_VSync_Width
0x00E0	[7:1]	MSA_MISC0_ColorIndicator	RW	0x0	MSA_MISC0_ColorimetryIndicator
	[0]	MSA_MISC0_SyncClock	RW	0x0	MSA_MISC0_SynchronousClock
0x00E4	[7:6]	MSA_MISC1_ColorIndicator	RW	0x0	MSA_MISC1_ColorimetryIndicator
	[5:3]	MSA_MISC1_Reserved	RW	0x0	MSA_MISC1_Reserved
	[2:1]	MSA_MISC1_Stero	RW	0x0	MSA_MISC1_SteroVideoAttributor
	[0]	MSA_MISC1_InterlaceEven	RW	0x0	MSA_MISC1_InterlacedVerticalTotalEven
0x00E8	[15:0]	MSA_HWidth	RW	0x0	MSA_HWidth
0x00EC	[15:0]	MSA_VHeigth	RW	0x0	MSA_VHeigth
0x0100	[23:16]	AUX_Tx_Data_Byte_Num	RW	0x0	The number of bytes to be transmitted in this AUX request transaction
	[8]	AUX_Tx_LengthField_Val	RW	0x0	1 means this AUX transaction transmission carries length field. 0 means this AUX transaction does not have length filed.
	[3:0]	AUX_Tx_Command	RW	0x0	AUX COMM[3:0] in this AUX transaction transmission
0x0104	[19:0]	AUX_Tx_DPCD_Address	RW	0x0	DPCD address in this AUX transaction transmission
0x0108	[7:0]	AUX_Tx_Length	RW	0x0	Length field in this AUX transaction transmission. It will no ignored if no Length field.
0x010C	[7:0]	AUX_Tx_Writting_Data	RW	0x0	For AUX Writing Request transaction, writing all the DPCD writing bytes into this register byte by byte.
0x0110	[18:0]	AUX_Reply_Timeout_Th	RW	0x001000	Waiting AUX Reply timeout threshold in aux_clk_i cycles
0x011C	[15:0]	AUX_TX_ Request_Num	RC	0x0	The number of AUX transactions to be transmitted
0x0120	[15:0]	AUX_RX_Reply_Num	RC	0x0	The number of AUX transactions to be received
0x0150	[15:0]	HPD_Status	RO	0x0	The status of input HPD signal
0x0154	[0]	HPD_IRQ	RC	0x0	Indicates if there is HPD interrupt
0x0180	[0]	IntMask_TotalInt	RW	0x1	Total interrupt mask. 1 means enable total interrupt and int_o
0x184	[5]	IntMask_HPD_Disconnect	RW	0x1	Interrupt mask for HPD disconnect event. 1 enable interrupt
	[4]	IntMask_HPD_Connect	RW	0x1	Interrupt mask for HPD connect event. 1 enable interrupt
	[3]	IntMask_HPD_IRQ	RW	0x1	Interrupt mask for HPD IRQ. 1 enable interrupt
	[2]	IntMask_AuxReplyTimeOut	RW	0x1	Interrupt mask for AUX Reply Timeout. 1 enable interrupt
	[1]	IntMask_NewAuxReply	RW	0x1	Interrupt mask for received AUX Reply. 1 enable interrupt
	[0]	IntMask_AuxTxDone	RW	0x1	Interrupt mask for AUX Request transmission done. 1 enable interrupt

...........continued

Address	Bits	Name	Type	Default	Description
0x0188	[16]	Int_total	RC	0x0	Interrupt: total interrupt
	[5]	Int_HPD_Disconnect	RC	0x0	Interrupt: HPD disconnect event
	[4]	Int_HPD_Connect	RC	0x0	Interrupt: HPD connect event
	[3]	Int_HPD_IRQ	RC	0x0	Interrupt: HPD IRQ
	[2]	Int_AuxReplyTimeOut	RC	0x0	Interrupt: AUX Reply Timeout
	[1]	Int_NewAuxReply	RC	0x0	Interrupt: Received new AUX Reply
	[0]	Int_AuxTxDone	RC	0x0	Interrupt: Transmission of AUX Request is done

5.7 Driver Configuration (Ask a Question)

You can find the driver files in the following path: ..\<Project_name>\component\Microchip\SolutionCore\dp_transmitter\<DisplayPort Tx IP version>\Driver.

6. Testbench (Ask a Question)

Testbench is provided to check the functionality of the DisplayPort Tx IP.

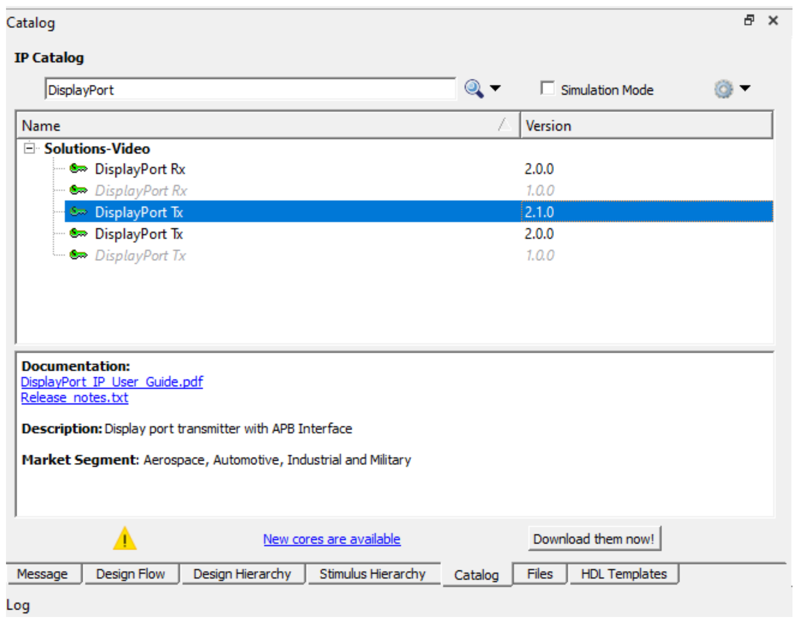
6.1 Simulation (Ask a Question)

To simulate the core using the testbench, perform the following steps:

1. Open Libero SoC **Catalog** tab, expand **Solutions-Video**, double-click **DisplayPort Tx**, and then click **OK**. The documentation associated with the IP are listed under **Documentation**.

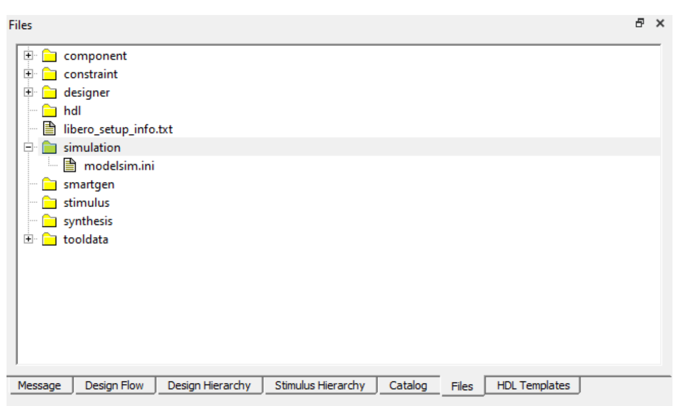
> **Important:** If you do not see the **Catalog** tab, navigate to **View** > **Windows** menu and click **Catalog** to make it visible.

Figure 6-1. DisplayPort Tx IP Core in Libero SoC Catalog



2. Go to the Files tab and select**simulation**, and then click **Import Files**.

Figure 6-2. Import Files

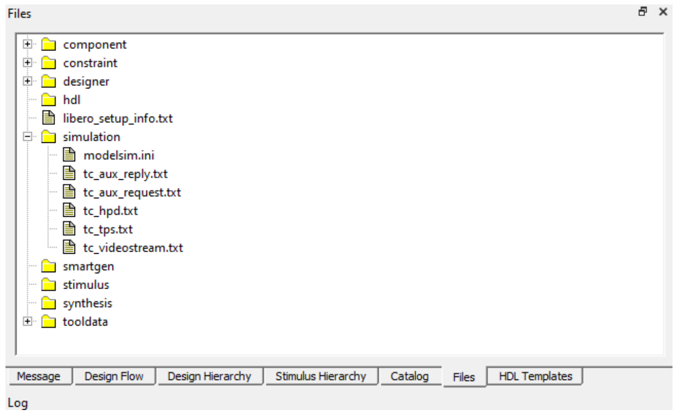


3. Import the `tc_videostream.txt`, `tc_tps.txt`, `tc_hpd.txt`, `tc_aux_reply` and `tc_aux_request` files from the following

path: ..\<Project_name>\component\Microchip\SolutionCore\ dp_transmitter\ <DisplayPort Tx IP version>\Stimulus.

4. To import a different file, browse the folder that contains the required file, and click **Open**. The imported file is listed under simulation, see the following figure.

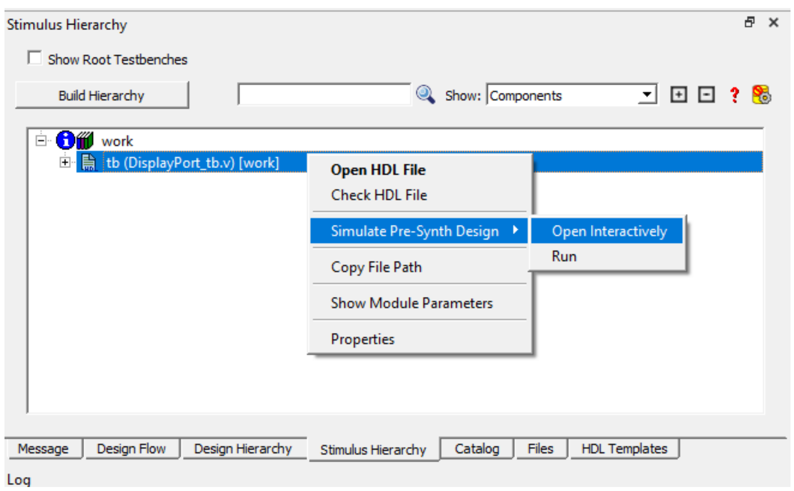
Figure 6-3. Imported Files



5. On the **Stimulus Hierarchy** tab, right click testbench (`DisplayPort_tb.v`), point to **Simulate Pre- Synth Design**, and then click **Open Interactively**.

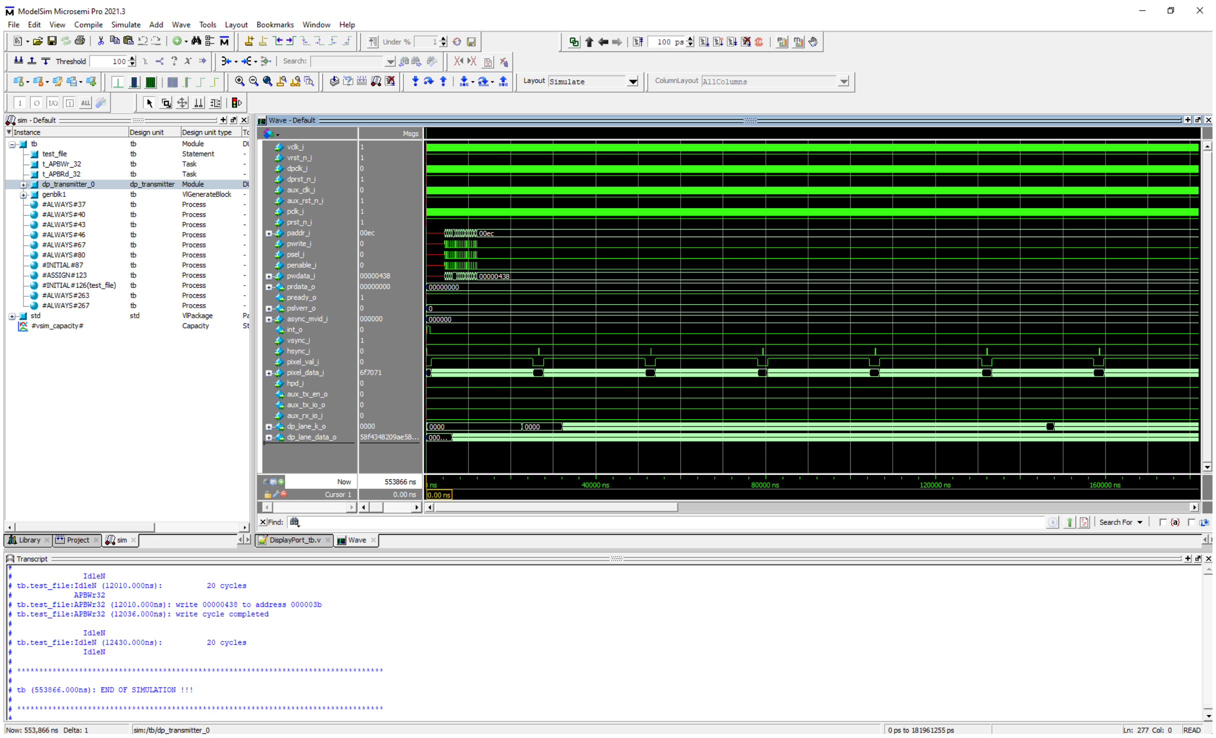
Important: If you do not see the **Stimulus Hierarchy** tab, navigate to **View** > **Windows** menu and click **Stimulus Hierarchy** to make it visible.

Figure 6-4. Simulating Pre-Synthesis Design



ModelSim opens with the testbench file, as shown in the following figure.

Figure 6-5. ModelSim Simulation Window



Important: If the simulation is interrupted due to the runtime limit specified in the `.do` file, use the `run -all` command to complete the simulation.

7. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 7-1. Revision History

Revision	Date	Description
A	04/2023	Initial release

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