TB3198

Capacitive Voltage Divider (CVD) Operation on 8-Bit PIC® Microcontrollers

Introduction

Author: Jason Layton, Microchip Technology Inc.

Microchip's Analog-to-Digital Converter with Computation (ADC^2) allows users to quickly and easily capture relative capacitance measurements on an analog pin by implementing the Capacitive Voltage Divider (CVD) feature. The internal sample and hold capacitor is utilized as a reference to an external conductive sensor during an ADC^2 acquisition. This feature of the ADC^2 can be used to simplify applications that implement capacitive touch or proximity sensing by reducing the amount of software needed, as well as lowering CPU overhead required for this functionality. The purpose of this technical brief is to give an overview of how to implement the CVD hardware included on the ADC^2 module and describe the basic operation and configuration of the CVD feature.

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1. CVD Overview

The CVD feature of the ADC^2 was developed to require only an Analog-to-Digital Converter and a very minimal amount of software to measure the capacitance of a pin connected to an external conductive sensor, such as a metal pad. By integrating the hardware needed for CVD sensing into the ADC^2 module, the need for external hardware and complex digital filtering is eliminated. Users can add capacitive touch and proximity sensing functionality into their application quickly without the need for external hardware or signal processing. The CVD allows the environmental changes around a capacitive sensor tied to an analog channel to be read and converted to a digital value by the ADC^2. The results of the ADC^2 conversion from the CVD reading can be easily processed and used by the PIC microcontroller.

1.1 CVD Operation

The ADC^2 module must be configured appropriately to utilize the internal capacitive voltage divider hardware to sense the capacitance on an analog channel. The CVD uses the internal ADC^2 sample and hold capacitor (C_{HOLD}) to form a voltage divider with an external conductive sensor. Through a series of steps, this allows the ADC^2 to capture the voltage on C_{HOLD}, which is directly related to the capacitance of the sensor tied to the channel. The internal ADC^2 sample and hold capacitance value may vary between devices, so it is important to refer to the device data sheet to verify specific electrical specifications. Figure 1-2 shows the waveform for a differential CVD measurement.

CVD operation begins with C_{HOLD} being disconnected from the path that connects it to the capacitive sensor. Doing this allows each capacitive component to be precharged to a known voltage level (V_{DD} or V_{SS}). When the precharge stage is complete, the acquisition stage of the CVD operation can begin. At this time, the path that connects C_{HOLD} to the external sensor is reconnected, allowing the voltage level between the two capacitive components to equally distribute. When C_{HOLD} and the external conductive sensor are connected, a capacitive voltage divider is created. The ADC^2 can then be used to measure the voltage level of C_{HOLD} and determine the capacitance of the channel.

Figure 1-1. Hardware Capacitive Voltage Divider Block Diagram

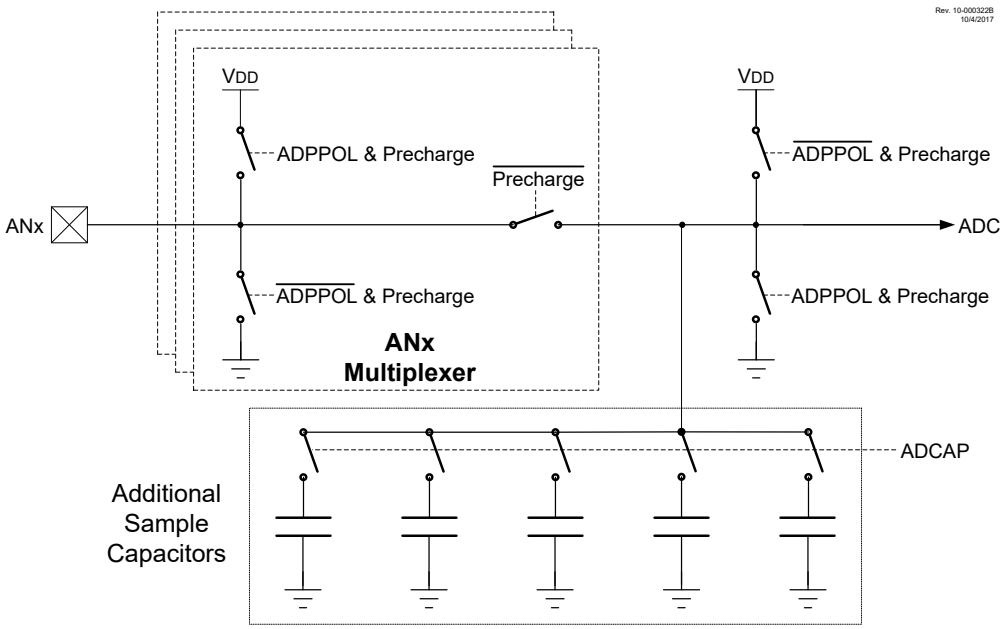
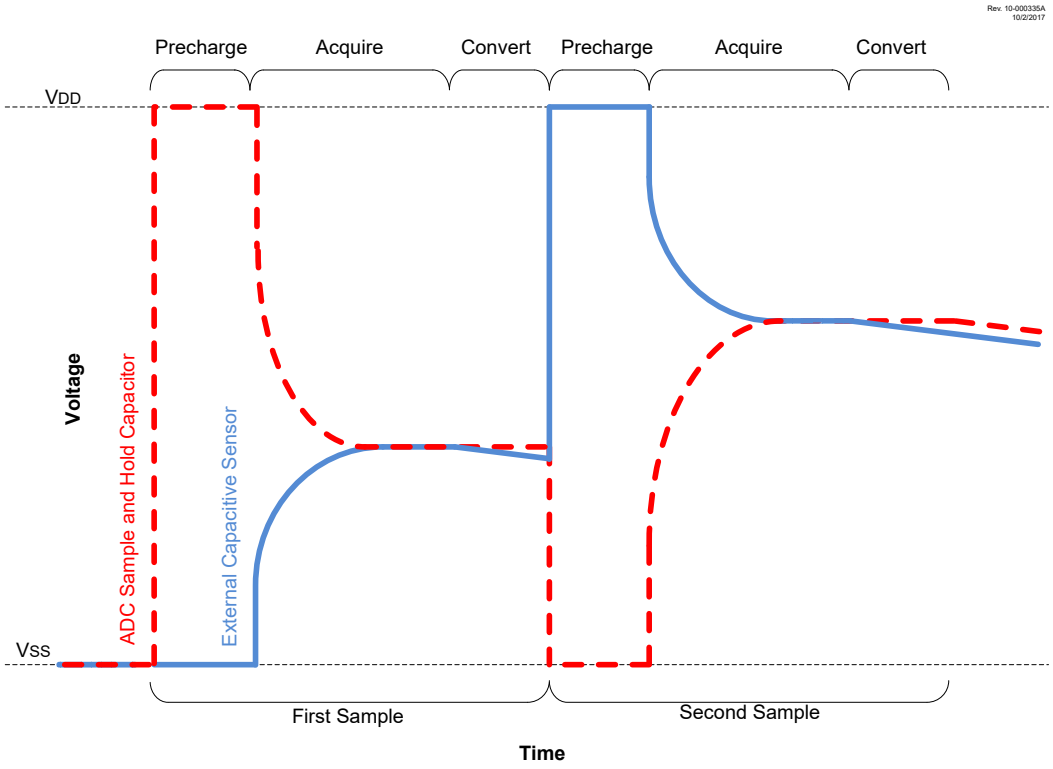


Figure 1-2. Differential CVD Measurement Waveform



The CVD feature allows users to quickly configure the ADC^2 module to be used for capacitive sensing applications in software. The registers associated with the configuration of the CVD are listed below.

- ADC Precharge Polarity (ADCON1)
- 13-Bit ADC Precharge Time (ADPREL/H)
- ADC Acquisition Time (ADACQL/H)
- Additional Sample and Hold Capacitor configuration (ADCAP)
- Guard Ring Outputs and Polarity (ADCON1)

2. ADC^2 and CVD Configuration

With the CVD being an integrated feature of the ADC^2 module, it is important to make sure that the ADC^2 is properly configured for use. The first step is to ensure that the I/O pin is configured correctly. The output driver on that port must be disabled by setting the corresponding bit in the TRISx register and configuring the pin as an analog channel by setting the corresponding bit in the ANSELx register. Once this has been completed, the next step is to configure the ADC^2 module. Refer to Microchip's ADC^2 Technical Brief (TB3146) or the device data sheet for more specific information about configuration of the ADC^2. A few key settings are mentioned below:

- ADC^2 Conversion Clock Selection (ADCLK/ADCON)
- Voltage Reference Selection (ADPREF/ADNREF)
- Analog Channel Selection (ADPCH)
- Enable/Turn on ADC Module (ADCON)

The next step is to configure the CVD specific registers in the ADC^2 module. These are covered in more detail later in this technical brief, however, it is important to remember to set up precharge control, acquisition control, additional sample and hold capacitance and the guard ring circuit. The CVD feature offers the ability to choose where the previous sample input select bits come from by setting the PSIS bit of the ADCON register.

2.1 CVD Precharge Control

CVD operation begins with an optional precharge state, where the external capacitive sensor and the internal C_{HOLD} capacitor are charged to known and opposite voltage levels (either V_{SS} or V_{DD}). The user needs to ensure that both sensors have enough time to charge completely to a known voltage level to ensure an accurate reading from the external sensor. The amount of time allocated for the precharge stage is determined by the value written to the corresponding precharge timer register (ADPRE). Reference the device data sheet to determine the size of the precharge timer register. The precharge polarity of the internal sample and hold capacitor and external sensor on the configured analog pin is determined by the value written to the PPOL bit of the appropriate ADCON register.

CVD operation can either be configured to perform one conversion for each trigger, or two conversions for each trigger (differential CVD). Double sampling can be enabled by setting the DSEN bit of the appropriate ADCON register. When performing a differential CVD operation, the A/D Inverted Precharge bit should be enabled (IPEN = `1`) to configure the precharge and guard signals in the second conversion cycle to precharge opposite of what was done for the first conversion. It is also important to determine the guard ring polarity during the precharge stage by setting the GPOL bit of the ADCON register. Refer to Example 2-1, which demonstrates the initialization of the appropriate ADC^2 registers to set up the precharge stage during a CVD operation. Refer to 3.1 Guard Ring Circuit for more information on the Guard Ring Circuit.

2.2 CVD Acquisition Control

Once C_{HOLD} and the external capacitive sensor are precharged to opposite known voltages, the line between the two is connected, effectively forming a capacitive voltage divider. The reconnection of C_{HOLD} and the external sensor that forms the voltage divider signifies the beginning of the acquisition stage. During the acquisition stage, the previously opposite voltage levels between the two will equalize to a middle value based upon the relationship of C_{HOLD} and the external capacitance on the sensor. After the

acquisition stage, the ADC^2 samples the voltage level of C_{HOLD}, which represents the relative capacitance measured on the analog channel.

The acquisition stage of the CVD operation is an optional period to allow C_{HOLD} to charge or discharge from the selected analog channel before the ADC^2 collects the sample. The ADC^2 module offers the flexibility to set the acquisition time during CVD operation to allow charge averaging between the precharged channel and the C_{HOLD} capacitor. The user can control the acquisition time (charge share time) by writing to the ADACQL/H register pair. For the ADC^2 to meet the specified accuracy, C_{HOLD} must be allowed to fully charge to the analog input channel voltage level. There are several things that can influence the minimum required time for acquisition. Refer to the device data sheet for more information about ADC acquisition requirements. Example 2-2 demonstrates how to configure the acquisition time for CVD operation using the PIC18F25K42 microcontroller. Example 2-3 provides an example of how the one would perform a CVD measurement using the ADC module. Note that minor changes may need to be made for this example to work on other PIC devices with this CVD feature.

Example 2-1. ADC Module Setup for CVD Measurement

```
// ADCC & CVD Initialize

ADRPT = 0x1F;   // ADC Repeat Threshold Bits;
ADACQL = 0x0A;  // ADC Acquisition Time Control Register (Low);
ADACQH = 0x00;  // ADC Acquisition Time Control Register (High);
ADCAP = 0x00;   // Additional Sample and Hold Capacitance;
ADPREL = 0x0A;  // ADC Pre-charge Time Control Register (Low);
ADPREH = 0x00;  // ADC Pre-charge Time Control Register (High);
ADCON1 = 0x00;  // ADC Control Register 1;
        // ADCON1bits.PPOL = Precharge Polarity Bit;
        // ADCON1bits.IPEN = ADC Inverted Precharge Polarity Enable Bit;
        // ADCON1bits.GPOL = Guard Ring Polarity Selection Bit;
        // ADCON1bits.DSEN = Double Sample Enable Bit;
ADCON2 = 0xD3;  // ADC Control Register 2;
ADCON3 = 0x00;  // ADC Control Register 3;
ADREF = 0x00;   // ADC Voltage Reference Selection Register;
ADCLK = 0x00;   // ADC Clock Selection Register;
ADCON0 = 0x84;  // ADC Control Register 0;
ADACT = 0x00;   // ADC Auto Conversion Trigger Control Register;
```

3. Additional Sample and Hold Capacitance

A unique feature of the integrated CVD hardware is the software adjustable additional capacitance that can be added in parallel with C_{HOLD}. The user can add an additional 1-31 pF by writing to the ADCAP register. Refer to the device data sheet for the specific register values and the corresponding added capacitance. In the event where the ADCAP register is left empty, no additional capacitance will be added. The additional capacitance is only connected during the precharge and acquisition stages and does not affect ADC^2 performance or timing. When used in CVD applications this feature allows the user to better match the internal sample capacitance to the external conductive sensor. Matching the internal and external capacitance can help improve sensitivity and performance of the sensor. Refer to Example 2-1, which shows how to add additional sample and hold capacitance.

3.1 Guard Ring Circuit

The ADC^2 module features a guard ring circuit that supports the integrated hardware capacitive voltage divider. In applications where more accuracy is required, the guard ring circuit can be implemented to increase the accuracy of the external sensor to capacitive changes. High impedance sensors, like conductive pads that are implemented in many touch applications, can be more susceptible to external noise. The guard ring circuitry can be used to ground any noise from unexpected changes in the electromagnetic field that the capacitative sensor may be exposed to. Two digital guard ring outputs (ADGRDA/ADGRDB) and the associated voltage divider resistors in the circuit are used to drive the guard ring voltage. The guard ring polarity and precharge are controlled using the GPOL and IPEN bits of the ADC^2 configuration registers. The two guard ring pins are configurable using Peripheral Pin Select (PPS). Refer to the device data sheet for more information regarding the timing and implementation of the guard ring circuit. Refer to Example 2-1, which shows how the guard ring circuit would be initialized and configured.

4. Conclusion

This technical brief gave an overview of the CVD feature integrated into the ADC^2 module and explained how it can be implemented in an application. By utilizing the built-in CVD hardware, the ADC^2 can perform relative capacitive measurements on any analog pin by using the internal sample and hold capacitance as a reference. The CVD offers the flexibility to work with several different types of sensors and meet the needs of the user. Refer to Microchip's ADC^2 Technical Brief (TB3146) as a resource when configuring the ADC^2 for CVD functionality. For more information or specifications pertaining to the CVD refer to the device data sheet.

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