

## Configurable Logic Cell on PIC<sup>®</sup> Microcontrollers

*Author: Swathi Sridhar  
Microchip Technology Inc.*

### INTRODUCTION

The Configurable Logic Cell (CLC) is an innovative peripheral that allows for the on-chip creation of custom logic functions for PIC<sup>®</sup> microcontrollers. The CLC provides programmable, combinational and sequential logic that operates independently of the CPU execution. The CLC can be used for interconnecting peripherals and designing general purpose logic, thus replacing the need for external circuitry.

### CONFIGURABLE LOGIC CELL (CLC) OVERVIEW

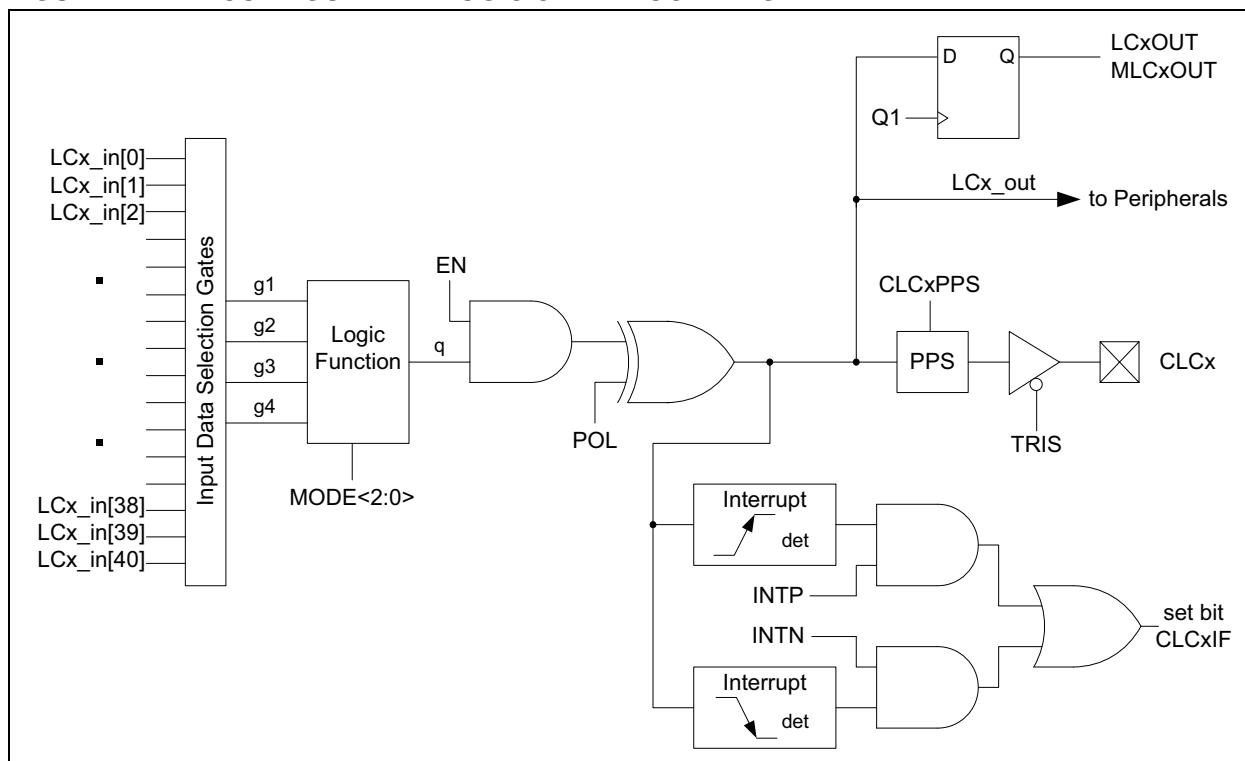
The CLC is user configurable similar to a Programmable Logic Device (PLD). The CLC can implement a variety of logic functions. A variety of

inputs, internal and external, can be routed to this module. CLC receives inputs from other peripherals or from an input pin. It then performs the intended logic operation and provides output that can be used to control other peripherals or another I/O pin. Logic functions can be achieved via programming, using Special Function Registers associated with the peripheral. The CLC can be used to operate even when the microcontroller is in Sleep mode. CLC helps in simplifying on-chip interconnection of peripherals when it is configured. External glue logic functions on the PCB can be eliminated by using the CLC, thus reducing board space. In addition, the logic functions implemented using CLC also save code space.

The following four sections are used to configure the CLC module:

- Data Selection
- Data Gating
- Logic Function Selection
- Output Polarity

**FIGURE 1: CONFIGURABLE LOGIC CELL BLOCK DIAGRAM**



## Data Selection

CLC receives a number of signals as inputs. Input sources are a combination of the following:

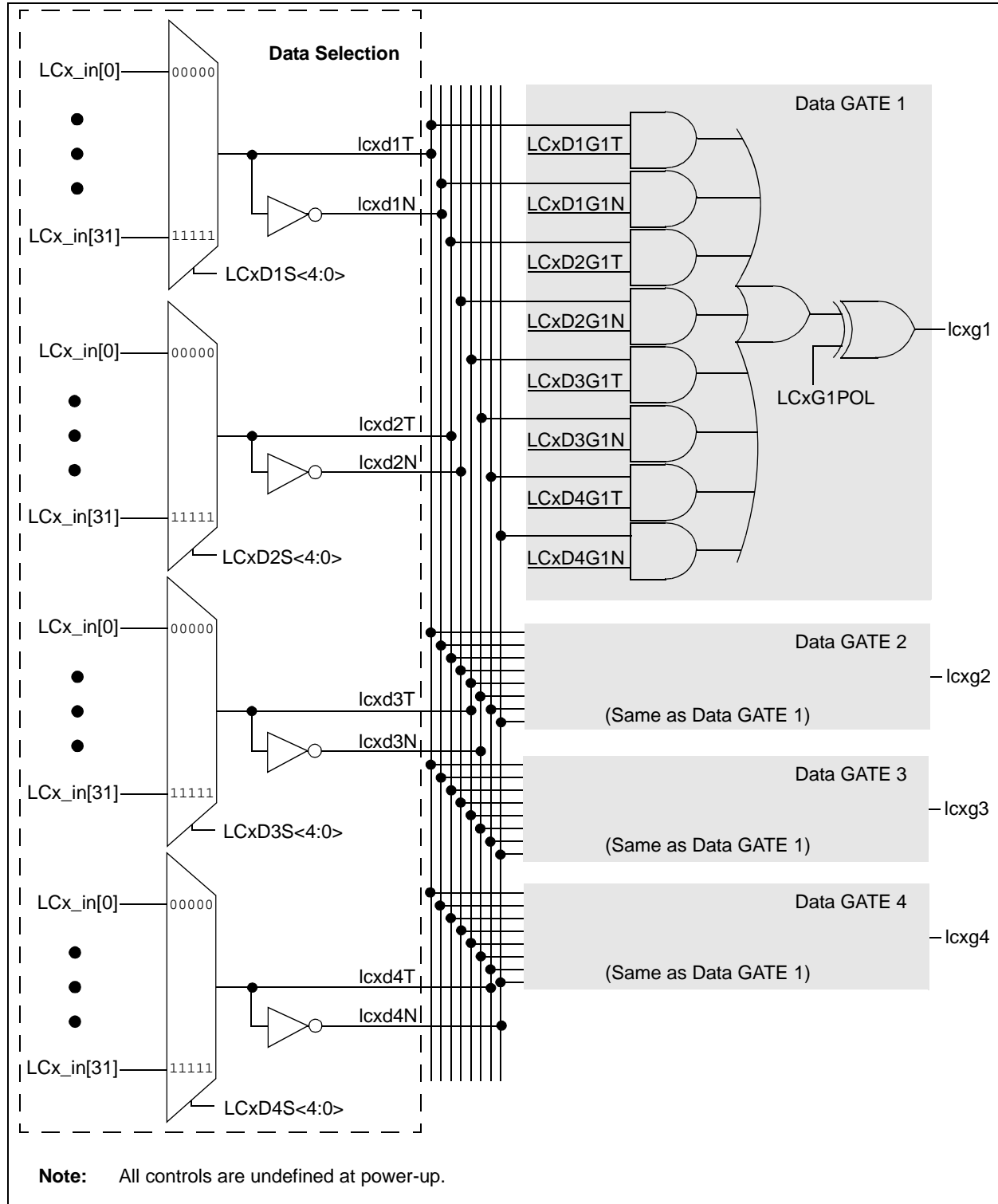
- I/O Pins
- Internal Clocks
- Peripherals
- Register Bits

Data selection is done through four multiplexers. Each multiplexer can have up to 32 inputs. The output of each of these multiplexers acts as an input to the logic functions. There are eight selectable single output logic functions to which the multiplexer outputs can be connected. The CLC input signals can be selected from the four registers, CLCxSEL0 through CLCxSEL3.

## Data Gating

Output of the multiplexers from the input stage are directed to the desired logic function through the data-gating stage. Each data gate can direct any combination of the four multiplexer outputs. The data-gating stage can be used for directing the input signal and also for configuring the directed input as inverted or non-inverted data. [Figure 2](#) displays the data-gating stage.

FIGURE 2: DATA SELECTION AND GATING STAGE



The output of the data selection stage provides both the true value and the negated value of the selected signal. It is at this stage that the user decides whether the true or the negated value of the signal is needed for the next stage. Each input to the data-gating section has a pair of bits in its respective CLCxGLSx register. The two bits

include a non-inverted bit 'T' and an inverted bit 'N' that needs to be set up. If the 'N' bit is set, then the negated input is selected. The selected (true or negated) signals are ORed to form the data gate output. The CLCxPOL register bit, LCxGxPOL, will invert or non-invert the output of the gate.

## Logic Function Selection

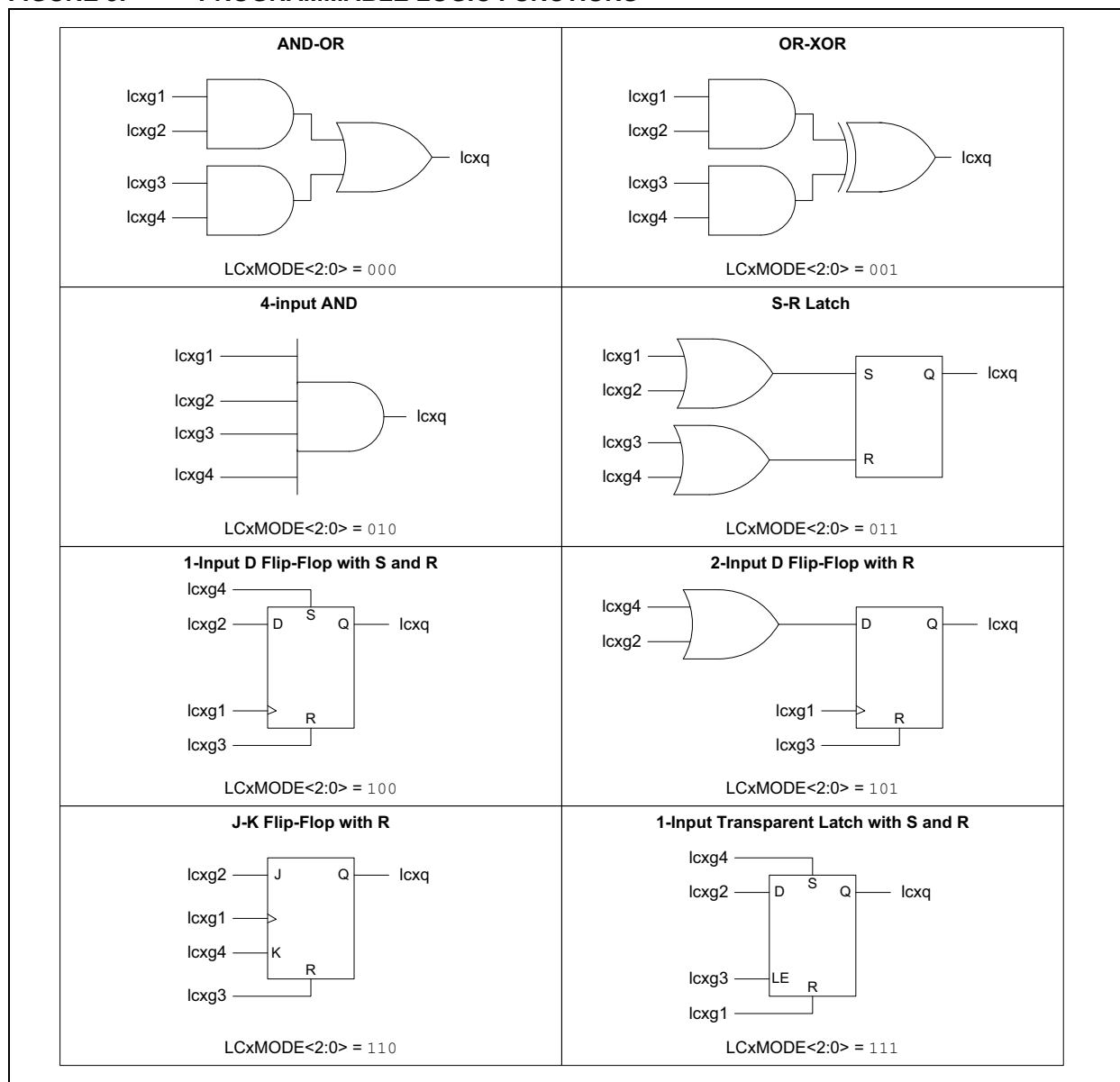
The outputs of the data-gating stage are inputs to the logic function selection stage. The four inputs are reduced to one output which can further be used as an input to any other peripheral or to drive an output pin. The desired logic function is selected with the  $LCxMODE<2:0>$  bits of the  $CLCxCON$  register.

There are eight available logic functions:

- AND-OR ( $LCxMODE<2:0> = 000$ )
- OR-XOR ( $LCxMODE<2:0> = 001$ )
- AND ( $LCxMODE<2:0> = 010$ )
- S-R Latch ( $LCxMODE<2:0> = 011$ )
- D Flip-Flop with Set and Reset ( $LCxMODE<2:0> = 100$ )
- D Flip-Flop with Reset ( $LCxMODE<2:0> = 101$ )
- J-K Flip-Flop with Reset ( $LCxMODE<2:0> = 110$ )
- Transparent Latch with Set and Reset ( $LCxMODE<2:0> = 111$ )

Figure 3 shows the different programmable logic functions.

**FIGURE 3: PROGRAMMABLE LOGIC FUNCTIONS**



## Output Polarity

The output polarity stage is the last stage in a CLC. We can select the desired polarity of the logic output with the LCxPOL bit of the CLCxCON register.

## CONFIGURATION OF THE CLC PERIPHERAL

Operation of the peripheral is controlled by the following registers:

- CLCxCON: It is used to enable the module and, more importantly, to select the logic function
- CLCxPOL: It is used to control the logic polarity of both the cell output and the intermediate variables
- CLCxSELx: The inputs are selected by the LCxDxS<5:0> bits in this register. There might be up to four data select registers.
- CLCxGLSx: This register allows the user to form an input to the logic function stage from an OR or AND of the data bus signals derived from the data selection stage. Either the true or negated values of each data signal can be chosen.

Table 1 contains the summary of registers associated with the CLC.

**TABLE 1: REGISTERS ASSOCIATED WITH CLC**

| Name     | Bit 7    | Bit 6    | Bit 5       | Bit 4    | Bit 3    | Bit 2        | Bit 1    | Bit 0    |
|----------|----------|----------|-------------|----------|----------|--------------|----------|----------|
| CLCxCON  | LCxEN    | LCxOE    | LCxOUT      | LCxINTP  | LCxINTN  | LCxMODE<2:0> |          |          |
| CLCxPOL  | LCxPOL   | —        | —           | —        | LCxG4POL | LCxG3POL     | LCxG2POL | LCxG1POL |
| CLCxSEL0 | —        | —        | LCxD1S<5:0> |          |          |              |          |          |
| CLCxSEL1 | —        | —        | LCxD2S<5:0> |          |          |              |          |          |
| CLCxSEL2 | —        | —        | LCxD3S<5:0> |          |          |              |          |          |
| CLCxSEL3 | —        | —        | LCxD4S<5:0> |          |          |              |          |          |
| CLCxGLS0 | LC1G1D4T | LC1G1D4N | LC1G1D3T    | LC1G1D3N | LC1G1D2T | LC1G1D2N     | LC1G1D1T | LC1G1D1N |
| CLCxGLS1 | LC1G2D4T | LC1G2D4N | LC1G2D3T    | LC1G2D3N | LC1G2D2T | LC1G2D2N     | LC1G2D1T | LC1G2D1N |
| CLCxGLS2 | LC1G3D4T | LC1G3D4N | LC1G3D3T    | LC1G3D3N | LC1G3D2T | LC1G3D2N     | LC1G3D1T | LC1G3D1N |
| CLCxGLS3 | LC1G4D4T | LC1G4D4N | LC1G4D3T    | LC1G4D3N | LC1G4D2T | LC1G4D2N     | LC1G4D1T | LC1G4D1N |

Example 1 is the code snippet used to demonstrate the ANDing of two signals using the CLC.

### EXAMPLE 1: CODE SNIPPET FOR ANDING TWO SIGNALS USING THE CLC

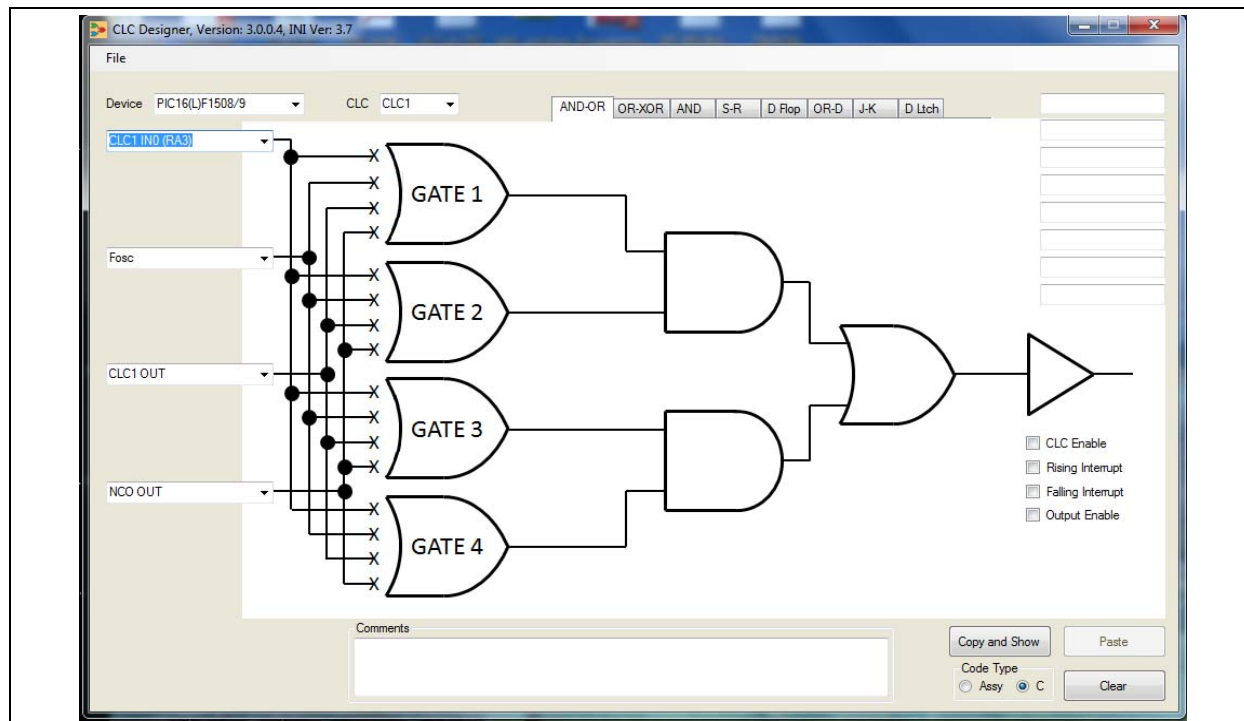
```
//CLC Setup
CLC1POL = 0x00;//Output of the logic cell is not inverted
CLC1SEL0 = 0x06;//Input Data selection 0
CLC1SEL1 = 0x0C;//Input Data selection 1
CLC1SEL2 = 0x04;//Input Data selection 2
CLC1SEL3 = 0x06;//Input Data selection 3
CLC1GLS0 = 0x02;//Input 1 is not inverted
CLC1GLS1 = 0x20;//Input 2 is inverted
CLC1GLS2 = 0xAA;//Input 3 is not inverted
CLC1GLS3 = 0x80;//Input 4 is not inverted
CLC1CON = 0x80;//CLC enabled; MODE AND-OR
```

## CLC Configuration Tool and MPLAB® Code Configurator for CLC

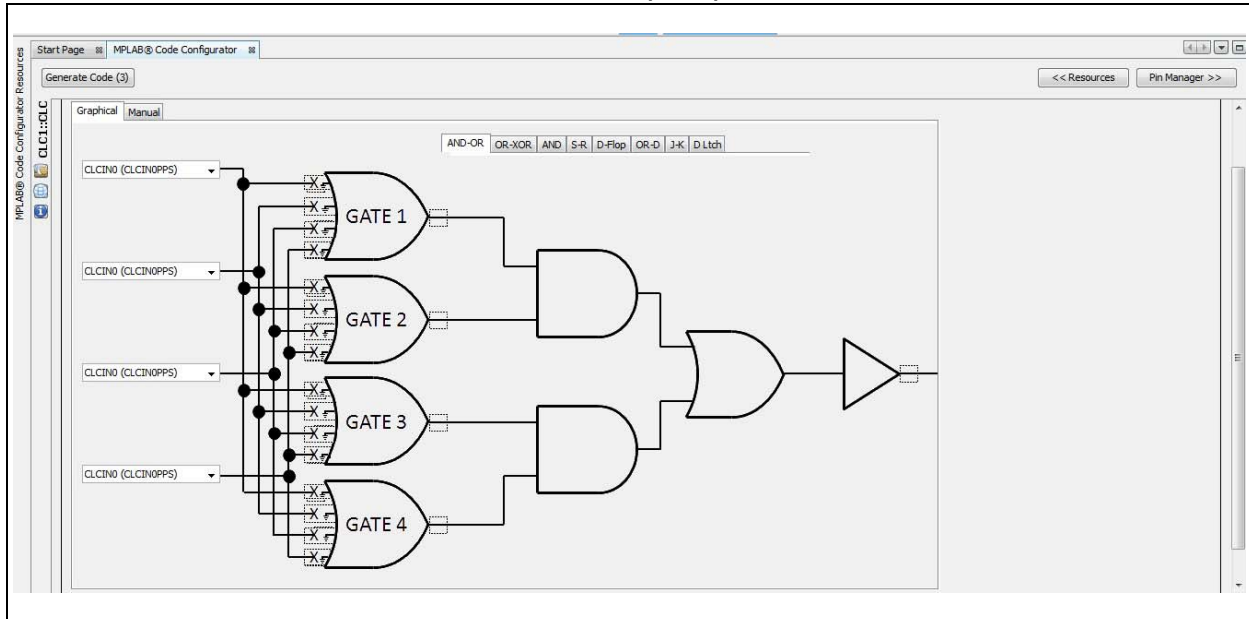
Configuration of the CLC module can be easily done with the help of the GUI-based tools, which help the user visualize the CLC structure and generate the code for the settings. The CLC configuration tool and the MPLAB® Code Configurator are the tools that help in streamlining the setup process of the CLC module and simulate the register settings in a graphical user interface.

The CLC configuration tool generates the source code either in C or Assembly, which can be incorporated into the existing MPLAB® X project. [Figure 4](#) shows the CLC configuration tool GUI. For further details refer to the “Configurable Logic Cell (CLC) Configuration Tool User’s Guide”(DS41597).

**FIGURE 4: CLC CONFIGURATION TOOL GUI**



The MPLAB Code Configurator, which is a plug-in tool for MPLAB X IDE, generates the drivers based on the settings and selections made in the GUI. MCC incorporates the CLC configuration tool and it outputs only C code. [Figure 5](#) shows the MPLAB Code Configurator GUI.

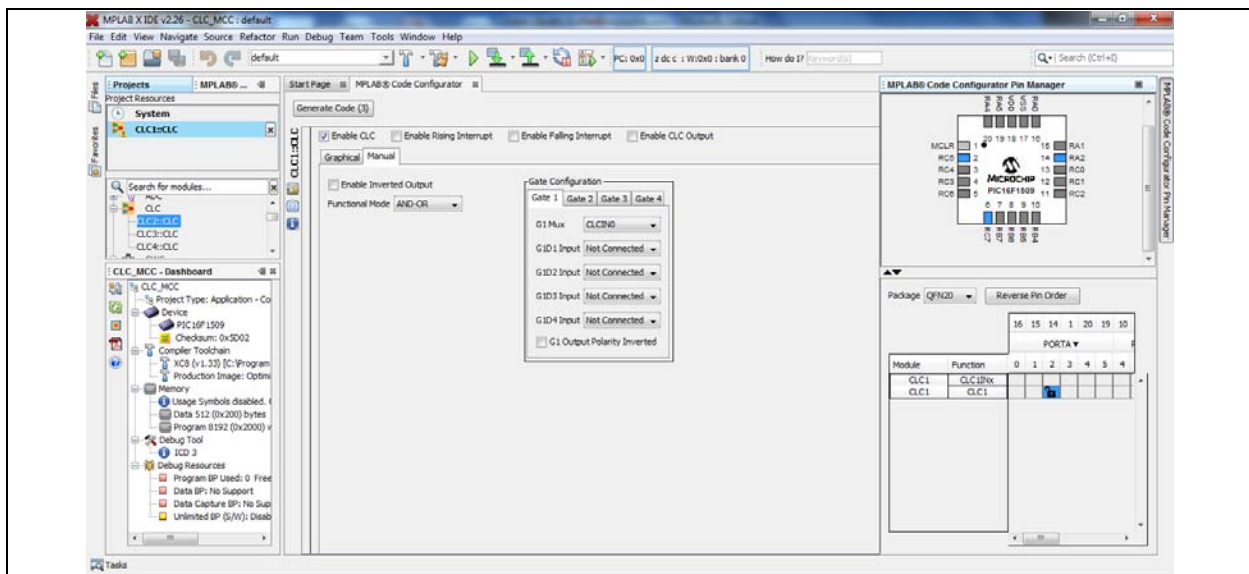
**FIGURE 5: MPLAB® CODE CONFIGURATOR (MCC) FOR CONFIGURABLE LOGIC CELL**

The composer area for the CLC has two tabs:

- Graphical
- Manual

In the Graphical tab (see [Figure 5](#)), the user can visualize the CLC structure and do the setup.

In the Manual tab (see [Figure 6](#)), the same settings can be done in the drop-down feature to configure all the Special Function Registers of the CLC. The tool generates the driver for the settings provided by the user. For further details refer to the “MPLAB® Code Configurator User's Guide” (DS40001725).

**FIGURE 6: MANUAL TAB IN MPLAB® CODE CONFIGURATOR (MCC) FOR CONFIGURABLE LOGIC CELL**

## CLC API List

The following API is generated by MCC for the CLC module:

- `void CLC1_Initialize(void)`: This API initializes the CLCxCON, CLCxPOL, CLCxGLSx and CLCxSELx registers

## CONCLUSION

Realization of various digital logic functions such as basic gates, flip-flops and latches can be achieved using the CLC peripheral on PIC microcontrollers. CLC offers the advantage of designing these logic functions on-chip, thereby eliminating a lot of additional circuitry on the board. In addition, many of the logic functions used for Fault activation, decision making and event handling that are conventionally done in software can easily be achieved using the CLC. This technical brief aims at familiarizing the reader with the functionality of the CLC and how programmable combinational and sequential logic can be achieved without intervention of the CPU. More details are available on the device-specific data sheet.

## REFERENCES

1. *Configurable Logic Cell (CLC) Configuration Tool User's Guide* (DS41597)
2. *Configurable Logic Cell Tips'n Tricks* (DS41631)
3. *MPLAB® Code Configurator User's Guide* (DS40001725)



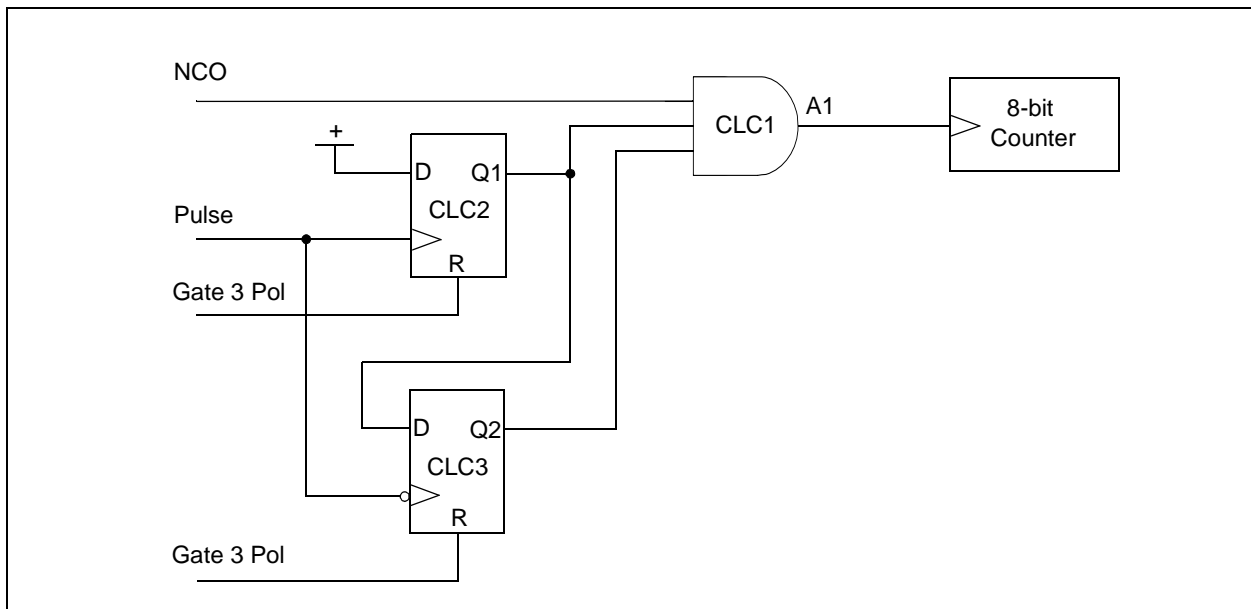
## APPENDIX A: APPLICATIONS OF THE CONFIGURABLE LOGIC CELL

### A.1 Servo Pulse Measurement Circuit

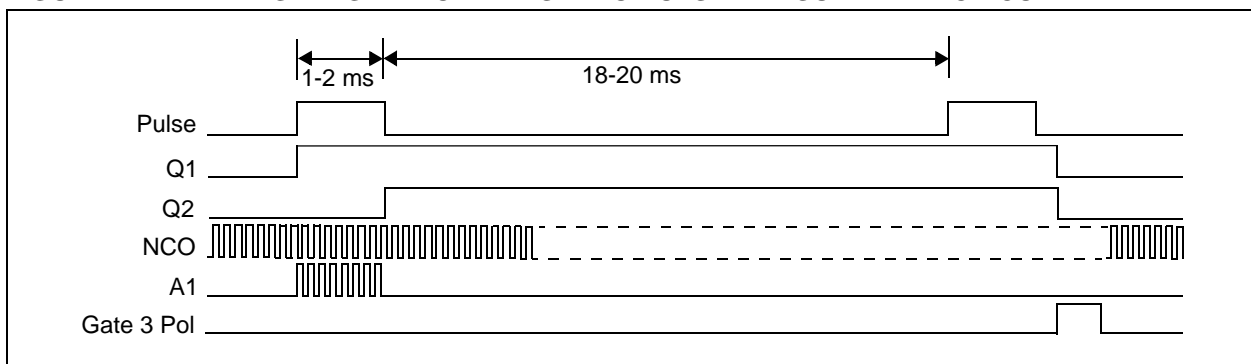
The pulse width of a periodic signal, such as that of a servo control signal, can be measured using the CLC along with other peripherals such as a Numerically Controlled Oscillator (NCO) and Timer0 on PIC microcontrollers (see [Figure A-1](#)). In the circuit exemplified in [Figure A-1](#), Timer0 is used as an 8-bit counter. This circuit captures a pulse from the pulse stream and provides a measurement count. The NCO output is used as a clock for the 8-bit counter. An RC receiver typically generates servo control pulses of varying width every 20 ms. The width of the pulse is between 1 to 2 ms.

The NCO frequency is selected as 200 kHz. The circuit is reset by presetting the counter to 56 and strobing the Gate 3 Pol bits high. The rising edge of the pulse sets Q1 and the falling edge sets Q2. When Q1 is high and Q2 is low, the counter counts at the NCO frequency. The operation is illustrated in the waveform in [Figure A-2](#). At 1 ms the counter rolls from 255 to 0, and at 2 ms the count is 200. Pulse is ready to be read when Q2 goes high. The count is held until the circuit is reset to capture another pulse. The circuit is reset to capture another pulse. CLC3 input from the CLC2 Q output synchronizes the pulse measurement after the asynchronous Reset.

**FIGURE A-1: SERVO PULSE MEASUREMENT CIRCUIT USING THE CLC**



**FIGURE A-2: TIMING DIAGRAM OF THE SERVO PULSE MEASUREMENT CIRCUIT**



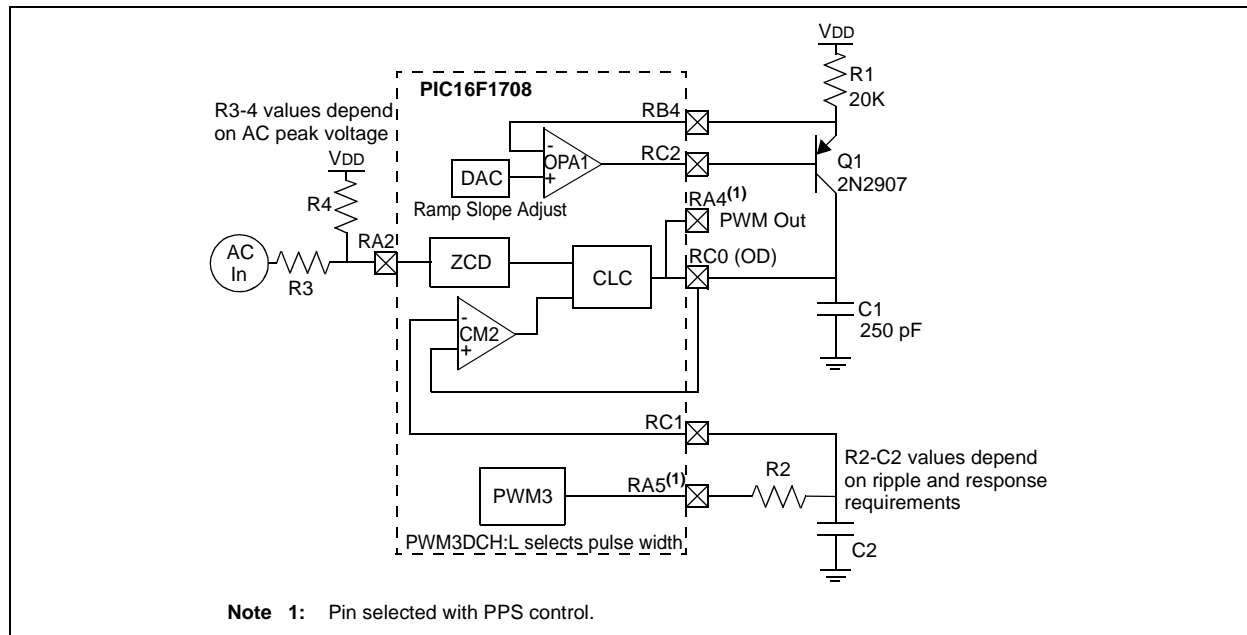
## A.2 10-Bit PWM Synchronous with AC Input

The PWM output can be made synchronous with the AC input with the help of on-chip peripherals such as the CLC, Zero-Cross Detect (ZCD) and comparator (CM2). In the circuit illustrated in Figure A-3, the CLC block consists of two CLC instances (CLC1 and CLC2). CLC1 is implemented as an XOR gate of the CLC2 and ZCD outputs. The CLC2 output is implemented as a D flip-flop, with ZCD output at the D input, and the comparator output rising edge at clock input. A ZCD change triggers CLC1 output to go high. When CLC1 becomes high, it enables the constant-current charge of C1 through the open-drain configuration of RC0.

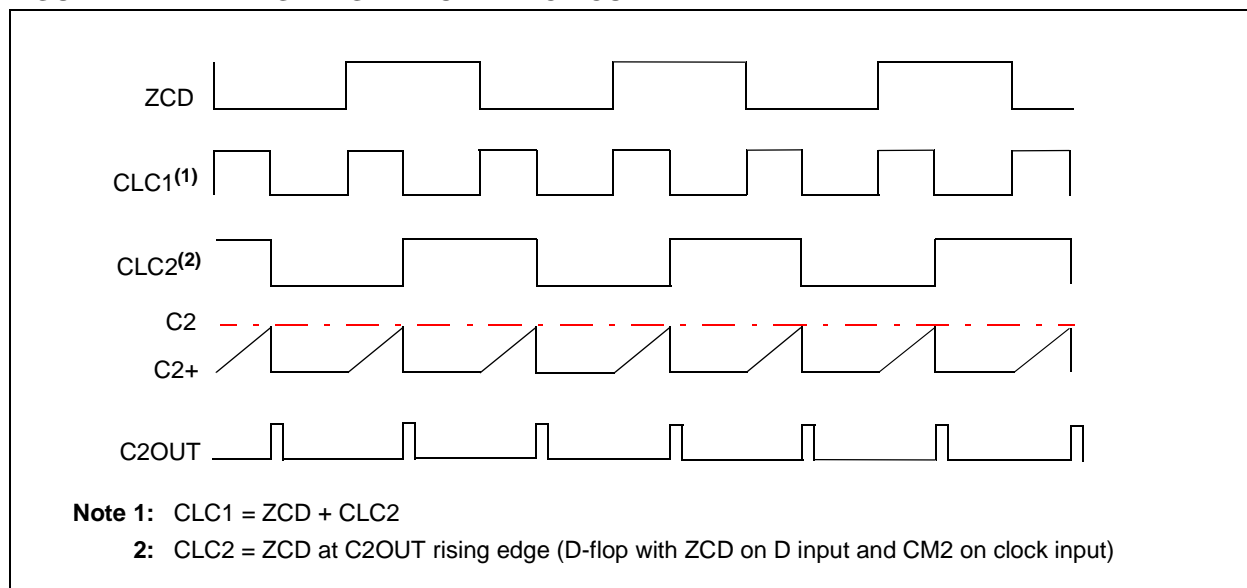
When C1 voltage reaches the voltage on C2, CM2 triggers CLC2 to the same level as the ZCD output, thereby forcing CLC1 output low. CLC1 low output discharges C1 through RC0 open-drain output until the next ZCD change. C2 voltage is set by the PWM3 duty cycle. Figure A-4 illustrates the timing diagram of the circuit.

OPA1, R1 and Q1 form a constant-current source for the linear charge of C1. DAC is the current source adjustment to match the C1 voltage ramp to the AC input half cycle.

**FIGURE A-3: CIRCUIT FOR MAKING PWM SYNCHRONOUS WITH AC INPUT**



**FIGURE A-4: TIMING DIAGRAM OF THE CIRCUIT**



---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, flexPWR, JukeBlox, KEELOQ, KEELOQ logo, Klear, LANCheck, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC<sup>32</sup> logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

The Embedded Control Solutions Company and mTouch are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, ECAN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, KlearNet, KlearNet logo, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, RightTouch logo, REAL ICE, SQI, Serial Quad I/O, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2015, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-63277-202-2

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**= ISO/TS 16949 =**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Austin, TX**  
Tel: 512-257-3370

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Novi, MI  
Tel: 248-848-4000

**Houston, TX**  
Tel: 281-894-5983  
Indianapolis

**Noblesville, IN**  
Tel: 317-773-8323  
Fax: 317-773-5453

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**New York, NY**  
Tel: 631-435-6000

**San Jose, CA**  
Tel: 408-735-9110

**Canada - Toronto**  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon

**Hong Kong**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Dongguan**  
Tel: 86-769-8702-9880

**China - Hangzhou**  
Tel: 86-571-8792-8115  
Fax: 86-571-8792-8116

**China - Hong Kong SAR**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8864-2200  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

### ASIA/PACIFIC

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-3019-1500

**Japan - Osaka**  
Tel: 81-6-6152-7160  
Fax: 81-6-6152-9310

**Japan - Tokyo**  
Tel: 81-3-6880-3770  
Fax: 81-3-6880-3771

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-5778-366  
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7828

**Taiwan - Taipei**  
Tel: 886-2-2508-8600  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Dusseldorf**  
Tel: 49-2129-3766400

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Germany - Pforzheim**  
Tel: 49-7231-424750

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Italy - Venice**  
Tel: 39-049-7625286

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Poland - Warsaw**  
Tel: 48-22-3325737

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**Sweden - Stockholm**  
Tel: 46-8-5090-4654

**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820