

Microchip MPU Power Solutions Tips and Tricks

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1.0 INTRODUCTION

This document demonstrates a number of solutions that enable or facilitate the application of Microchip Power Management Integrated Circuits (PMICs) targeted to MPU power to nonstandard use cases.

These solutions include methods to:

- implement a reliable start-up/restart upon initial application or restoration of the input voltage, using PWRHLD as a normal enable pin. For more information, see [Section 2.0, Using PWRHLD as an ENABLE](#).
- eliminate external power train components of Buck1, when the generation of the I/O voltage (typically, 3.3V) is not required (for example, because it is already available). The method can be also extended to other Buck channels. For more information, see [Section 3.0, Reducing BOM cost in applications with VIN=3.3V](#).
- convert the Buck1 channel into a simple noninverting Buck-Boost, with the addition of two inexpensive and small discrete components. For more information, see [Section 4.0, Buck1 Channel In Noninverting Buck-Boost Configuration](#).

1.1 MCP16501/2 Description

The MCP16501/2 are cost and size-optimized PMICs, compatible with Microchip's Embedded Microprocessors Units (EMPU), requiring Dynamic Voltage Scaling (DVS) with the use of High-Performance mode (HPM, MCP16502 only). MCP16501/2 are compatible with SAMA5D2, SAM9X6 and SAMA7G MPUs, which are supported by dedicated device variants.

MCP16501 integrates three DC-DC Buck regulators and one auxiliary Low-Dropout (LDO) while the MCP16502 has four DC-DC Buck regulators and two auxiliary LDOs.

All Buck channels can support loads up to 1A and are 100% duty cycle-capable.

The 300 mA LDOs enable support for sensitive analog loads.

The DDR memory voltage (Buck2 output) is selectable by means of two 3-state input pins. This method allows greater precision in the output voltage setting by eliminating inaccuracies due to external feedback resistors, while minimizing external component count. The voltage selection set allows easy migration across different memory generations.

The default power channel sequencing is built-in, according to the requirements of the MPU. A dedicated pin (LPM) facilitates the transition to Low-Power modes and the implementation of backup mode with DDR in self-refresh (Hibernate mode).

MCP16501/2 feature a low, no-load operational quiescent current, under 300 μ A.

Active discharge resistors are provided on each output and the output active discharge feature is enabled by default. A pre-biased output safe start-up protects the device in case of incomplete output capacitor discharge.

Note: On the MCP16502, the output active discharge feature can be disabled through I²C.

1.2 MCP16501/2 Features

- Input voltage: 2.7V to 5.5V
- 1A Output Current Buck Channels with 100% Maximum Duty Cycle Capability
- 2 MHz Buck Channels PWM Operation
- 300 mA Low-Dropout Linear Regulators (LDOs)
- +1% Voltage Accuracy for DDR (Buck2 Output), Core (Buck3 output) and CPU (Buck4 output, MCP16502)
- Pin-Selectable Output Voltages for Buck2: 1.2V, 1.35V, 1.8V
- MPU-Specific Built-in Default Channels Sequencing and nRSTO Assertion Delay
- Support of Hibernate (MCP16501/2), Low-Power (MCP16501/2) and High-Performance Modes (MCP16502) with DVS
- 1 MHz I²C Interface for Programming and Diagnostics (MCP16502)
- Leakage-Free Interfacing to MPU in Any Operating Condition through Optimized ESD Protection
- Cost and Size-Optimized BOM
- Thermal Shutdown and Current Limit Protection

2.0 USING PWRHLD AS AN ENABLE

2.1 Role of PWRHLD for Start-Up

A typical application start-up sequence can be initiated in two different ways, depending on the presence of a backup supply in the application:

1. nSTRT event (nSTRT pin pulled low), maintained by PWRHLD assertion. In applications with a backup battery, the PWRHLD signal is typically already high before the nSTRT event. A capacitor (connected to the nSTRT pin) can be used to delay the rise of nSTRT enough to automatically trigger a start-up event.
2. A low-to-high transition of the PWRHLD signal, regardless of the nSTRT event, when the PWRHLD pin is driven exclusively by the MPU SHDN pin. This is only possible in applications with backup supply (Figure 1). This mode is typically originated by an external wake-up event asserted by a peripheral device of the MPU Shutdown and Wake-up Controller (SHDWC), which is still powered in Backup mode.

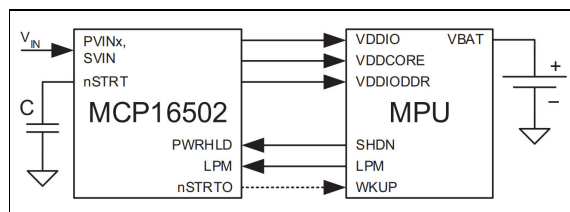


FIGURE 1: Application with a Backup Supply Block Diagram.

In other application scenarios, it is desirable to turn on the power rails based on a single, level-sensitive logic input (such as a normal ENABLE pin), which may be connected directly to the input voltage to achieve automatic start-up upon application of the input voltage. The nSTRT capacitor method described in the data sheets can provide a solution if the dynamics of the input supply voltage are predictable.

However, when the input voltage is unstable or the rise time is long or unknown, the PMIC might fail to power up through the delay caused by the capacitor on nSTRT. In such cases, the nSTRT capacitor method cannot be used. The recommended solution is to use the PWRHLD input, which is sensitive to a rising edge when used to command the PMIC start-up.

To be recognized as a valid start-up event, the PWRHLD rising edge must occur after the input voltage (applied to the SVIN pin) has risen above the internal UVLO threshold of the PMIC (V_{UVLO_TH} in the data sheets' EC Table) and has been above it long enough for the internal boot to complete (about 100 μ s, assume 200 μ s for extra margin).

In conclusion, in applications where the PWRHLD is not driven by other MPU/MCU signals and all that is needed is a simple enable command activated by the input voltage, the use of an input voltage monitoring circuit driving the PWRHLD input appears to be the most logical solution. The trip threshold of the input voltage monitor must be above the internal PMIC UVLO threshold under all circumstances, and some small amount of delay (200 μ s or more) must be provided before PWRHLD transitions from LOW to HIGH. It should also be noted that this technique allows the user to program the input voltage turn-on and turn-off thresholds, thus overriding the internal UVLO level.

Figure 2 exemplifies the input voltage instability problem. When power is first applied, the regulator starts normally (using an nSTRT capacitor). If VIN falls under the UVLO threshold without resetting the nSTRT capacitor, the regulator shuts down and the PMIC does not automatically restart.

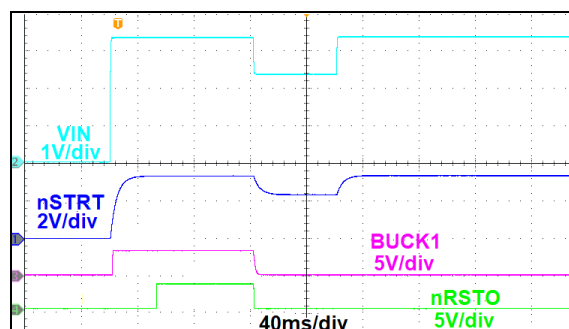


FIGURE 2: Unstable VIN.

The second problem is caused by slow rise of VIN (Figure 3). Because the start-up condition is dictated by the nSTRT capacitor, if VIN rises too slowly, the delay may not be sufficient. Increasing the capacitor is not always a solution, as this may cause increased start-up delays when not necessary and there might still be situations when VIN rises too slowly to trigger a start-up.

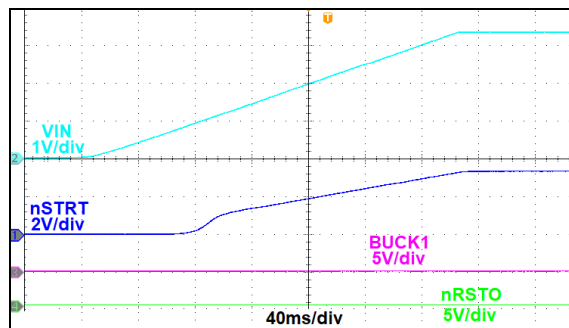


FIGURE 3: Slow Input Voltage Rise.

With regards to the input voltage monitor circuits driving PWRHLD, some solutions and their experimental performance are described in the following pages.

2.2 Voltage Supervisor with Built-In Delay

Voltage supervisors work by monitoring the rail voltage and, depending on the internally set threshold, assert a signal if the monitored voltage is within limits or de-assert it if the monitored voltage is out of spec.

Requiring only a decoupling capacitor and a pull-up resistor, a very simple voltage monitoring circuit can be designed using MIC803 (Figure 4).

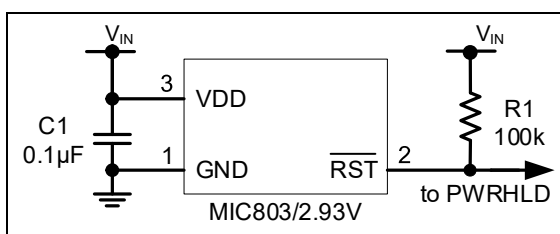


FIGURE 4: MIC803 Voltage Supervisor Schematic.

This circuit has the advantage of having a supervisor built-in assertion delay, so fast variations in the input voltage cause a low-high transition only after the delay has passed. This means that, in the case of an unstable input voltage, the circuitry remains in reset and the MCP16501/2 starts only after the input voltage has stabilized.

The delay can be selected when choosing the part number: 20 ms, 140 ms or 1120 ms, with a recommended threshold of 2.93V for a typical 3.3V rail.

Figure 5 exemplifies the start-up behavior of the system when MIC803 is used.

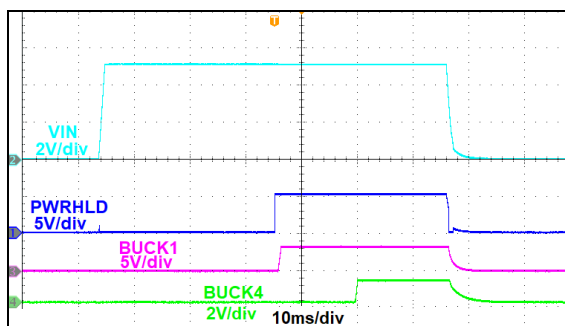


FIGURE 5: MCP16502 Start-Up Using MIC803.

When a slow input voltage ramp is applied, the MIC803 voltage supervisor correctly monitors the input voltage and after the 2.93V threshold is hit and the delay time has passed, PWRHLD is allowed to go high (Figure 6).

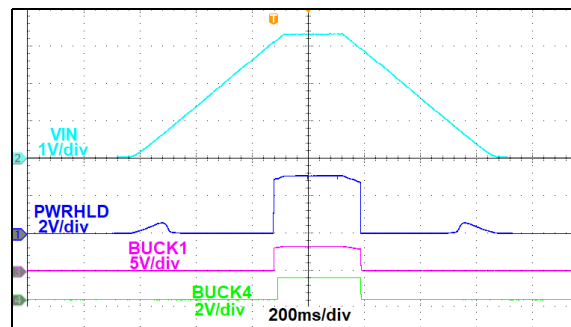


FIGURE 6: Slow Input Voltage Response Using MIC803.

The MIC803 response when the input voltage falls can be seen in Figure 7.

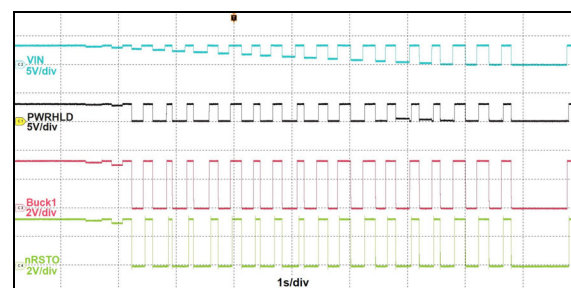


FIGURE 7: Decreasing VIN Step Response Using MIC803.

Each VIN step decrease represents an approximate 5% of nominal input voltage for a 3.3V system. The VIN wave shape used in Figure 7 mimics the stimulus described in ISO16750-2:2012 for Reset Behavior at Voltage Drop test [1]. The first few steps are over the 2.93V threshold so the MCP16501/2 remains operational. When VIN drops under the threshold, a shutdown event is triggered and, when VIN returns to normal, a start-up event is correctly generated and the nRSTO behavior is clean.

2.3 Automotive Supervisor with 120 ms Delay

For automotive applications, MCP102 can be used instead. For a 3.3V nominal input voltage, a 2.93V monitoring voltage option should be used (Figure 8).

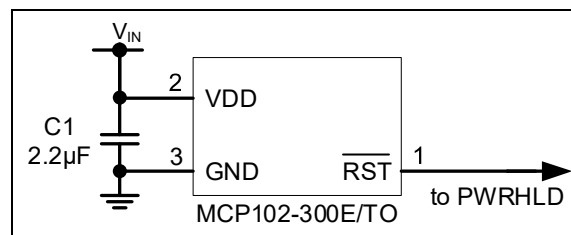


FIGURE 8: MCP102 Automotive Voltage Supervisor Schematic.

The MCP1XX family of supervisors offer the options of push-pull (MCP102/3), open-drain (MCP121) or open-drain with internal pull-up resistor (MCP131) variants for increased flexibility.

Figure 9 shows the start-up delay included in the MCP102 family of devices.

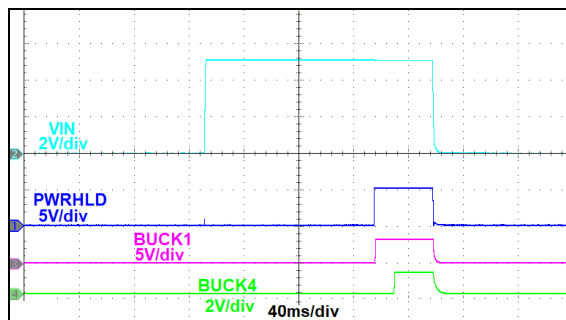


FIGURE 9: MCP16502 Start-Up Using MCP102.

When a slow input voltage ramp is applied, the MCP102 correctly monitors the voltage. While the voltage is ramping up, it triggers a start-up event after the correct voltage is detected and 120 ms have passed. This delay is only present when the input voltage is rising; when VIN falls, the supervisor immediately signals a shutdown (Figure 10).

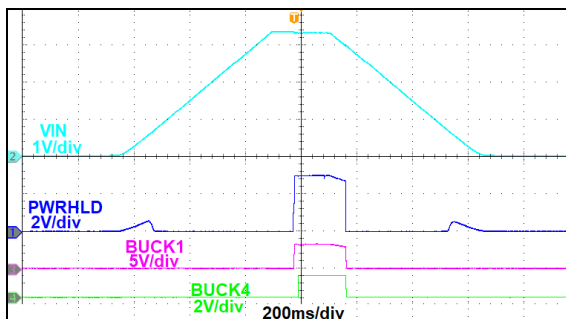


FIGURE 10: Slow Input Voltage Response Using MCP102.

Figure 11 exemplifies the behavior when the input voltage decreases with 5% every step for a 3.3V input voltage system. Again, the VIN waveform used in Figure 11 mimics the stimulus described in ISO16750-2:2012 for Reset Behavior at Voltage Drop test.

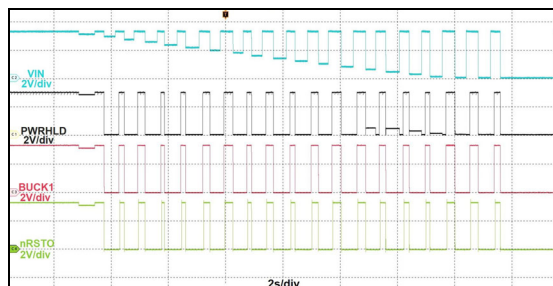


FIGURE 11: Decreasing VIN Step Response Using MCP102.

The first step does not fall below the minimum threshold, so the PWRHLD signal is maintained. However, when VIN starts decreasing below the minimum threshold, the MCP102 circuit begins generating shutdown events. When VIN goes back to regulation, the MCP102 correctly generates start-up events and the nRSTO behavior is clean.

2.4 Comparator-Based Solution with User-Selectable ON Delay

In applications when specific thresholds or delays are desired, a discrete circuit can be used. Using the MIC841N is a great option here. Having fixed internal reference and high and low threshold input pins, the user can select (using three resistors) the high and low thresholds, implementing a custom hysteresis. The delay is achieved through a combination of pull-up resistor (R4) and capacitor (C1) RC delay. The PWRHLD transition is generated by a Schmitt trigger, the 74LVC1G17 (Figure 12). Using a 360 kΩ resistor with 0.022 μF capacitor, a delay of approximately 6 ms is obtained. This delay is best observed in Figure 13.

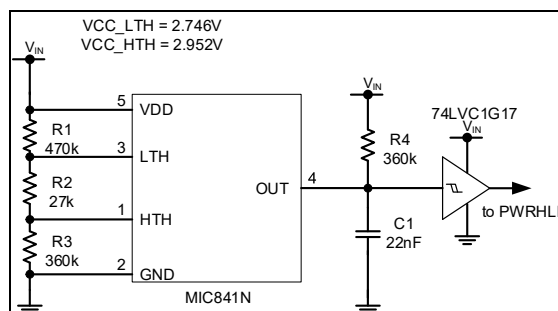


FIGURE 12: MIC841N Based Schematic.

For a 3.3V nominal system voltage, 2.95V was selected as the high threshold voltage and the 2.75V was selected as the low threshold voltage, resulting in a 200 mV hysteresis. To take full advantage of the good threshold accuracy of the MIC841N ($\pm 1.25\%$), 1% precision resistors should be used for R1, R2 and R3.

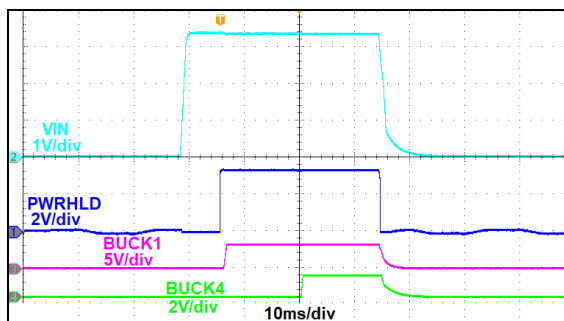


FIGURE 13: MCP16502 Start-Up Response Using MIC841N Circuit.

When a slow input voltage is applied, the delay is less visible and the system is turned on in proximity of the input voltage rising threshold crossing (see Figure 14).

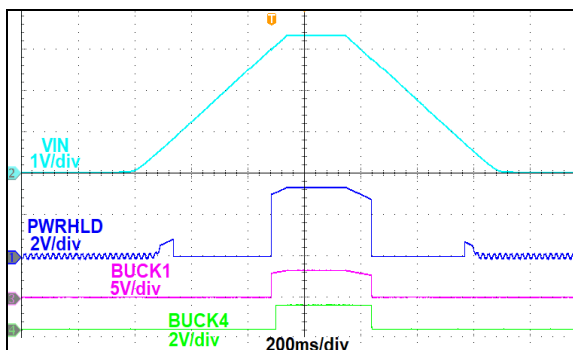


FIGURE 14: Slow Input Voltage Response Using MIC841N Circuit.

Figure 15 exemplifies the behavior when the input voltage decreases by 5% more for each step.

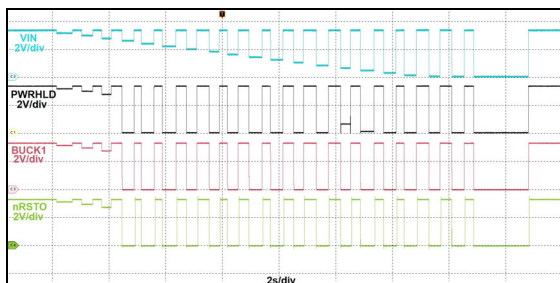


FIGURE 15: Decreasing VIN Step Response Using MIC841N Circuit.

In this case, the input voltage falls by more than 15% before the monitoring circuit starts generating shutdown and start-up events.

2.5 PGOOD Based Circuit When Pre-Regulator is Used

There are also cases when the main rail voltage is greater than the maximum input voltage of the MCP16501/2, for example 12V. In this case, a pre-

regulator must be used, for example the MCP16361. By using the Power Good output pin of the MCP16361, the PMIC can be controlled to power up or shutdown, depending on the situation.

A delay can also be added by using a pull-up resistor to the output voltage of the pre-regulator and a capacitor, thus forming an RC delay. Because of the slow PGOOD ramp, a Schmitt trigger should be used to generate clean and sharp low-to-high and high-to-low transitions for the PWRHLD (Figure 16).

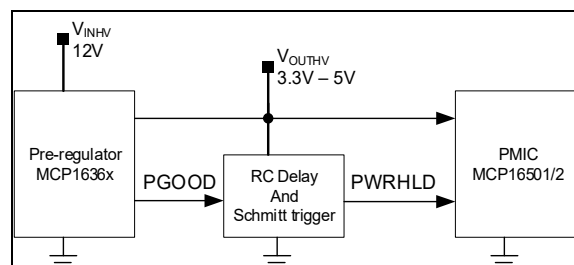


FIGURE 16: MCP16501/2 with MCP1636x Block Diagram.

The actual schematic as well as the RC values for the delay are below (Figure 17).

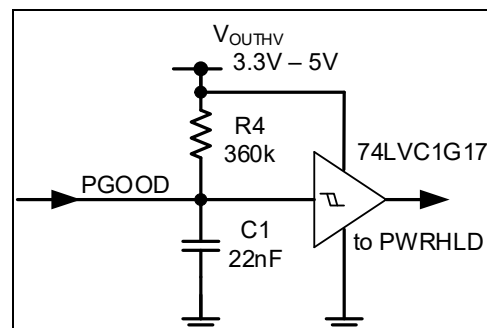


FIGURE 17: RC Delay and Schmitt Trigger.

Figure 18 shows the fast VIN step response of the MCP16361 and MCP16502 pair when the PMIC is enabled by the MCP16361 PGOOD circuit.

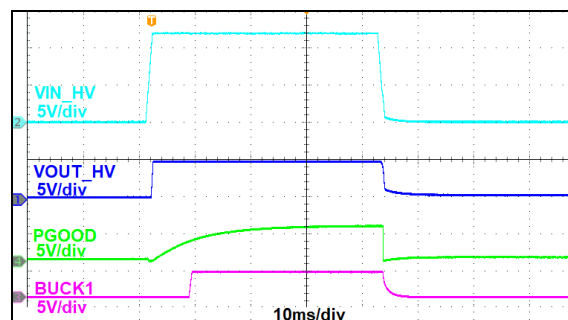


FIGURE 18: System Response with Pre-Regulator.

When testing MCP16361 with a slow-rising input voltage, although there is voltage present on its output, the PMIC does not start unless the PGOOD signal goes high. This ensures that the attached load can start and operate normally (Figure 19).

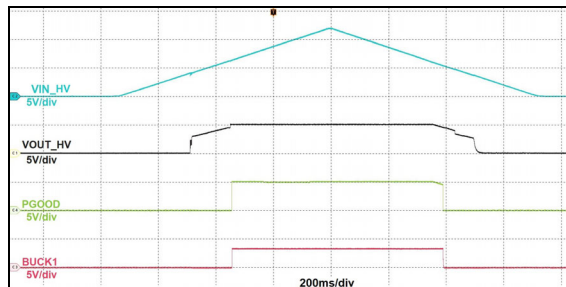


FIGURE 19: System Response with Slow-Rising Input Voltage.

Because of the pre-regulator, while testing the line step response where the high-voltage input decreases by 5% each step, the system is much more tolerant to decreases in the main input voltage V_{INH} .

For a 12V nominal input, the input voltage can decrease as much as 5.5V before seeing variations in the output voltage of 5V.

Here, when the output voltage goes below the PGOOD threshold (93% nominal), the system generates a shutdown and only after V_{OUTHV} goes back into regulation, the system is restarted (Figure 20).

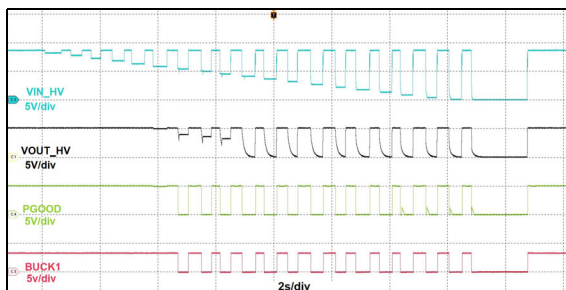


FIGURE 20: System Response to Decreasing Input Voltage.

2.6 Discrete Input Voltage Monitoring for 3.3V Main Supply Systems

If a very low-cost solution is desired, and board space and quiescent current are less of a concern, a circuit composed of TLV431 (precision shunt regulator), a transistor and a few passive components can be used, together with a dual Schmitt trigger inverter to generate the appropriate PWRHLD transition (Figure 21).

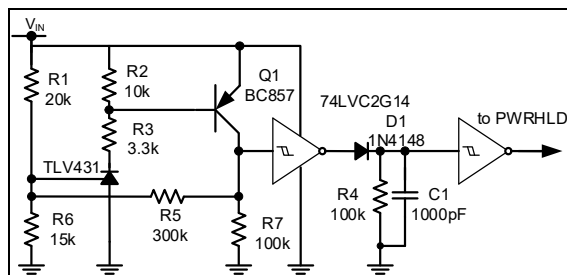


FIGURE 21: Discrete 3.3V Input Voltage Monitor Schematic.

This circuit has the advantage of being highly customizable, as the trigger voltage, hysteresis and delay can be easily changed.

The threshold voltage can be adjusted by the R1 and R6 pair that set the reference voltage for the TLV431, the hysteresis is mainly dictated by R5.

The Schmitt triggers, along with D1, R4 and C1, add a delay and square the signal for PWRHLD.

The fast step response is presented below (Figure 22).

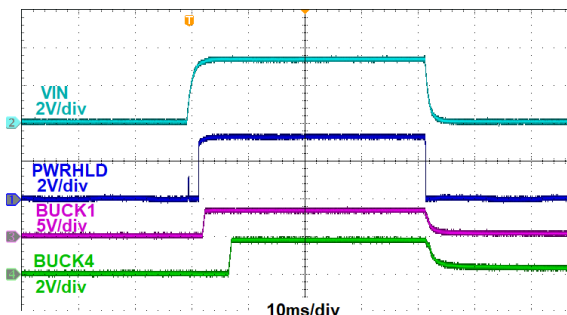


FIGURE 22: Discrete 3.3V Input Voltage Monitor Circuit Step Response.

Even with fast input supply rise times, the delay is adequate to ensure that the PWRHLD low-to-high transition happens after the PMIC has completed its boot process and therefore can be recognized as a valid start-up event. The delay is adjustable through R4 and C1.

When the input voltage ramps up slowly, the circuit is able to generate a proper start-up event according to the programmed static threshold value, which in any case must be higher than the UVLO threshold of the PMIC (Figure 23).

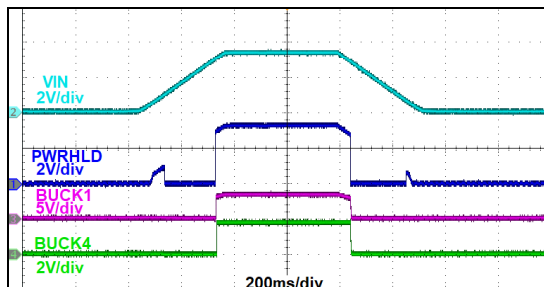


FIGURE 23: Slow Rising 3.3V Input Voltage Response Using Discrete Circuit.

The 5% decreasing VIN step response shows a similar result to the other voltage monitoring circuits, generating proper shutdown and start-up events (Figure 24).

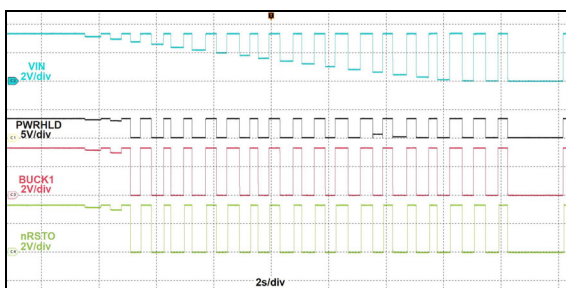


FIGURE 24: Decreasing 3.3V Input Voltage Step Response.

2.7 Discrete Input Voltage Monitoring for 5V Main Supply Systems

For 5V nominal systems and when a discrete circuit is desired, the following variation of the previous circuit can be used, where the nominal trip threshold (rising) is set to approximately 4.5V (Figure 25).

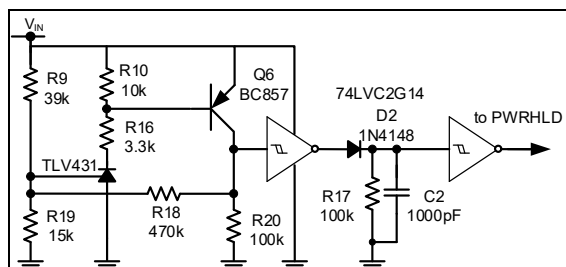


FIGURE 25: Discrete 5V Input Voltage Monitor Schematic.

The working principle is the same as the 3.3V nominal input voltage monitor schematic, but with different R9 and R18 resistor values for trip threshold and hysteresis settings.

This design has also a fast response time to a rising input voltage step, yet ensures a proper start-up event (Figure 26).

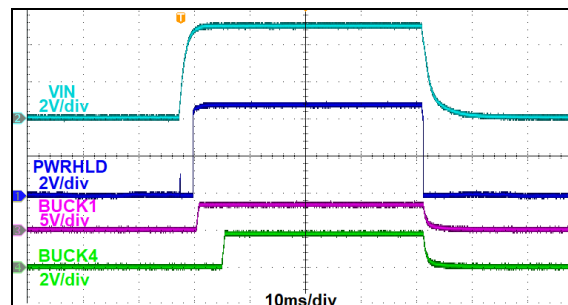


FIGURE 26: Discrete 5V Input Voltage Monitor Circuit Step Response.

Since the trip threshold is much higher than the typical UVLO threshold of the MCP16501/2, the behavior of the circuit is relatively insensitive to variations of the trip threshold set voltage. Therefore, as long as the variation of the trip threshold value is not a big concern, 5% resistors can be used with a suitable choice of nominal trip threshold (Figure 27).

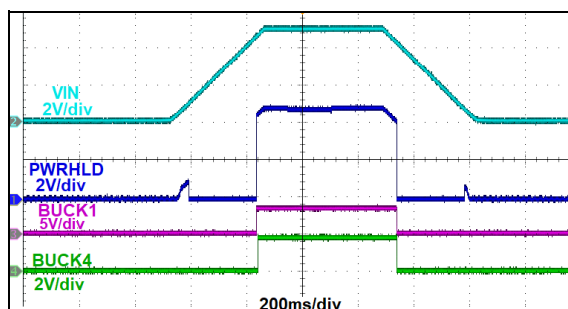


FIGURE 27: Slow-Rising 5V Input Voltage Response Using Discrete Circuit.

The 5% decreasing input voltage also shows a proper response, not triggering for the first 2 steps (~4.75V and ~4.5V) but generating restarts for steps lower than 4.2V (Figure 28).

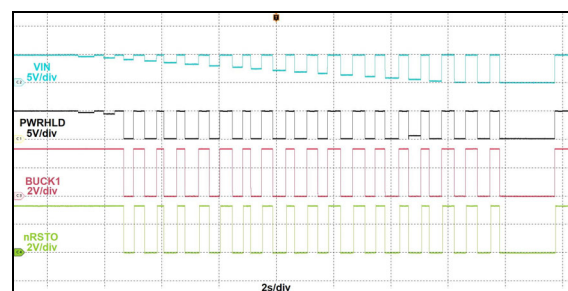


FIGURE 28: Decreasing 5V Input Voltage Step Response.

Table 1 summarizes the solutions for the input voltage monitoring circuits. It shows both the advantages/disadvantages, and provides a quick comparison between them.

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TABLE 1: INPUT MONITORING SOLUTIONS COMPARISON

	Automotive	BOM Cost	Complexity	Board space	Current Iq	Customizability
MIC803	No	Very Low	Low	Low	4.49µA@3.3V	Low
MIC102	Yes	Low	Low	Low	0.5µA @3.3V	Low
MIC841	No	Medium	Medium	Medium	5µA @3.3V	Medium
Discrete	Yes	Very Low	High	High	0.5mA@3.3V 1.4mA@5V	High

3.0 REDUCING BOM COST IN APPLICATIONS WITH VIN=3.3V

There may be cases where MCP16501/2 is used in a regulated 3.3V nominal input voltage application and the functionality of Buck1 (that is usually set to 3.3V) is not needed. While it is possible to generate customized part numbers that eliminate Buck1 (or any other power channel) from the start-up sequence, this process requires involvement of the factory and may not be as fast as the customer development schedule would permit.

Note: Contact your local Microchip Sales Office if such a custom solution is required.

In this case, a very simple and inexpensive work-around can be implemented such that Buck1 can still be depopulated without compromising the start-up sequence and proper reset (nRSTO) generation. Also note that the method can be extended to any other Buck channel.

This can be achieved, when not using Buck1, by connecting OUT1 pin to VIN while not populating the passive components associated with Buck1. The underlying idea is to bypass the Start-up POK Bypass Threshold (see the data sheets for [MCP16501](#) and [MCP16502](#)) by connecting OUT1 to a voltage equal to (or slightly below) the PVIN1 voltage (equal to VIN), such that the internal start-up engine acts as if the voltage at OUT1 was correctly established by virtue of the Buck converter action.

In normal operation, there is no additional current consumption from VIN, except for the very small current absorbed by the internal feedback network connected to OUT1. For MCP16501/2, the feedback divider impedance is typically in the 1.5M Ω range and therefore it draws negligible current.

However, when shut down, the automatic discharge function connects a 25 Ω resistor (typical) from OUT1 to GND, greatly increasing the shutdown current. To get around this issue, a simple pull-up resistor of 100k Ω can be used ([Figure 29](#)), connecting OUT1 to VIN with negligible voltage drop when the automatic discharge switch is OFF while limiting the extra current consumption to a low level when the switch is ON ([Figure 30](#)). In this case, the additional current when the regulator is OFF is only of about 33 μ A.

Also note that for MCP16502, the discharge switch can be disabled through the I²C command by clearing the respective DISCH bit, such that the additional current consumption when the channel is disabled can be permanently eliminated (as long as the SVIN supply voltage remains above the UVLO threshold and the registers' configuration is retained).

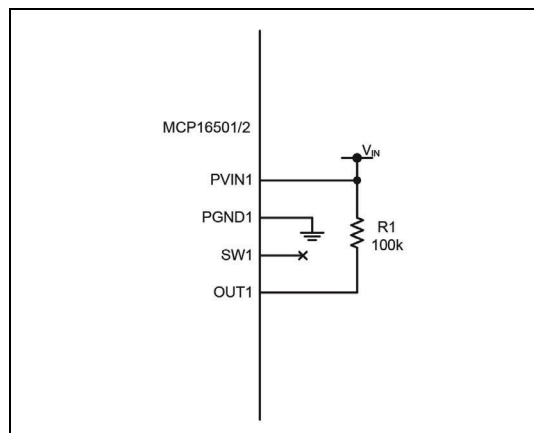


FIGURE 29: Depopulated Buck1 Schematic.

Note: PGND1 and PVIN1 should still be connected to the board Power GND and to the input supply respectively, like in normal operation.

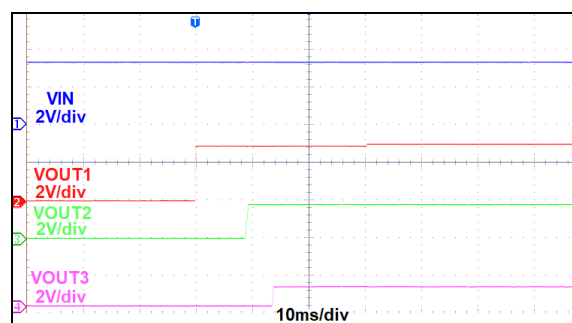


FIGURE 30: Depopulated Buck1 Start-Up With 100k Pull-up On OUT1.

It is recommended that a maximum of 100 k Ω resistor is used (based on [Equation 1](#)). Because the internal resistor network divider as well as other internal circuitry are connected to the OUT1 pin, there must be a small current flowing into OUT1, to GND. A greater value of pull-up resistor could cause the OUT1 pin voltage to not go high enough, a start-up error to be generated and the start-up sequence to not complete.

[Equation 1](#) shown below establishes the limit value for R1, which should not be exceeded under any conditions.

EQUATION 1: R1 LIMIT VALUE

$$R1_{limit} = \frac{R_{fdbk}}{\left(\frac{V_{VIN}}{V_{POKB_TH_B1}} - 1\right)}$$

Where:

- V_{VIN} is the input voltage, applied to PVIN1;
- R_{fdbk} is the value of the internal feedback resistor, typically 1.5MΩ. This is an internal resistor, whose absolute value subject to process variations and therefore a +/-30% tolerance should be considered for a safe design margin;
- $V_{POKB_TH_B1}$ is the so-called Start-up POK Bypass Threshold as given in the EC Table (see the data sheets for [MCP16501](#) and [SAMA5D27 Wireless SOM1](#)).

In conclusion, assuming that the maximum value that VIN can take for Buck1 when depopulated is 3.6V, we obtain in a worst-case scenario, [Equation 2](#).

EQUATION 2: R1 LIMIT CALCULATION EXAMPLE

$$R1_{limit} = \frac{1.5M\Omega \times 0.7}{\left(\frac{3.6V}{360mV} - 1\right)} = 116.7k\Omega$$

Where

- 360mV is the minimum value of $V_{POK_B_TH_B1}$ given in the EC Table.

Using 100 kΩ provides an additional safety margin.

A similar procedure can be carried out for the other Buck channels, keeping in mind that the threshold to be considered is POK_THx which is relative to the target voltage the Buck channel should be generating. Since MCP16502 options where one Buck channel is not activated during the start-up sequence are already available (for example, the "AA" and "AE" options), this is considered a very unlikely use case.

4.0 BUCK1 CHANNEL IN NONINVERTING BUCK-BOOST CONFIGURATION

In today's market there are many applications where the output voltage must be regulated even if the input voltage varies within a range in which it can be higher or lower than the output voltage. In automotive, Internet of Things (IoT) and other similar applications, it can be necessary to step-down and step-up the input voltage as needed requiring a Buck-Boost converter configuration. While there are several dedicated, efficiency-optimized noninverting Buck-Boost solutions in the market, in some situations it may be acceptable to configure a Buck channel (namely, Buck1) to support a noninverting Buck-Boost topology.

Buck1 channel of the MCP16501/2 can be set in a noninverting Buck-Boost configuration as shown in Figure 31.

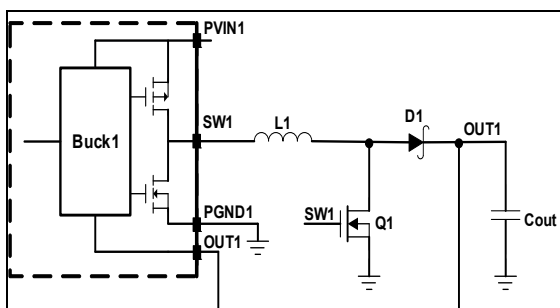


FIGURE 31: Buck1 Channel in a Noninverting Buck-Boost Topology.

To configure the Buck1 channel in a noninverting Buck-Boost topology, two external components need to be added to the circuit: a diode connected between the inductor and the output, and a N-channel MOSFET connected from the anode of the diode to ground, controlled by the switching signal SW1 (such that it runs in phase with the internal high-side switch). This technique is well-known [2] and while it is less efficient than a separate dedicated noninverting Buck-Boost solution where the switching of the power switches is optimized according to the input/output operating conditions, it is cost-competitive and comes with little board space penalty.

By taking power losses into consideration, a more realistic conversion ratio of the Buck-Boost converter $V_{out}/V_{in}(D)$ can be seen in Figure 32 [3]. The conversion ratio depends (in addition to the duty cycle) on the ON resistance of the switches, the DC resistance of the inductor and the voltage drop on the diode. In the lower range of the duty cycle those losses are quite small, but as the duty cycles increases those components become significantly larger in relation to D . This creates a critical duty cycle (D_{crit}) after which the power losses increases while the output voltage

decreases. When D_{crit} is exceeded, MCP16501/2 increases the duty cycle to compensate for the output voltage drop, further decreasing the output voltage.

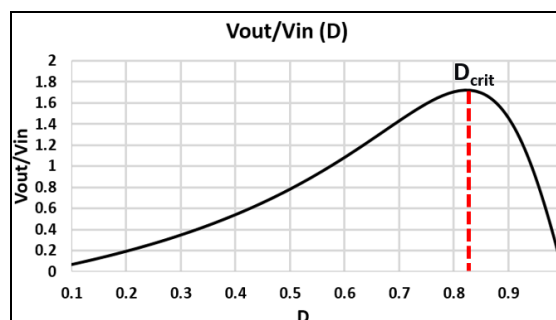


FIGURE 32: $V_{out}/V_{in}(D)$ Conversion Ratio.

From the shape of the conversion ratio, it is apparent that some mechanism is needed to prevent the duty cycle from reaching values where the slope is negative. If this ever occurs, an increase of the duty cycle causes the output voltage to decrease, which in turn causes a further increase in the duty cycle. At this point, the regulation loop changes from negative to positive feedback beyond the peak of the conversion ratio. If the control commands a duty cycle (for any reason) beyond the critical peak (at $D=D_{crit}$), it will quickly push the duty cycle to the maximum limit.

MCP16501/2 buck channels are 100% duty cycle capable, therefore without any other safety mechanisms, the maximum D equals 1, keeping closed Q1 and the internal high-side switch which shorts the input of the converter. However, it can be shown that the peak current limit of the MCP16501/2 prevents this critical behavior, and thus limits the duty cycle to a value smaller than the D_{crit} . In case of a short overload condition, the duty-cycle is limited as a direct consequence of the inductor current reaching the current limit as shown in Figure 33.

The output voltage does not collapse to zero and once the overload condition is removed, the voltage goes back to 3.3V.

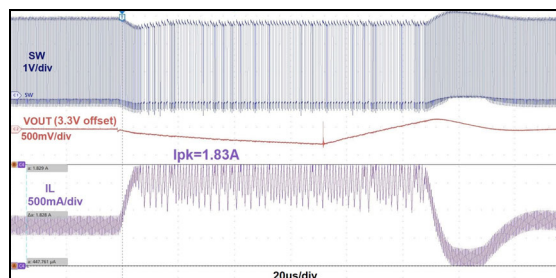


FIGURE 33: Overload and Recovery.

This critical duty cycle is highly dependent on the specifications of the external components, and therefore they must be chosen carefully. The average

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current flowing through inductor and switches in a Buck-Boost converter ($I_{IN}+I_{OUT}$) is higher than in a buck or a boost converter, which results in higher conduction losses.

4.1 Detailed Circuit Implementation

The detailed circuit implementation of the concept configuration shown in Figure 34 and the BOM is provided in Table 2.

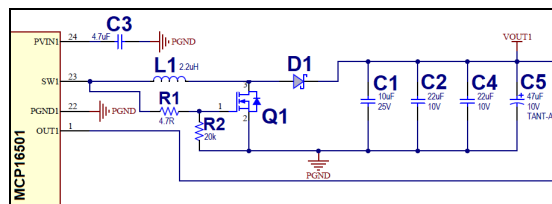


FIGURE 34: MCP16501 Buck1 Channel in Buck-Boost Configuration Schematic.

TABLE 2: MCP16501 BUCK1 CHANNEL BOM

Item	Part Number	Description
C1	C1608X5R1E106M080AC	Capacitor, 10uF, 25V, 20%, X5R, 0603
C2, C4	C2012X7S1A226M125AC	Capacitor, 22uF, 10V, 20%, X7S, 0805
C3	C1608X7S1A475K080AC	Capacitor, 4.7uF, 10V, 10%, X7S, 0603
C5	TLJA476M010R0600	Capacitor, 47uF, 10V, 20%, TANT A
L1	74404043022A	Inductor, 2.2uH, 2.28A, 30%, 4mm x 4mm
D1	PMEG2010AEH	Diode Schottky, 430mV, 1A, 20V, SOD-123F
Q1	IRLML2502	Transistor N-channel, 20V, 4.2A, SOT-23
R1	MCMR04X4R7	Resistor, generic 4.7 Ohm, 5%, 0402
R2	MCMR04X203	Resistor, generic 20 kOhm, 5%, 0402

4.2 Experimental Results

The following experimental results are derived by implementing a noninverting Buck-Boost topology for the Buck1 channel of the MCP16501 using the circuit described in Section 4.1, Detailed Circuit Implementation. The efficiency of the converter is affected by the forward diode voltage, the ON resistance of the external transistor and the DCR of the inductor. Figure 35 shows the efficiency of the proposed implementation for different input voltages.

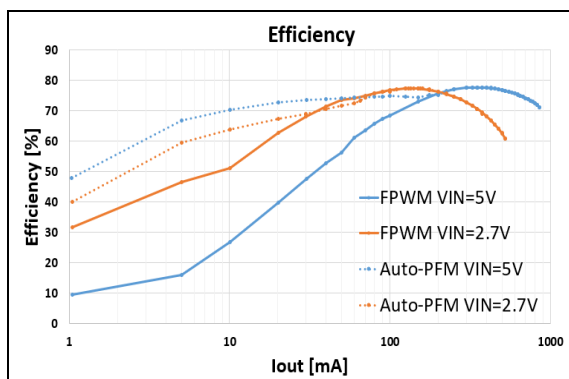


FIGURE 35: MCP16501 Buck1 (3.3V) Channel Efficiency.

The average current flowing through inductor and switches ($I_{IN}+I_{OUT}$) is higher than in a buck converter, which causes a reduction of the output current capability with respect to the Buck configuration as shown in Figure 36.

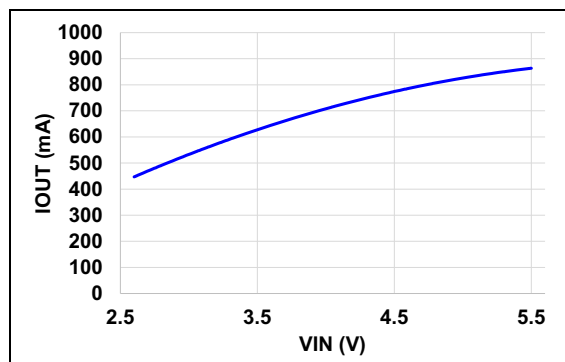


FIGURE 36: Output Current Capability vs Input Voltage (typical curve).

Figure 37 show the output voltage of the Buck-Boost when the input voltage is stepped from 2.6V to 5.5V.

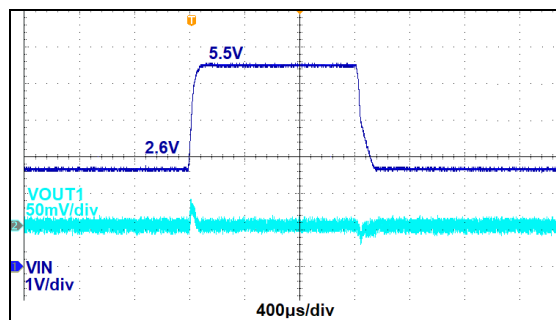


FIGURE 37: Line Step from 2.6V to 5.5V @0.13A Load.

Figure 38 and Figure 39 show the Load step response achieved when the load current is stepped from 25 mA to 460 mA (Figure 38) and from 25 mA to 700 mA (Figure 39), both with $V_{out}=3.3V$, AC coupled in the scope shots.

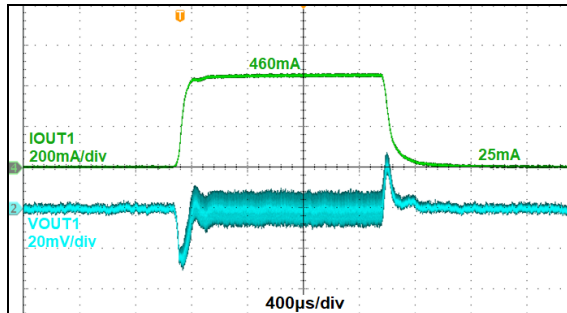


FIGURE 38: Load Step (2.6V input).

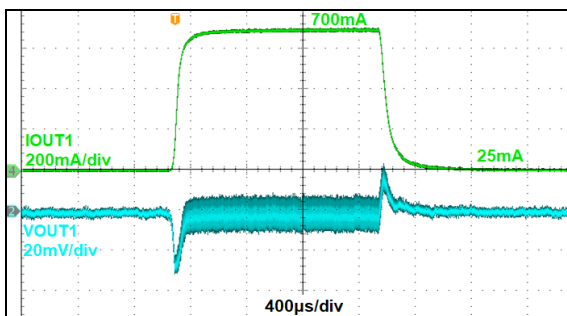


FIGURE 39: Load Step (5.5V input).

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www.iso.org/standard/61280.html

[2] MCP16301. *High Voltage Buck-Boost Demo Board User's Guide*. DS52020A. © 2012 Microchip Technology Inc.

[3] M. Kazimierczuk, *Pulse-Width Modulated DC-DC Power Converters*, pages 151-153 - Wiley, 2008.

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