

Saving Power with Atmel PLDs

Introduction

Many designers today are looking for ways to reduce power consumption in their designs to meet expanding market demands for portable and battery-operated products. With the push to add more features to these products while maintaining the same board size and power budget, Programmable Logic Devices with the low power consumption are playing a larger role in the design of these products. These devices allow the designer to add more features in the same board space, yet be able to maintain or decrease the overall power consumption of the system. Atmel offers a variety of PLDs, in several density classes with pin counts ranging from 20 to 160 pins, that lower power consumption significantly by Atmel's proprietary Input Transition Detection (ITD) technology. ITD capable PLDs are indicated by a "L" or "Z" in the suffix of the part name.

Power Consumption for PLDs

Before discussing the detailed features of Atmel's Low-power PLDs, it is important to point out the two components for PLD power consumption.

1. $P_{\text{average}} = nC_{\text{Load}} F_{\text{op}} (V_{\text{supply}})^2$
2. $P_{\text{standby}} = I_{\text{CC,SB}} \times V_{\text{supply}} =$
Standby Power when the device is powered down

Where:

P_{average} = average power consumed while outputs are switching

C_{load} = load capacitance on each output pin

n = number of output pins switching

F_{op} = Frequency of operation

V_{supply} = supply voltage.

As shown in equation 1, a designer may be able to reduce the overall power consumption of his or her design by reducing the supply voltage, pin capacitive loading, or operating frequency. However, these alternatives are usually not practical. Another alternative a designer can choose, as equation 2 shows, is to use parts that consume as little standby power as possible during idle periods when the device is not responding to input stimulus. Atmel's Low-power PLDs are ideally suited for this purpose.

Power Consumption Savings with Atmel ITD PLDs

Atmel Low- or Zero-power PLDs include an input transition detection (ITD) feature, indicated by the "L" or "Z" in the part number suffix. These PLDs save power by automatically powering down to a "standby" or "sleep" mode when no signal transitions occur on the inputs or internal feedback nodes of the device. When an input signal transition next occurs, the ITD feature "wakes up" the device returning it to the active mode. Figure 1 shows the Average I_{CC} vs. Frequency characteristics for Atmel's standard and low-power PLDs. For frequencies less than F_{active} , a low-power device will automatically go through active and standby cycles to reduce the average current consumption. Compared with a standard power device, which always remains active, low-power PLDs offer significant power savings. As the input signal frequency increases, the percentage of time a low-power device is active will also increase proportionally until F_{active} is approached. For frequencies greater than or equal to F_{active} , a low-power device will consume about the same amount of current as a standard-power device.



Erasable Programmable Logic Device

Application Note



Standby Mode

When a low-power device is in the standby mode, the internal fuse array powers-down and the device draws standby current, $I_{CC,SB}$ from the system's supply. The device will enter the "standby" mode automatically when no inputs or internal feedbacks have switched within a time period of T_{active} .

Equation 3 shows how to calculate T_{active} for a ATF16V8BQL PLD device.

$$3. T_{active} = 1/(2 \times F_{active})$$

Where:

T_{active} = Active time period

F_{active} = Cutoff Frequency

For example, on the ATF16V8BQL,

$I_{active} = 35 \text{ mA}$, $F_{active} = 40 \text{ MHz}$, and $I_{CC,SB} = 5 \text{ mA}$.

So, $T_{active} = 1/(2 \times 40 \text{ MHz}) = 12.5 \text{ nsec}$.

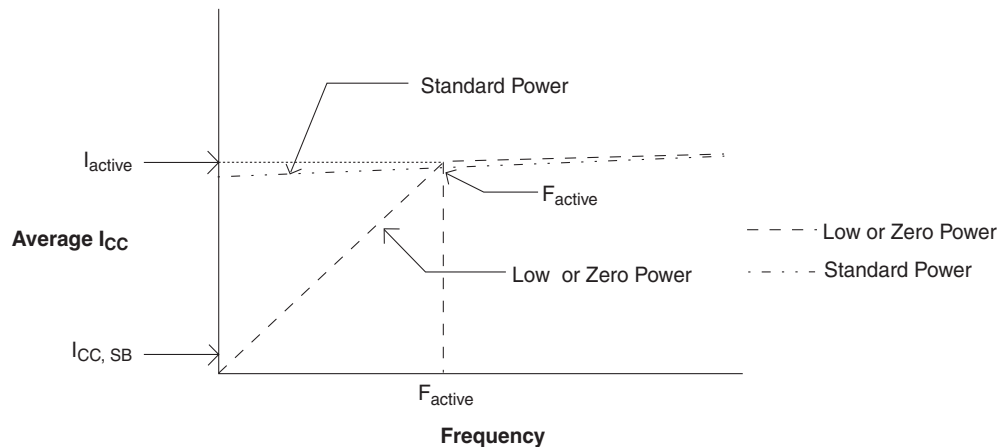
Therefore, if no inputs or feedbacks have switched for 12.5 ns, the ATF16V8BQL will power down to the standby mode and only draw 5 mA from the supply.

During the standby mode, all logic signals are latched so all outputs and internal feedbacks will remain valid. Since the device powers down to this mode automatically, no separate power-down pin is required.

The Active Mode

An Atmel Low-power PLD automatically wakes up to the active mode when it senses an input change from either low-to-high or high-to-low. When waking up, the internal fuse array is powered up and transient current increases from $I_{CC,SB}$ to a peak value of I_{active} . The current remains at the peak value while the device is awake. The time required for the device to change current from $I_{CC,SB}$ to I_{active} during wake-up or vice versa during power down is called the "wake-up" time or T_{wake} . The wake-up time is already included within the Propagation Delay (T_{pd}) specification in the Atmel datasheet. On average, the wake-up time ranges from 3 to 5 ns for most of the Atmel devices. Figure 2 shows what happens while the device is awake. In Figure 2(i), the device awoke by a single input transition and saw no additional transitions. Hence, the device will stay awake for T_{active} before entering the standby mode. In Figure 2(ii), the device sees several input transitions after the first transition that woke the device up. Therefore, it will stay awake for T_{active} after the *last* input transition occurs before powering down.

Figure 1. Average I_{CC} vs. Frequency for Atmel Standard and Low-power Devices



Where: $I_{CC,SB} = I_{CC}$ in standby mode
 $I_{active} = I_{CC}$ at cutoff frequency
 F_{op} = Frequency of operation
 F_{active} = Cutoff frequency

The slopes on Figure 2 show the transient current slew rate required for an Atmel Low-power device to change current from $I_{CC,SB}$ to I_{active} during the wake-up time for both the wake-up and power-down process. This slew rate can be calculated by equation 4 below:

$$4. \quad I_{CC} \text{ Slew Rate during wake up} = \frac{dI}{dt} = \frac{I_{active} - I_{CC,SB}}{T_{wake}}$$

$$\text{during power down} = \frac{dI}{dt} = \frac{I_{active} - I_{CC,SB}}{T_{wake}}$$

For example, for a ATF16V8BQL device,

$$I_{active} = 35 \text{ mA}, I_{CC,SB} = 5 \text{ mA}, \text{ and } T_{wake} = 3 \text{ ns}$$

Therefore, during wake up,

$$dI/dt = (35 \text{ mA} - 5 \text{ mA})/(3 \text{ ns}) = 10 \text{ mA/ns.}$$

During power-down the slew rate is negative or -10 mA/ns.

Average I_{CC} vs. Peak I_{CC}

The total current required for a low-power device to complete an active cycle is the sum of transient and peak currents. Since the transient current cancels during the wake-up and power-down portions of the active cycle, its total contribution is zero. Therefore, the total current required is the peak current.

The average current required by the device when operating at a particular operating frequency can be approximately related to the peak current in the active cycle by:

$$5. \quad \text{For } F_{op} = 0 \quad \text{Average } I_{CC} = I_{CC,SB}$$

$$\text{For } F_{op} < F_{active} \quad \text{Average } I_{CC} \sim [F_{op}/F_{active}] \times I_{peak} + [1 - (F_{op}/F_{active})] \times I_{CC,SB}$$

$$\text{For } F_{op} \geq F_{active} \quad \text{Average } I_{CC} \sim I_{active},$$

Where:

F_{op} = Frequency of Operation

$I_{peak} = I_{active}$ = Peak Current or current at the cutoff frequency

F_{active} = Cutoff frequency

For example, with an ATF22V10BQL device,

For $F_{op} = 10 \text{ MHz}$; $F_{active} = 20 \text{ MHz}$,

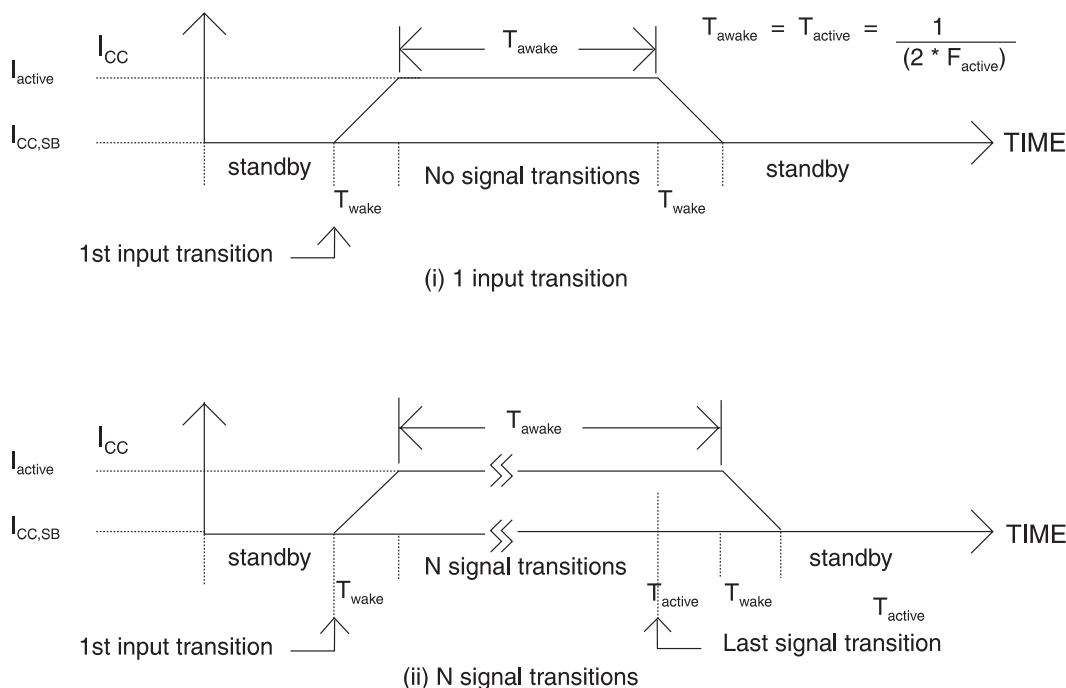
$I_{peak} = I_{active} = 45 \text{ mA}$, and $I_{CC,SB} = 8 \text{ mA}$.

F_{active} , I_{peak} , and $I_{CC,SB}$ are determined from the I_{CC} vs. Frequency curves in the data book,

$$\text{Average } I_{CC} \sim (10 \text{ MHz}/20 \text{ MHz}) \times (45 \text{ mA}) + (1 - (10 \text{ MHz}/20 \text{ MHz})) \times 8 \text{ mA} = 26.5 \text{ mA.}$$

Therefore, at an operating frequency of 10 MHz, the average current drawn by a ATF22V10BQL device should be about 26.5 mA.

Figure 2. Active Cycle



Supplying Transient and Peak Currents

In many applications with limited power sources, such as battery supplied or portable systems, the transient and peak currents required by the active cycle can be generated by the existing decoupling capacitors on the board. Decoupling capacitors act as a temporary power source to the PLD's supply, supplying a low-power device with the necessary amount of current so it can undergo active cycles automatically to save power.

To calculate the minimum decoupling capacitance needed, we first need to compute the total amount of charge required during an active cycle and use this amount to derive the capacitance. The total charge needed is:

$$6. \quad Q_{\text{total}} = Q_{\text{active}} + Q_{\text{transient}}$$

$I_{\text{transient}}$ cancels during the active mode so $I_{\text{transient}} = 0$. Therefore, $Q_{\text{transient}} = 0$ as well. Substituting this result into equation 6 gives,

$$7. \quad Q_{\text{total}} = Q_{\text{active}} = (I_{\text{active}}) \times [1/(2 \times F_{\text{active}})]$$

The decoupling capacitance required can then be calculated as Q_{total}/dV and is:

$$8. \quad C_{\text{req}} = \frac{I_{\text{active}} \times [1/(2 \times F_{\text{active}})]}{dV}$$

Where dV is the maximum droop allowed in the supply voltage caused by draining this charge from the capacitors.

For example, with a ATF16V8BQL device:

Assume $dV = 100 \text{ mV}$ maximum, $I_{\text{active}} = 35 \text{ mA}$, and $T_{\text{active}} = 12.5 \text{ ns}$.

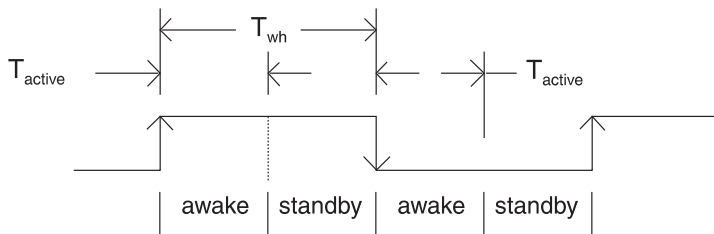
Therefore, $Q_{\text{active}} = (35 \text{ mA}) \times (12 \text{ ns}) = 0.42 \text{ nC}$ and $C_{\text{req}} = (0.42 \text{ nC})/(100 \text{ mV}) = 4.2 \text{ nF}$.

This is the minimum decoupling capacitance needed to supply the peak and transient currents required for the active time period, in this case 12.5 ns.

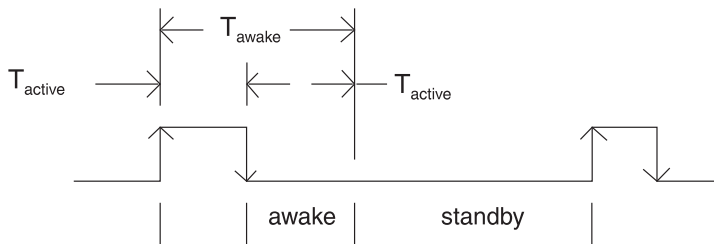
How Duty Cycle Affects Power Consumption

A low-power device normally wakes up twice for each clock input cycle. For example, with a 50% duty cycle input (Case 1, Figure 3), the device wakes up on the rising edge and falling edges of the input. If the input signal width, T_{wh} , is less than or equal to T_{active} , as shown in Case 2 Figure 3, the device will wake up once during each input cycle. From Case 2 Figure 3, we see that the input duty cycle affects the power consumption of a low-power device by reducing the time it is awake. If the input duty cycle is greater than 50%, the device will consume the same power as in Case 2 Figure 3.

Figure 3. Awake Time vs. Input Duty Cycle



(i) 50% Duty Cycle



(ii) < 50% Duty Cycle

CASE 1

$$T_{\text{wh}} \Rightarrow T_{\text{active}}$$

$$T_{\text{awake}} = 2 \times T_{\text{active}}$$

2 "Wake-up" cycles per second

CASE 2

$$T_{\text{active}} > T_{\text{wh}} \Rightarrow T_w$$

$$T_{\text{awake}} = T_{\text{wh}} + T_{\text{active}}$$

1 "Wake-up" cycle per second

T_w = Minimum input width (specified in the Atmel datasheet)

Design Guidelines for “L/Z” Devices

The “L/Z” devices offer many benefits that allow you to save power in your design. To derive the greatest benefit from these features Atmel recommends that you follow the guidelines below:

1. **Decoupling Capacitor** – As discussed in the previous section on “Supplying Transient and Peak Currents” for “L/Z” devices. When an “L/Z” device wakes up after detecting an input transition, it draws the same current as a standard-power part for a limited time period (T_{awake}). The time it takes the “L/Z” device to wake-up is quite small, typically 3 to 5 ns for most of the Atmel devices. Because so much current is required for such a small time period, a large transient occurs on the power supply. In practice this is more than most supplies can handle. Therefore, Atmel recommends that a 0.22 μF or greater ceramic or tantalum decoupling capacitor be placed as close to the supply pin(s) of an “L/Z” device as possible.
2. **Unused Inputs and I/O Pins** – If you are designing with an “L/Z” device and have any unused Inputs or I/O's in your design, Atmel recommends that you either pull them up or enable the pin-keeper option (if available) on the part. Floating Inputs or unused I/O pins create a high impedance path for noise to couple within the device. This, in turn, may create noise on the device's outputs. Atmel has made additions to its PLD product family to eliminate this requirement. Some devices (ATF16V8/20V8/22V10B) have internal pull-up resistors on all inputs and I/O pins. Other devices (ATF1500AS Family) have weak latches, pin-keeper circuits, that hold inputs and I/O pins to a stable logic state within the device. Older Atmel PLD devices (ATV series devices) do not have these features above, so this recommendation still applies.
3. **Running at Higher Clock/ Input Transition Frequencies** – Low-power devices offer maximum power savings at lower clock frequencies as shown on the I_{CC} vs. Frequency curve in Figure 1. Atmel recommends that you use Standard power instead of an “L/Z” device if your design has either inputs, feedbacks or clocks that transition (high/low) at a time period close to the T_{awake} time. Standard-power devices consume equivalent power as “L/Z” devices when operating close to F_{active} and do not require special design guidelines described herein. The value for T_{awake} is defined in Figure 2 above. F_{active} is determined in the Atmel datasheet for the device.

4. **Input Setup Time** – When using “L/Z” devices for registered or mixed logic applications make sure that all inputs and feedback meet the Input Setup Time requirements specified in the Atmel datasheet. Violating this setup time may cause registered outputs to become either metastable or incorrectly clock data. This could affect how the device functions in your system.

Atmel PLD Product Selections

In addition to standard and low-power PLDs, Atmel also offers Quarter Power and Low Voltage products. These versions are also available with the ITD feature. Figure 4 shows the Average I_{CC} vs. Frequency characteristics for all Atmel PLDs.

Atmel Standard-power and Low-power PLDs

Atmel standard-power PLDs are high performance devices whose power consumption remains about the same with frequency. Low-power products approach standard-power PLD power consumption at higher frequencies but save power at lower frequencies and when the device is idle.

Quarter Power PLDs

Atmel Quarter Power PLDs are available in two versions, a standard-power Quarter Power part (“Q” suffix) and a Quarter Power device, which has the ITD feature (“QL” suffix). Both versions have approximately one half the average I_{CC} of a standard-power PLD and consume a quarter of the power of a comparable Bipolar part. The “QL” devices have the Quarter Power active current, plus the ITD feature.

Atmel Low-voltage PLDs

Atmel 3.3V PLDs include the letters “LV” in the device name or “V”, “LV” or “BV” in the suffix. These devices save power compared to standard-power 5V PLDs, because they operate at lower voltage.

Atmel Low-voltage PLDs are capable of operation down to the reset level, V_{RST} , which is generally just below the specified minimum power supply voltage. The ATF150XASV Series of low-voltage devices has two options for the hysteresis about the reset level: Small and Large. To ensure a robust operating environment in applications where the device is operated near Minimum V_{CC} , Atmel recommends that during the fitting process users configure the device with the Power-up Reset Hysteresis set to Large. When the Large hysteresis option is active, I_{CC} is reduced by several hundred microamps as well.

As with other Atmel PLDs, low-voltage parts are also available with the ITD (automatic standby) feature. If the user wants to control the power-down process, separate dedicated power-down pin(s) are available on some Atmel PLDs.

Zero-power PLDs

Zero-power PLDs have the same features as low-power devices except that they power down to a standby state where the I_{CC} is in the μA range.

Summary

We have discussed the features of Atmel's Low-power PLD products and have seen that these devices can offer the system designer many benefits for applications where power consumption is a critical requirement. These benefits include:

ITD Feature in ALL PLD and CPLD Products

Designers can use any Atmel PLD or CPLD product, from 20 up to 160 pins, and still take advantage of the low-power or zero-power feature.

High-performance AND Power Consumption Savings

Designers can save power in their designs yet not sacrifice overall system operation speed. There is *no* separate delay for the ITD feature. All delays are included in the T_{pd} specification in the Atmel data sheet.

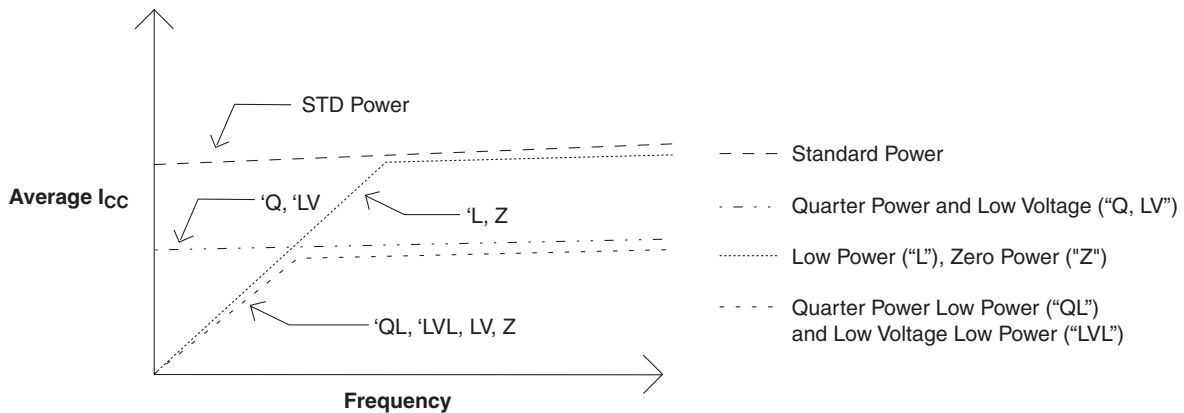
Separate or Automatic Power-down Option

Atmel's patented ITD feature automatically powers down the device to a low-power mode when no inputs or internal feedbacks are switching. Therefore, no separate power-down pin is needed, since power-down is automatic.

Increased System Reliability

Atmel Low-power parts consume less power, and operate cooler. So thermal related issues are less of a concern in the overall system design.

Figure 4. Average I_{CC} vs. Frequency for all Atmel PLDs





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