USB5926C

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB5926C. These checklist items should be followed when utilizing the USB5926C in a new design. A summary of these items is provided in Section 10.0, "Hardware Checklist Summary," on page 27. Detailed information on these subjects can be found in the corresponding section:

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The USB5926C implementor should have the following documents on hand:

- *USB5926C Data Sheet*
- *AN1700 - FlexConnect Applications*
- *AN1997 - USB-to-GPIO Bridging with Microchip USB3.1 Gen 1 Hubs*
- *AN1998 - USB to I2C Bridging with Microchip USB 3.1 Gen 1 Hubs*
- *AN2316 - Configuration Options for the USB58xx and USB59xx Application Note*
- *AN4027 - USB58xx and USB59xx FlexConnect Operation*

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.4 USB-IF Compliant USB Connectors

- USB-IF certified USB Connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass the USB-IF product certification.

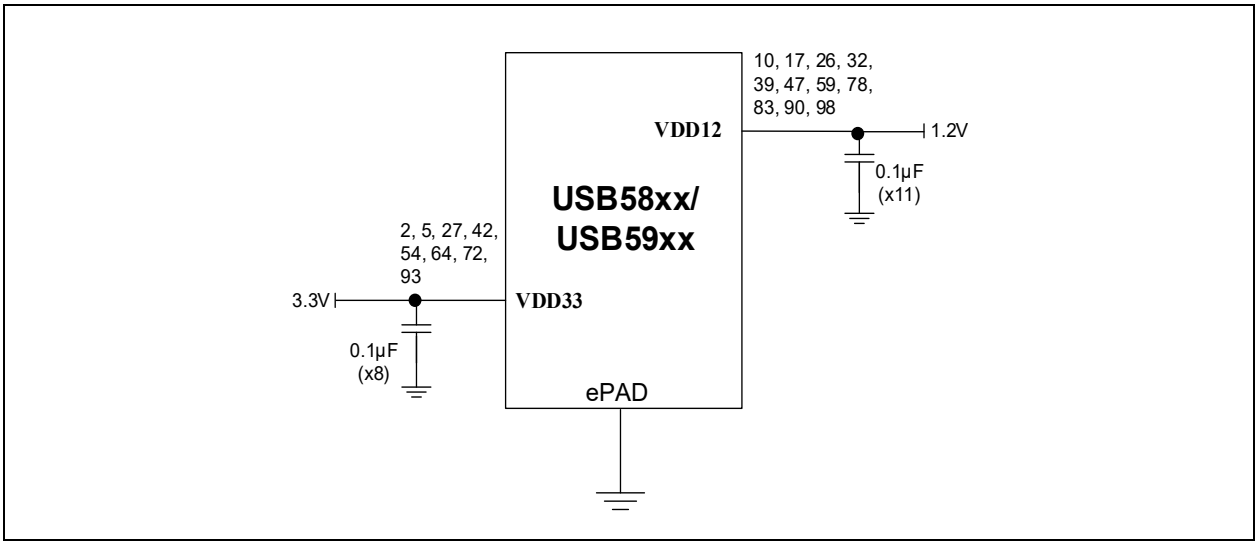
3.0 POWER

3.1 Power and Bypass Capacitance

- The analog supplies (**VDD33**) are located on pins 2, 5, 27, 42, 54, 64, 72, and 93, and require a connection to a regulated 3.3V power plane.
- The **VDD33** pins each should include 0.1 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The analog supplies (**VDD12**) are located on pins 10, 17, 26, 32, 39, 47, 59, 78, 83, 90, and 98, and require a connection to a regulated 1.2V power plane.
- The **VDD12** pins each should include 0.1 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



4.0 USB SIGNALS

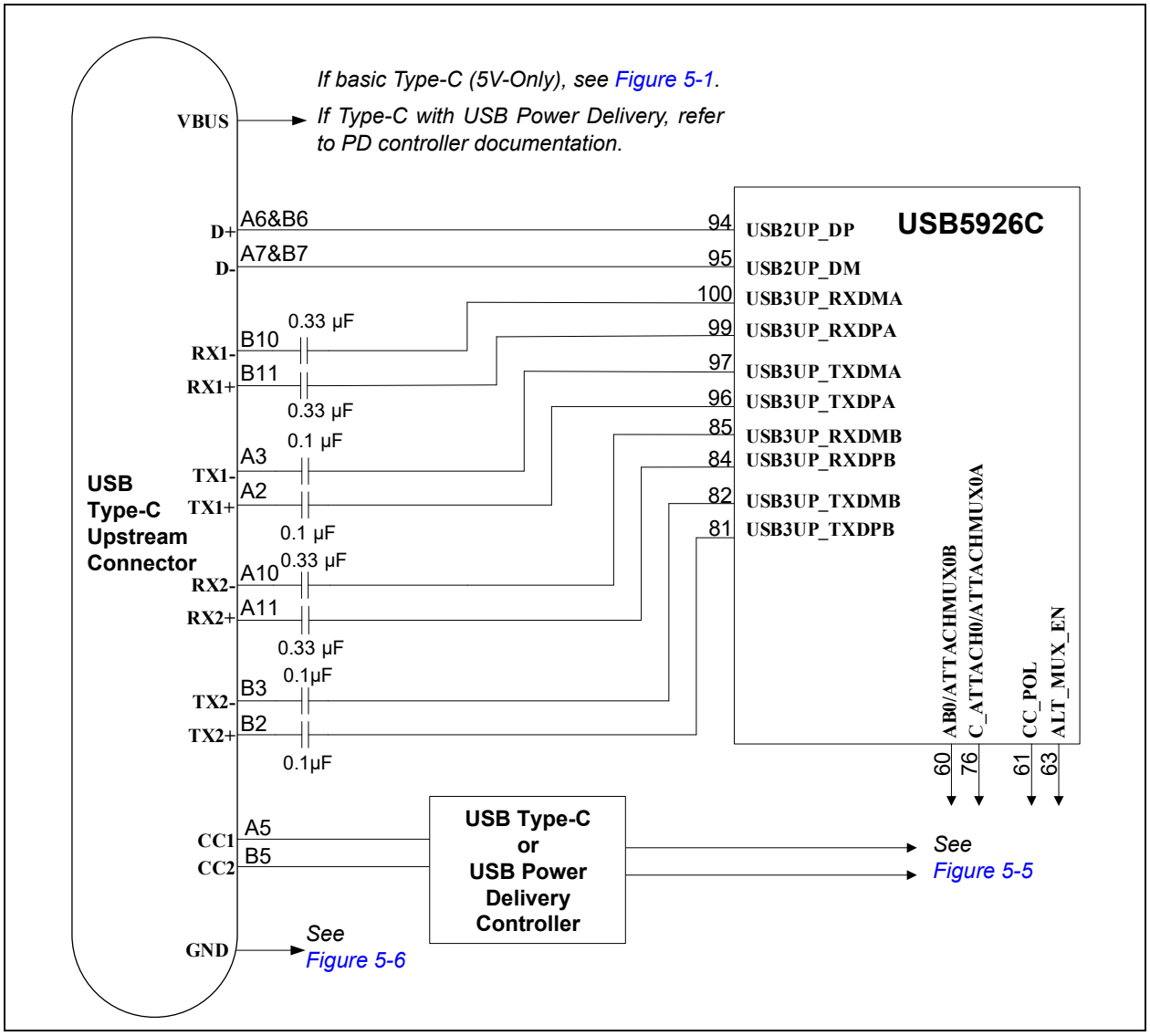
4.1 Upstream Port USB Signals

- **USB2UP_DP** (pin 94): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the D+/DP[1] pin of a USB Connector.
- **USB2UP_DM** (pin 95): This pin is the negative (-) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the D-/DM[1] pin of a USB Connector.
- **USB3UP_TXDPA** (pin 96): This pin is the positive (+) signal of the upstream USB3.1 TX1+ transmitter (TX) differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX-)[2] pin of the USB Connector.
- **USB3UP_TXDMA** (pin 97): This pin is the negative (-) signal of the upstream USB3.1 TX1- TX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX- (or TX+)[2] pin of the USB Connector.
- **USB3UP_RXDPA** (pin 99): This pin is the positive (+) signal of the upstream USB3.1 RX1+ receiver (RX) differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX+ (or RX-)[2] pin of the USB Connector. According to the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, this pin is highly recommended to have a series 0.33 µF decoupling (DC blocking) capacitor before connecting to the USB connector.
- **USB3UP_RXDMA** (pin 100): This pin is the negative (-) signal of the upstream USB3.1 RX1- RX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX- (or RX+)[2] pin of the USB Connector. Based on the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, attaching a series 0.33 µF decoupling (DC blocking) capacitor to this pin before connecting to the USB connector is highly recommended.
- **USB3UP_TXDPB** (pin 81): This pin is the positive (+) signal of the upstream USB3.1 TX2+ TX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX-)[2] pin of the USB Connector.
- **USB3UP_TXDMB** (pin 82): This pin is the negative (-) signal of the upstream USB3.1 TX2- TX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX- (or TX+)[2] pin of the USB Connector.
- **USB3UP_RXDPB** (pin 84): This pin is the positive (+) signal of the upstream USB3.1 RX2+ RX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX+ (or RX-)[2] pin of the USB Connector. Based on the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, attaching a series 0.33 µF decoupling (DC blocking) capacitor to this pin before connecting to the USB connector is highly recommended.
- **USB3UP_RXDMB** (pin 85): This pin is the negative (-) signal of the upstream USB3.1 RX2- RX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX- (or RX+)[2] pin of the USB Connector. According to the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, this pin is highly recommended to have a series 0.33 µF decoupling (DC blocking) capacitor before connecting to the USB connector.

Note 1:	The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I^{2}C configuration registers.
2:	A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the TX lines are swapped, or if the positive and negative pins of the RX lines are swapped.

When connecting the upstream port of a USB5926C to a Type-C connector, an external basic Upstream Facing Port (UFP) Type-C Controller or USB Power Delivery (PD) Type-C Controller is required. For the standard Type-C port connection details, refer to Figure 4-1.

FIGURE 4-1: UPSTREAM PORT TYPE-C USB DATA CONNECTIONS



It is not recommended to connect a USB5926C to an embedded USB host. Consider using a USB5806C, USB5807C, USB5816C, or USB5826C device instead.

4.2 Type-C Downstream USB3 Port Signals (Ports 1-2)

When connecting a downstream port to a Type-C connector, a basic Downstream Facing Port (DFP) Type-C Controller or USB Power Delivery (PD) Type-C Controller is also required and must be properly connected to the hub for connection detection and orientation control.

- **USB2DN_DP1/USB2DN_DP2** (pin 6/28): This pin is the positive (+) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the D+/DP[1] pin of a USB Connector.
- **USB2DN_DM1/USB2DN_DM2** (pin 7/29): This pin is the negative (-) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the D-/DM[1] pin of a USB Connector.
- **USB3DN_TXDP1A/USB3DN_TXDP2A** (pin 8/30): This pin is the positive (+) signal of the downstream port TX1+ USB3.1 transmitter (TX) differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the

TX+ (or TX-)[2] pin of the USB Connector.

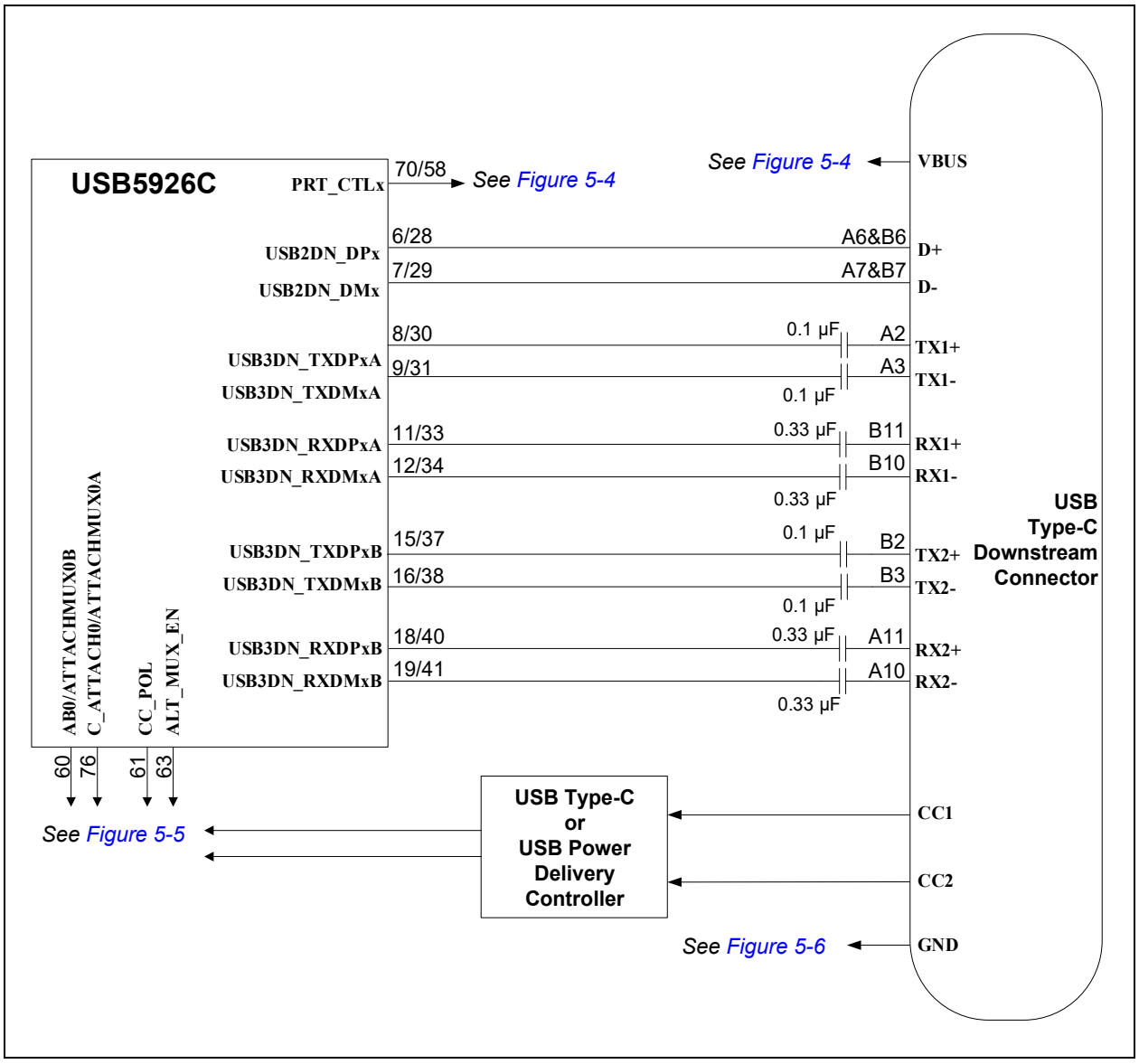
- **USB3DN_TXDM1A/USB3DN_TXDM2A** (pin 9/31): This pin is the negative (-) signal of the downstream port TX1- USB3.1 TX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX- (or TX+)[2] pin of the USB Connector.
- **USB3DN_TXDP1B/USB3DN_TXDP2B** (pin 15/37): This pin is the positive (+) signal of the downstream port TX2+ USB3.1 TX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX-)[2] pin of the USB Connector.
- **USB3DN_TXDM1B/USB3DN_TXDM2B** (pin 16/38): This pin is the negative (-) signal of the downstream port TX2- USB3.1 TX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX- (or TX+)[2] pin of the USB Connector.
- **USB3DN_RXDP1A/USB3DN_RXDP2A** (pin 11/33): This pin is the positive (+) signal of the downstream port RX1+ USB3.1 receiver (RX) differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX+ (or RX-)[2] pin of the USB Connector. According to the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, this pin is highly recommended to have a series 0.33 µF decoupling (DC blocking) capacitor before connecting to the USB connector.
- **USB3DN_RXDM1A/USB3DN_RXDM2A** (pin 12/34): This pin is the negative (-) signal of the downstream port RX1- USB3.1 RX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX- (or RX+)[2] pin of the USB Connector. According to the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, this pin is highly recommended to have a series 0.33 µF decoupling (DC blocking) capacitor before connecting to the USB connector.
- **USB3DN_RXDP1B/USB3DN_RXDP2B** (pin 18/40): This pin is the positive (+) signal of the downstream port RX2+ USB3.1 RX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX+ (or RX-)[2] pin of the USB Connector. According to the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, this pin is highly recommended to have a series 0.33 µF decoupling (DC blocking) capacitor before connecting to the USB connector.
- **USB3DN_RXDM1B/USB3DN_RXDM2B** (pin 19/41): This pin is the negative (-) signal of the downstream port RX2- USB3.1 RX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX- (or RX+)[2] pin of the USB Connector. According to the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, this pin is highly recommended to have a series 0.33 µF decoupling (DC blocking) capacitor before connecting to the USB connector.

Note 1: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I^{2}C configuration registers.

2: A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the TX lines are swapped, or if the positive and negative pins of the RX lines are swapped.

For the standard downstream Type-C port connection details, refer to Figure 4-2.

FIGURE 4-2: DOWNSTREAM PORT TYPE-C USB DATA CONNECTIONS



4.3 Type-A Downstream USB3 Port Signals (Ports 3-4)

- **USB2DN_DP3/USB2DN_DP4** (pin 43/86): This pin is the positive (+) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the D+/DP[1] pin of a USB Connector.
- **USB2DN_DM3/USB2DN_DM4** (pin 44/87): This pin is the negative (-) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the D-/DM[1] pin of a USB Connector.
- **USB3DN_TXDP3/USB3DN_TXDP4** (pin 45/88): This pin is the positive (+) signal of the downstream port USB3.1 transmitter (TX) differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX+ (or TX-)[2] pin of the USB Connector.
- **USB3DN_TXDM3/USB3DN_TXDM4** (pin 46/89): This pin is the negative (-) signal of the downstream port USB3.1 TX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin requires a series 0.1 µF decoupling (DC blocking) capacitor before being connected directly to the TX- (or TX+)[2] pin of the

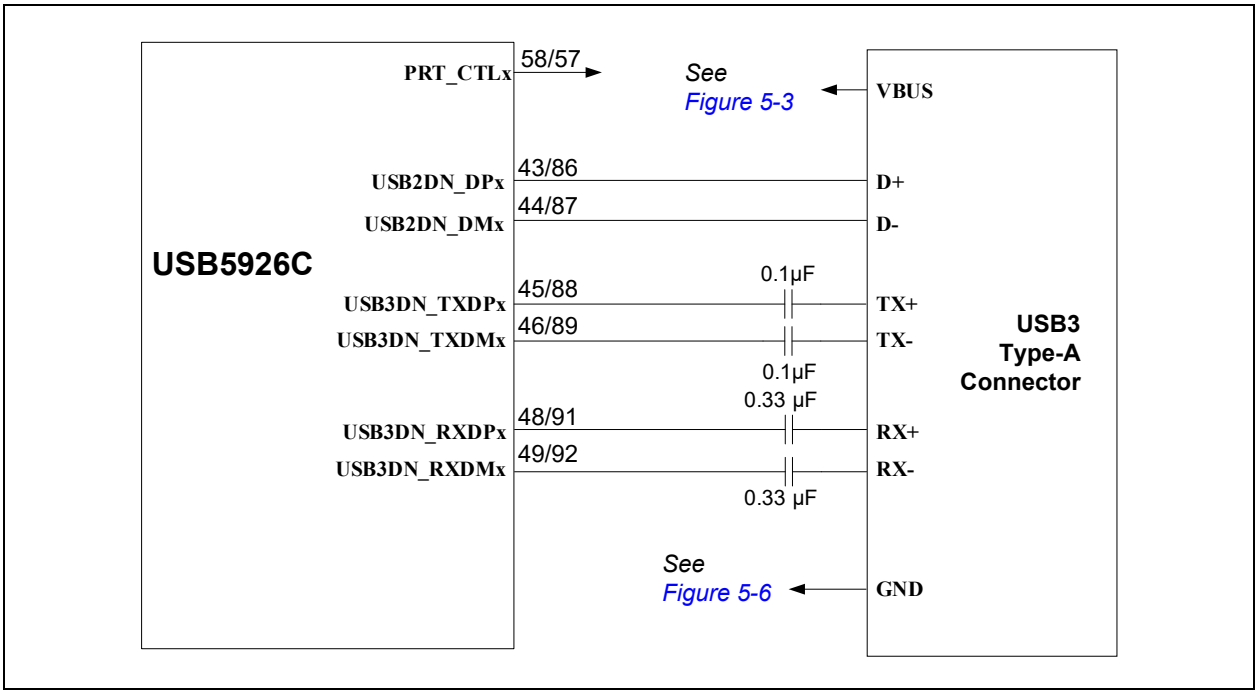
USB Connector.

- **USB3DN_RXDP3/USB3DN_RXDP4** (pin 48/91): This pin is the positive (+) signal of the downstream port USB3.1 receiver (RX) differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX+ (or RX-)[2] pin of the USB Connector. As stated in the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, this pin is highly recommended to have a series 0.33 µF decoupling (DC blocking) capacitor before connecting to the USB connector.
- **USB3DN_RXDM3/USB3DN_RXDM4** (pin 49/92): This pin is the negative (-) signal of the downstream port USB3.1 RX differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can be connected directly to the RX- (or RX+)[2] pin of the USB Connector. Based on the USB-IF Engineering Change Notice titled *RX AC Coupling Capacitor Option*, attaching a series 0.33 µF decoupling (DC blocking) capacitor to this pin is highly recommended before connecting it to the USB connector.

Note 1:	The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I^{2}C configuration registers.
2:	A standard feature of USB3.1 is automatic polarity detection and correction. There is no negative impact if the positive and negative pins of the TX lines are swapped, or if the positive and negative pins of the RX lines are swapped.

For the standard Type-A port connection details, refer to Figure 4-3.

FIGURE 4-3: DOWNSTREAM PORT TYPE-A USB CONNECTIONS

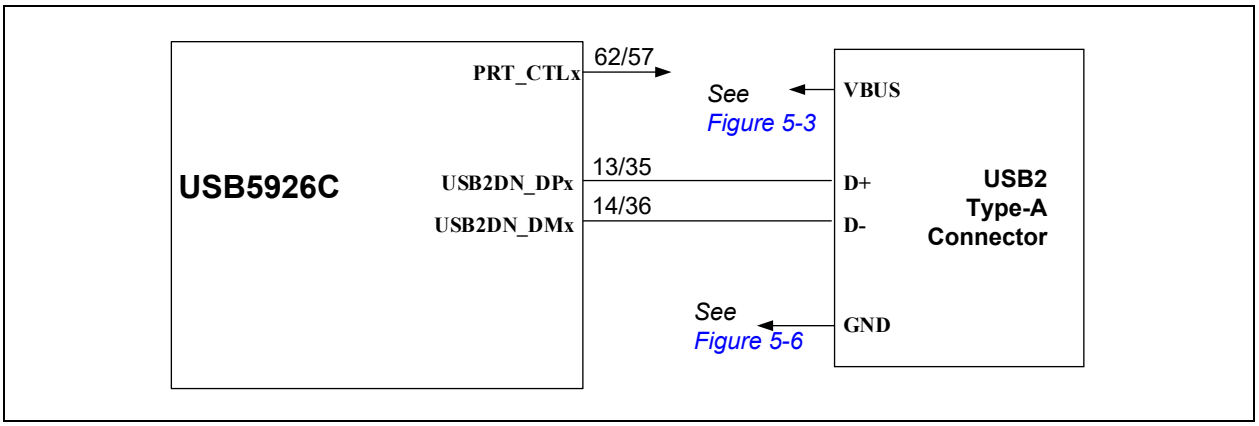


4.4 Type-A Downstream USB2.0 Port Signals (Ports 5 and 6)

- **USB2DN_DP5/USB2DN_DP6** (pin 13/35): This pin is the positive (+) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the D+/DP[1] pin of a USB Connector.
- **USB2DN_DM5/USB2DN_DM6** (pin 14/36): This pin is the negative (-) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the internal IC. This pin can connect directly to the D-/DM[1] pin of a USB Connector.

If connecting a downstream port to a USB2.0 only connector, refer to Figure 4-4. Note that in this configuration, the USB3.1 portion of the port should be disabled in the hub configuration to meet USB specification requirements.

FIGURE 4-4: DOWNSTREAM PORT USB2.0-ONLY TYPE-A USB CONNECTIONS



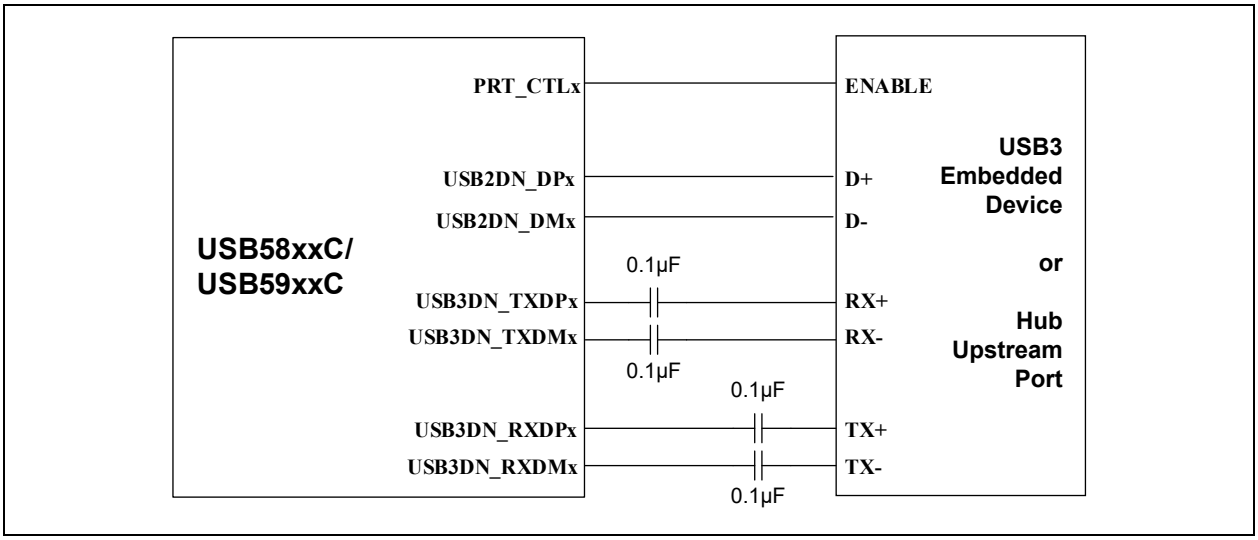
4.5 Downstream Port Connections to Embedded Devices or Secondary Hub Tiers

When connecting the downstream port to an embedded USB3.1 device, or the upstream port of another embedded USB3.1 hub, take note of the following design considerations:

- It is strongly recommended to use the **PRT_CTLx** pin to control the enable signal, Reset, or VBUS detection signal of the device or secondary tier hub. This ensures that:
  - the device or hub tier is able to achieve a Low-power state when the controlling hub is not connected or enabled.
  - the device or hub tier does not attempt to connect to the controlling hub until a host is present and the hub is ready to connect.
  - any attempt to reset the device using the USB hosts' port disable and re-enable command sequences have the intended effect.
- The differential signal polarity should be taken note. USB3 signals allow for automatic polarity detection and correction, but USB2.0 does not have this capability.
- It is strongly recommended to connect both the USB2.0 and USB3 interfaces of an embedded device, even if the device is intended to operate at USB3 speeds under normal use. This allows the devices to fall back to USB2.0 mode of operation in the event that the system is connected to a USB2.0-only host, or the USB3 operation fails for some reason.
- DC blocking/decoupling capacitors are required on both USB3 differential pairs.
- It must be ensured that the USB3 transmitter of the USB hub is connected to USB3 receiver or the device/secondary hub tier, and vice versa.

For an example on how to connect the downstream ports to an embedded USB device or hub upstream port, refer to Figure 4-5.

FIGURE 4-5: DOWNSTREAM PORT EMBEDDED DEVICE USB CONNECTIONS



4.6 Disabling Downstream Ports

If a downstream port of the USB5926C is unused, it should be disabled. This can be achieved through hub configuration (I^2C or OTP), or through a port disable strap option.

If using the port disable strap option, the USB2DN_DPx and USB2DN_DMx signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net, or through a pull-up resistor. All other signals related to the associated port may be floated.

4.7 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories.

- TVS protection diodes
  - ESD protection for IEC-61000-4-2 system-level tests
- Application-targeted protection ICs or galvanic isolation devices
  - DC overvoltage protection for short-to-battery protection
- Common-mode chokes
  - For EMI reduction

The USB5926C can be used in conjunction with these types of devices, but it is important to understand the negative effect on USB signal integrity that these devices may have and to select components accordingly and follow the implementation guidelines from the manufacturer of these devices. You may also use the following general guidelines for implementing these devices:

- Select only devices that are designed specifically for high-speed applications. Per the USB2.0 specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry. In a USB3.1 Gen 1 system, ESD protection should add no more than 0.5 pF capacitance to the differential pairs.
- Place ESD protection devices as close as possible to the USB connector.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- The effectiveness of TVS devices depends heavily on effective grounding. Always ensure a very low impedance path to a large ground plane.
- Place the TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

4.7.1 ADDITIONAL PROTECTION OPTIONS FOR USB3 PINS

In addition to TVS diodes, some or all of the following may be implemented:

- Use decoupling capacitors on both the TX and RX differential pairs. Decoupling capacitors on the RX pairs are not required for operation but add some additional ESD immunity at a low cost.
- Use decoupling capacitors with high voltage ratings. 0.1 µF capacitors at 0402 sizes are widely available.
- A very small resistor of 0.3Ω to 0.5Ω may be placed in series with the decoupling capacitor (placed physically between the TVS diode and the decoupling capacitor) to help steer more of the ESD energy through the TVS diode. A resistor network (2-resistor/4-contact) in 0402 or 0201 size can be placed with very little impact to the differential routing of the signals.

Note:	Microchip PHYBoost, VariSense, and High-Speed Disconnect Threshold adjustment configuration options are available for compensating the negative effects of these devices. These features can help overcome marginal failures. It is simplest to determine the appropriate setting using laboratory experiments, such as USB eye diagram tests, on physical hardware.

5.0 USB CONNECTORS

5.1 Upstream Port VBUS and VBUS_DET

The upstream port VBUS line must have no more than 10 µF of total capacitance connected.

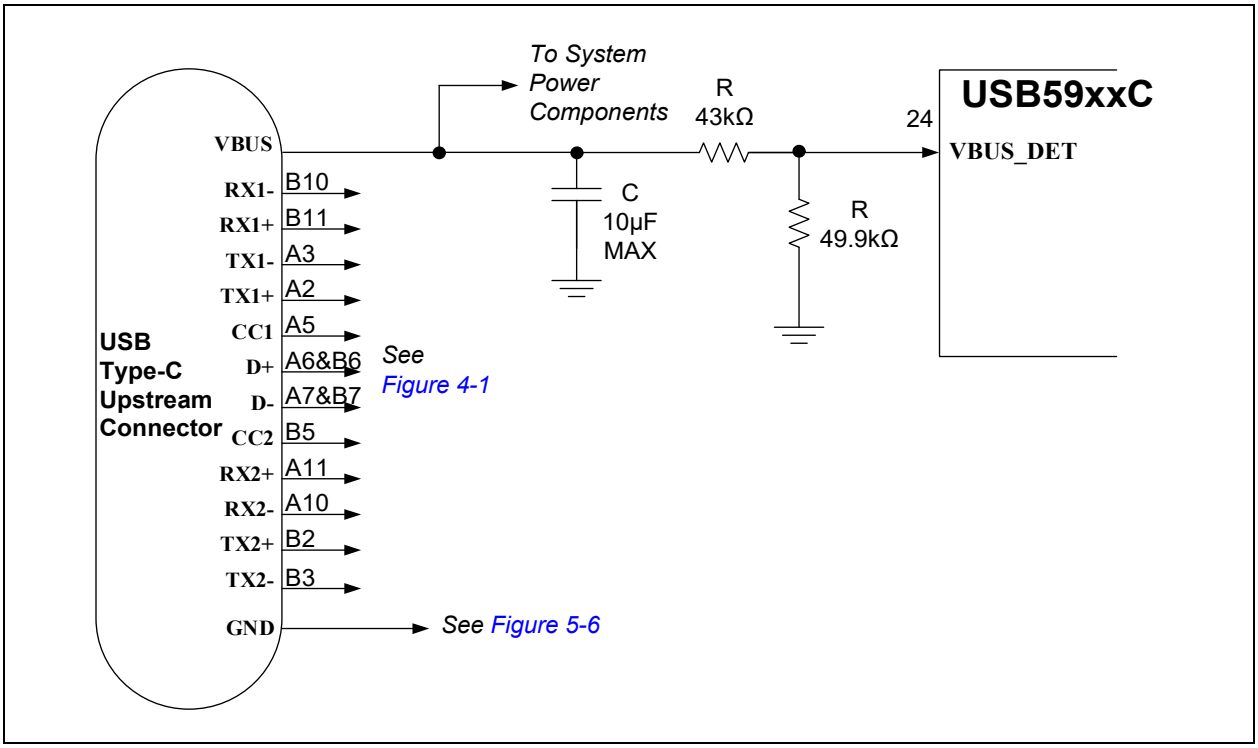
The **VBUS_DET** pin is used by the USB5926C to detect the presence of a USB host. The USB host can also toggle the state of VBUS at any time to force a soft Reset and reconnection of the USB5926C.

It is permissible to tie **VBUS_DET** directly to 3.3V. However, this is not recommended as the ability to force a Reset of the hub from the USB host VBUS control is lost.

If connecting the upstream port to a basic USB Type-C port where VBUS never exceeds 5V, the recommended implementation is shown in Figure 5-1. Note that the precise resistor values are not critical, and alternate values may be selected as long as:

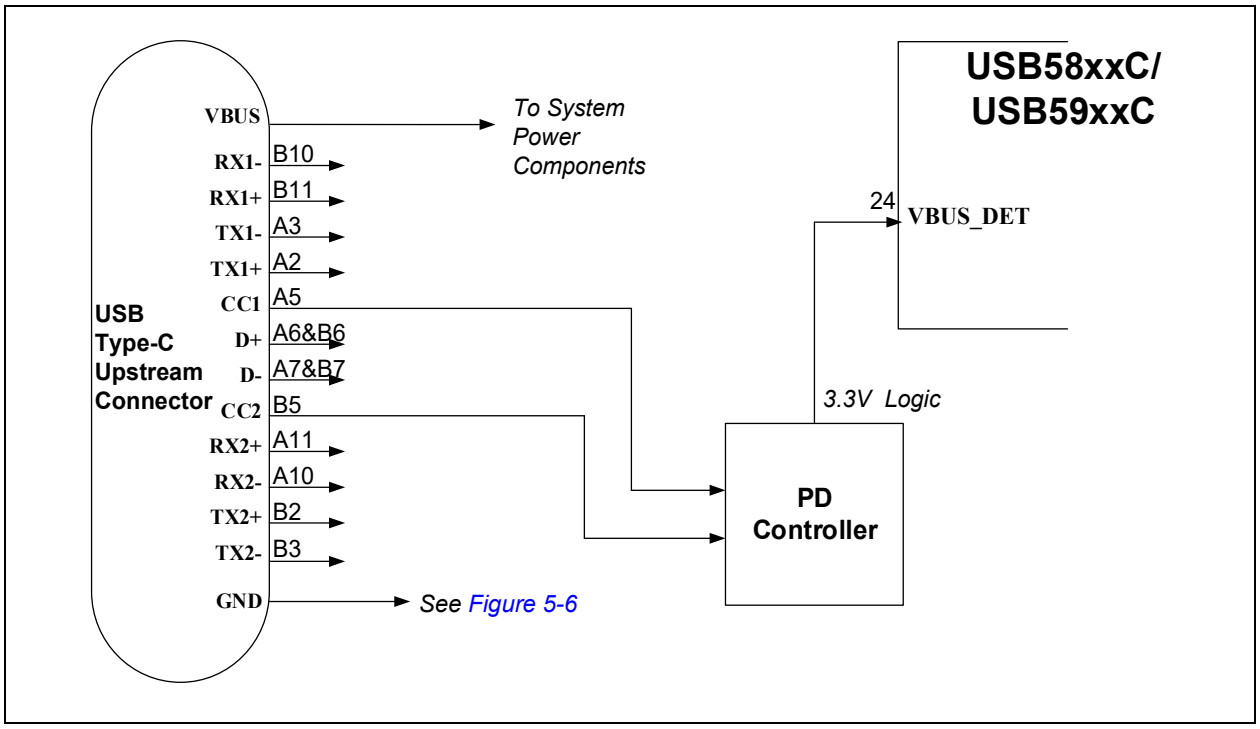
- The impedance from the **VBUS** pin of the USB connector to the **VBUS_DET** pin is sufficiently high to minimize pin leakage when VBUS is present before the hub IC is powered on.
- A sufficient voltage level is present on the **VBUS_DET** pin for the full range of VBUS (4.5V to 5.5V).

FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS FOR A BASIC TYPE-C PORT



If connecting the upstream port to USB Type-C with USB Power Delivery support (where VBUS may be elevated above 5V), the recommended implementation is shown in Figure 5-2.

FIGURE 5-2: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS FOR A FULL FEATURED TYPE-C PORT WITH POWER DELIVERY



5.2 Downstream Port VBUS and PRT_CTLx Connections for Standard Type-A Ports

The **PRT_CTLx** pin is a hybrid input/output (I/O) pin that has the following states:

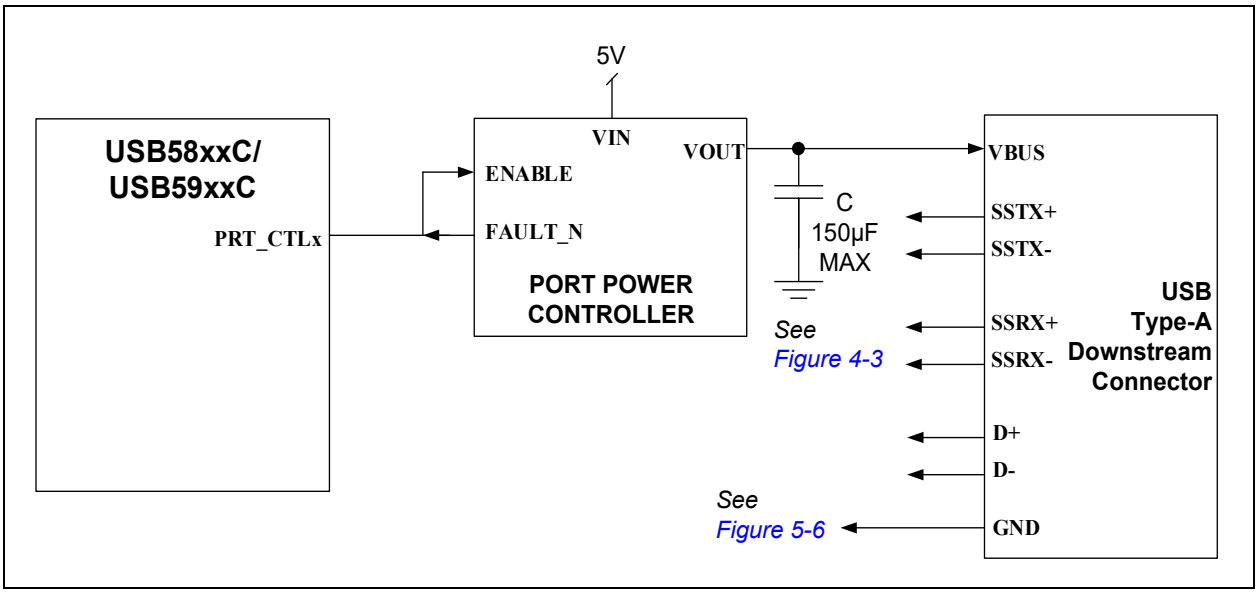
- *PORT OFF*: **PRT_CTLx** is an output and drives low. The **PRT_CTLx** pin will only transition to the PORT ON state through a specific command from the USB host.
- *PORT ON*: **PRT_CTLx** is an input with an internal weak pull-up enabled. The input buffer monitors for overcurrent events, which are indicated by the port power controller by pulling the PRT_CTLx line low. Once an overcurrent event is detected, the PRT_CTLx automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

When connecting the **PRT_CTLx** pin to a port power controller, the signal should be connected to both the enable and the Fault indicator pins of the port power controller. Do not place an external pull-up resistor on the line.

Note:	The overcurrent detect debounce parameters are configurable and may be adjusted if required to operate properly with the selected port power controller.

A typical downstream port Type-A implementation is shown in Figure 5-3.

FIGURE 5-3: DOWNSTREAM PORT VBUS AND PRT_CTLX CONNECTIONS

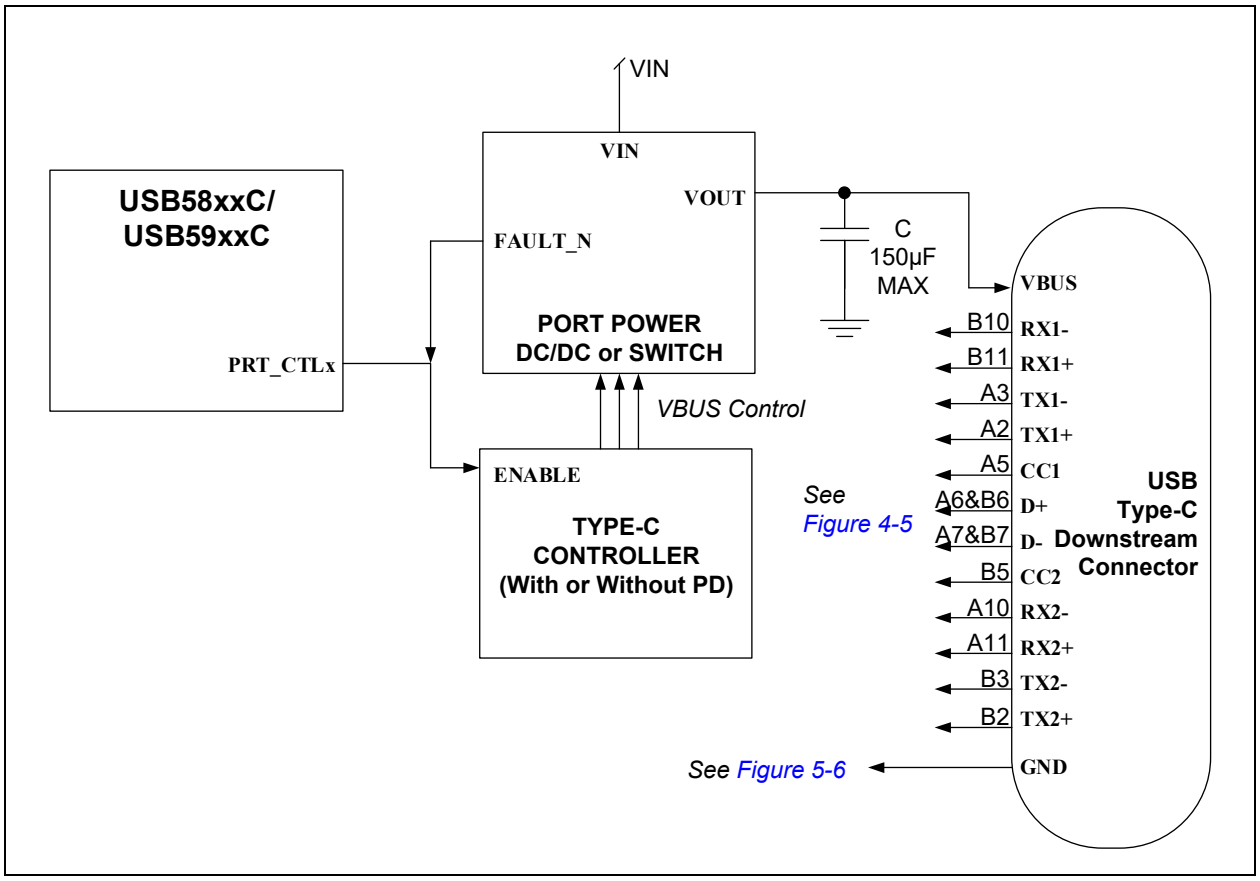


The implementation as shown in Figure 5-3 assumes that the port power controller has an active-high enable input, and an active-low, open-drain style Fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.3 Downstream Port VBUS and PRTCTLx Connections for Type-C Ports

A typical Type-C implementation is shown in Figure 5-4. Specific details on how to connect the VBUS switch or DC/DC regulator should be obtained from the supplier of the Type-C/Power Delivery controller device.

FIGURE 5-4: DOWNSTREAM PORT VBUS AND PRT_CTL CONNECTIONS FOR TYPE-C PORT



Note:	The implementation as shown in Figure 5-4 assumes that the port power controller has an active-high enable input, and an active-low, open-drain style Fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.4 Type-C Port Control

Type-C ports require external Type-C port controllers. These port controllers are necessary to:

- inform the hub port when a valid Type-C attach is detected.
- inform the hub port about the orientation of the Type-C connection.
- (Upstream Facing Ports only) ensure the **VBUS_DET** pin reflects the state of VBUS or the attach state of the Type-C port.
  - For basic USB® Type-C ports that do not elevate VBUS beyond the nominal 5V level, **VBUS_DET** can be connected directly to the **VBUS** pin of the USB connector through a resistor divider, similar to Type-B applications.
  - For USB Power-Delivery-capable Type-C ports that elevate VBUS beyond the nominal 5V levels, **VBUS_DET** cannot be connected directly to **VBUS**. Instead, a connection indicator must control the **VBUS_DET** pin. For example, the same control line that connects to the **C_ATTACH0** pin to communicate when Type-C is attached may also be connected to **VBUS_DET** in this case.
- (Downstream Facing Ports only) control VBUS and VCONN power supplies according to Type-C port requirements.

There are several configuration options available, which allow the USB5926C control scheme to be adapted to closely match the available control signals of the selected Type-C controller.

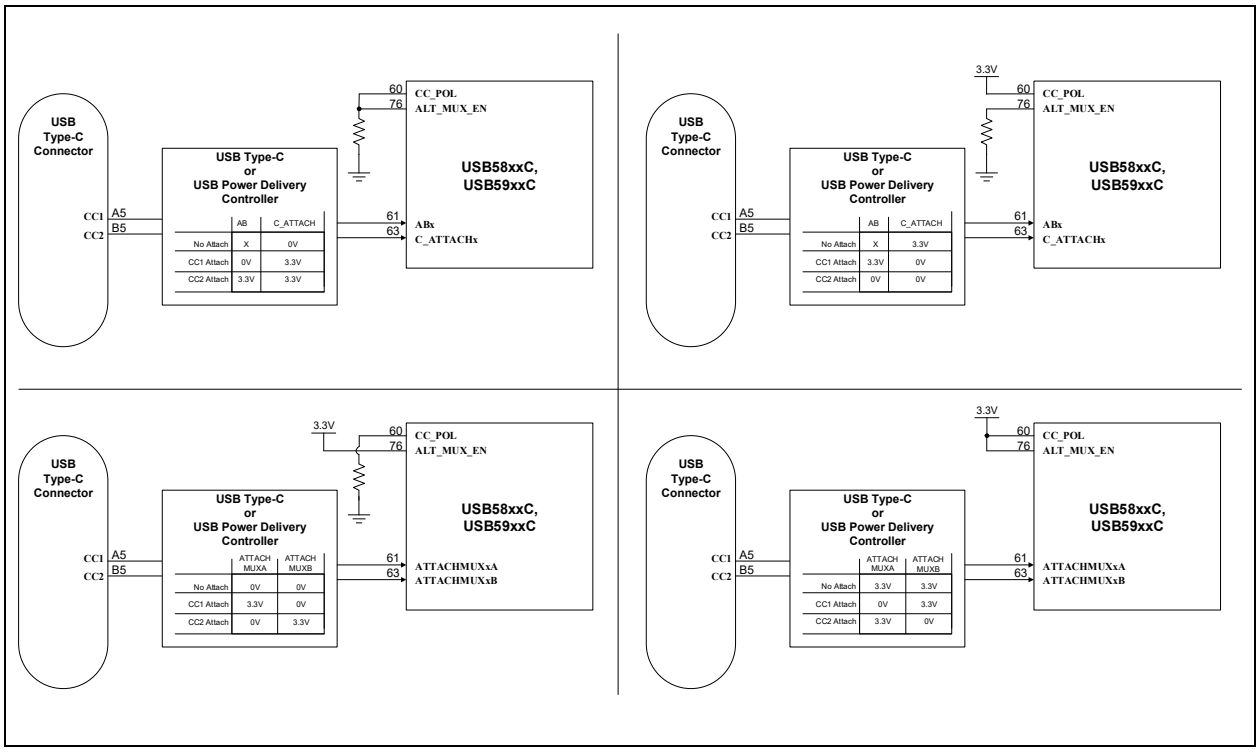
The control scheme is selected via the state of **CC_POL** (pin 61) and **ALT_MUX_EN** (pin 63), which impacts how the **C_ATTACHx/ATTACHMUXxA** and the **ABx/ATTACHMUXxB** pins must control the hub interface.

TABLE 5-1: TYPE-C CONTROL OPTIONS

ALT_MUX_EN	CC_POL	Connection State	Required Input Controls	Active USB3 PHY
0 ABx and C_ATTACHx Mode	0	Type-C Detached	C_ATTACHx: 0 ABx: X (Don't Care)	none
		Type-C Attached and in "Unflipped" Orientation (CC line detected on CC1 pin)	C_ATTACHx: 1 ABx: 0	A
		Type-C Attached and in "Flipped" Orientation (CC line detected on CC2 pin)	C_ATTACHx: 1 ABx: 1	B
	1	Type-C Detached	C_ATTACHx: 1 ABx: X (Don't Care)	none
		Type-C Attached and in "Unflipped" Orientation (CC line detected on CC1 pin)	C_ATTACHx: 0 ABx: 1	A
		Type-C Attached and in "Flipped" Orientation (CC line detected on CC2 pin)	C_ATTACHx: 0 ABx: 0	B
1 ATTACHMUXxA and ATTACHMUXxB Mode	0	Type-C Detached	ATTACHMUXxA: 0 ATTACHMUXxB: 0	none
		Type-C Attached and in "Unflipped" Orientation (CC line detected on CC1 pin)	ATTACHMUXxA: 1 ATTACHMUXxB: 0	A
		Type-C Attached and in "Flipped" Orientation (CC line detected on CC2 pin)	ATTACHMUXxA: 0 ATTACHMUXxB: 1	B
	1	Type-C Detached	ATTACHMUXxA: 1 ATTACHMUXxB: 1	none
		Type-C Attached and in "Unflipped" Orientation (CC line detected on CC1 pin)	ATTACHMUXxA: 0 ATTACHMUXxB: 1	A
		Type-C Attached and in "Flipped" Orientation (CC line detected on CC2 pin)	ATTACHMUXxA: 1 ATTACHMUXxB: 0	B

A schematic level representation of the Type-C control options is shown in Figure 5-5.

FIGURE 5-5: TYPE-C PORT CONTROL OPTIONS



5.5 GND and EARTH Recommendations

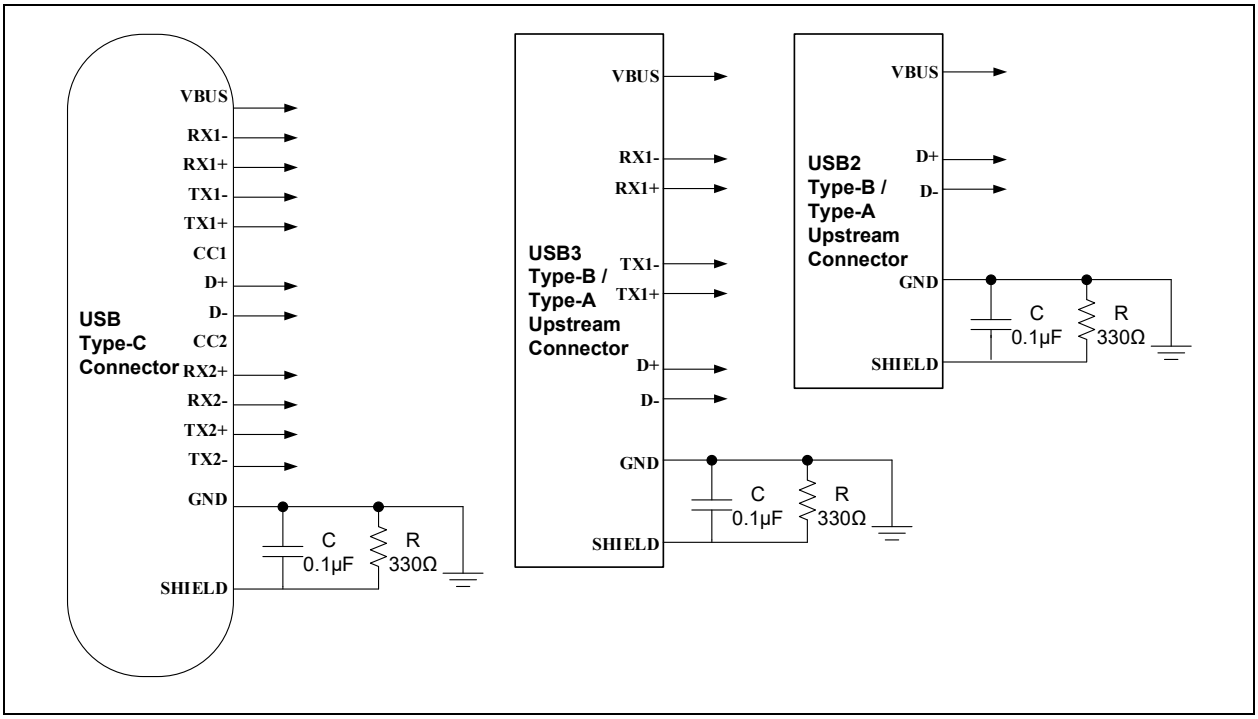
The **GND** pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The EARTH pins of the USB connector may be connected in one of two ways:

- (Recommended) To the GND plane through a resistor and a capacitor in parallel. An RC filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Directly to the GND plane

The recommended implementation is shown in Figure 5-6.

FIGURE 5-6: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



6.0 CLOCK CIRCUIT

6.1 Crystal or External Clock Connection

A 25.000 MHz (±50 ppm) reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *USB5926C Data Sheet*.

- **XTALI** (pin 3) is the clock circuit input for the USB5926C. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTALO** (pin 4) is the clock circuit output for theUSB5926C. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- The crystal loading capacitor values are system-dependent, based on the total C_L specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly-used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:

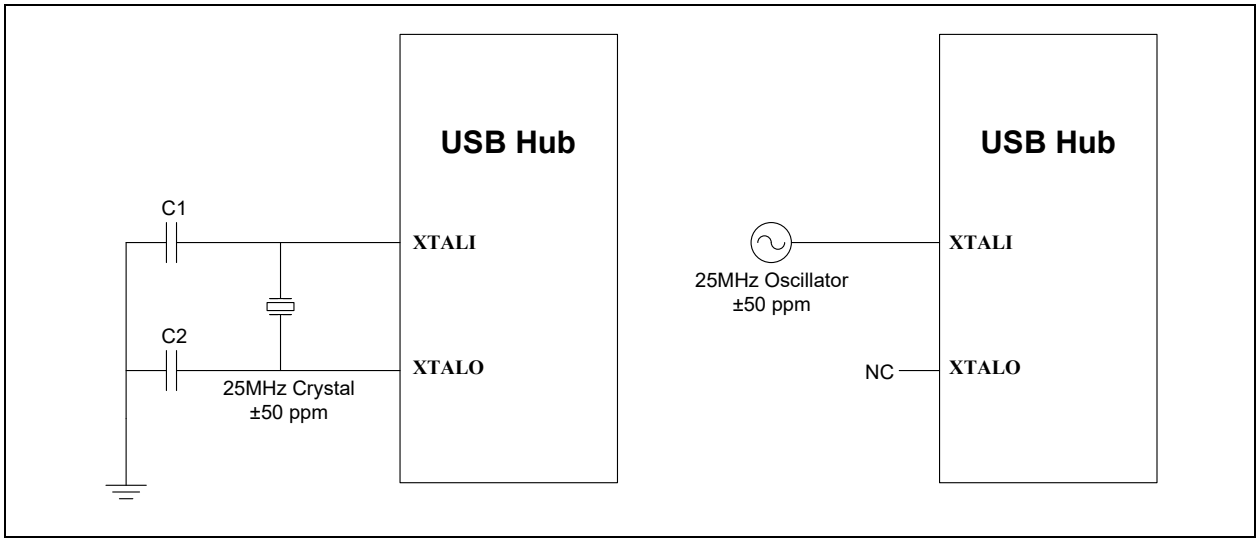
  $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$

  Where: C_L is the specification from the crystal data sheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$

Note: C_{stray} is the stray/parasitic capacitance due to PCB layout. It can be assumed to be very small, in the 1-2 pF range, and then verified by physical experiments in the laboratory if PCB simulation tools are not available.

- Alternately, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the USB5926C. When using a single-ended clock source, **XTALO** should be left floating as No Connect (NC).

FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS



7.0 POWER AND STARTUP

7.1 RBIAS Resistor

RBIAS (pin 1) on the USB5926C must connect to ground through a 12 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close as possible to the IC pin, and be given a dedicated, low impedance path to a ground plane.

7.2 Board Power Supplies

7.2.1 POWER RISE TIME

The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB5926C Data Sheet*.

If a monotonic/fast power rail rise cannot be assured, then the RESET_N signal should be controlled by a Reset supervisor and only released when the power rail has reached a stable level.

7.2.2 CURRENT CAPABILITY

It is important to size the 5V and 3.3V power rails appropriately. The 5V power supply must be capable of supplying sufficient power for all exposed USB ports concurrently without drooping below the minimum voltage permissible in the USB specification:

- 500 mA per-port for USB2 ports if BC1.2 is not enabled on the port
- 900 mA per-port for USB3 ports if BC1.2 is not enabled on the port
- 1.5A per BC1.2-enabled port (if BC1.2 is enabled)
- 1.5A or 3.0A per Type-C port (depending on setting of the Type-C controller)

The 3.3V power supply must be able to supply enough power to the USB hub IC. It is recommend that 3.3V power rail be sized such that is able to supply the maximum power consumption specification as displayed in the *USB5926C Data Sheet*

The 1.2V power supply must be able to supply enough power to the USB hub IC. It is recommend that 1.2V power rail be sized such that is able to supply the maximum power consumption specification as displayed in the *USB5926C Data Sheet*

7.3 Reset Circuit

RESET_N (pin 25) is an active-low Reset input. This signal resets all logic and registers within the USB5926C. A hardware Reset (RESET_N assertion) is not required following power-up. Please refer to the latest copy of the *USB5926C Data Sheet* for Reset timing requirements. Figure 7-1 shows a recommended Reset circuit for powering up the USB5926C when Reset is triggered by the power supply. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

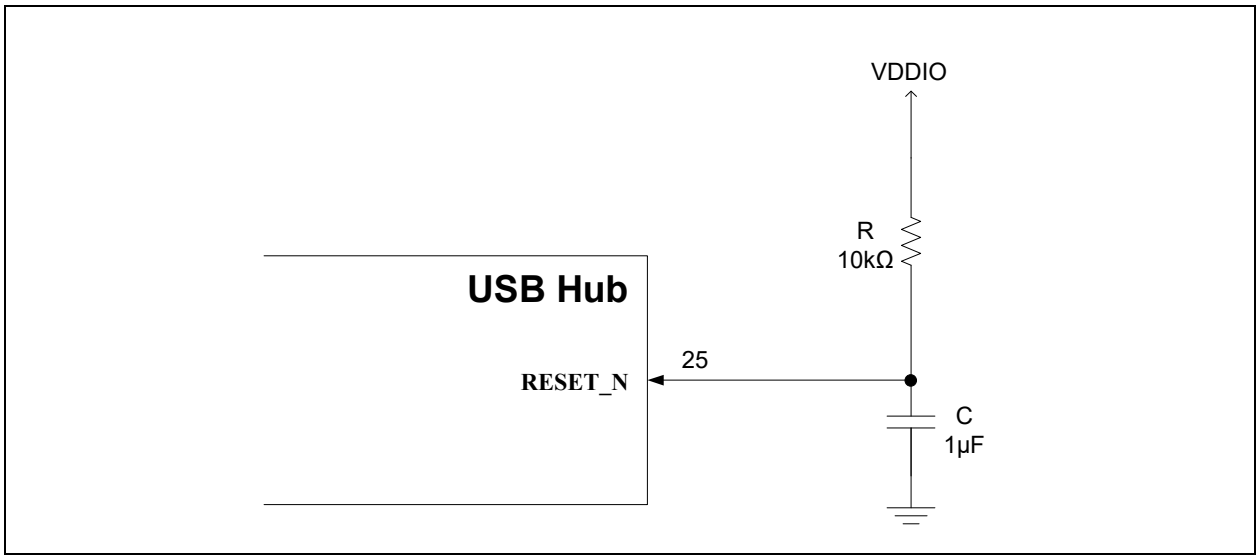
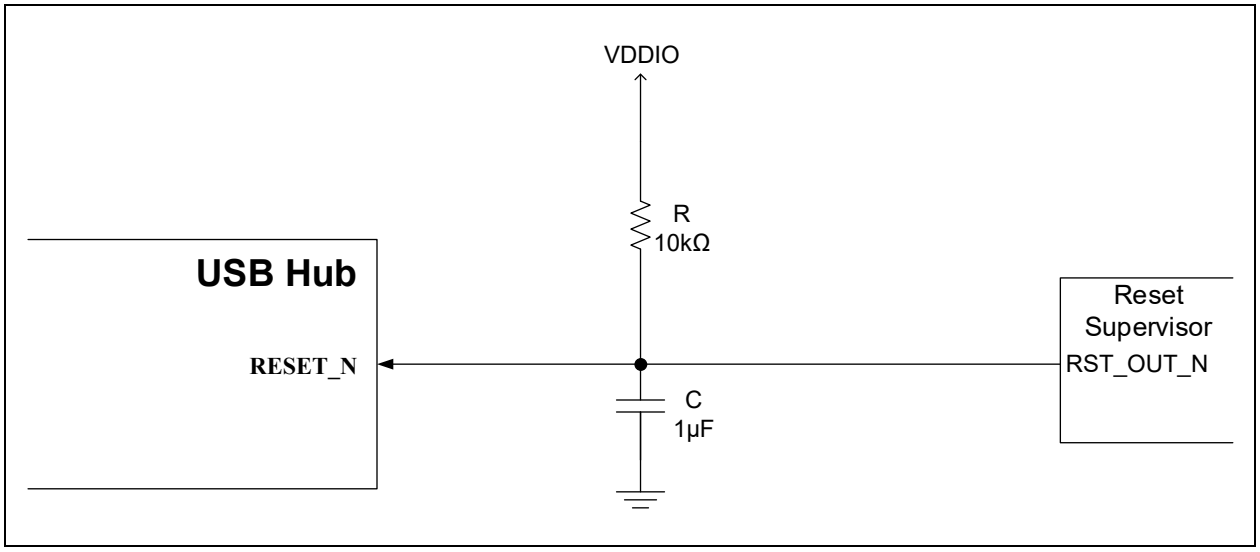


Figure 7-2 details the recommended Reset circuit for applications where Reset is driven by an external CPU/MCU. The Reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm Reset after power-up. The values for the "R" resistor and "C" capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT



8.0 EXTERNAL SPI MEMORY

8.1 SPI Operation Summary

By default, the USB5926C executes firmware from an internal read only memory (ROM). The USB5926C supports optional firmware execution from an external SPI Flash device. An SPI Flash device is only required if a custom firmware is required for the application.

The SPI interface can operate at 60 MHz or 30 MHz.

The SPI interface can operate in Dual mode or Quad mode.

The firmware image can be executed in one of two ways:

- *Execute in place*: Firmware is continuously executed directly from the SPI Flash device, and the interface is constantly active.
- *Execute in internal SRAM*: Firmware is loaded into the hub's internal SRAM and executed internally. This may only be supported if the firmware image is smaller than the hub's SRAM size.

Note: All firmware images are developed, compiled, tested, and provided by Microchip. The SPI interface speed is an OTP-configurable option and only speeds that were specifically tested with the firmware image should be selected. The execution method is configured with the firmware image itself and cannot be changed via configuration.

8.2 Compatible SPI Flash Devices

Microchip recommends SST-brand SPI Flash devices. Microchip has verified compatibility of the following list of SPI Flash devices:

- SST26VF064B
- SST25VF064C

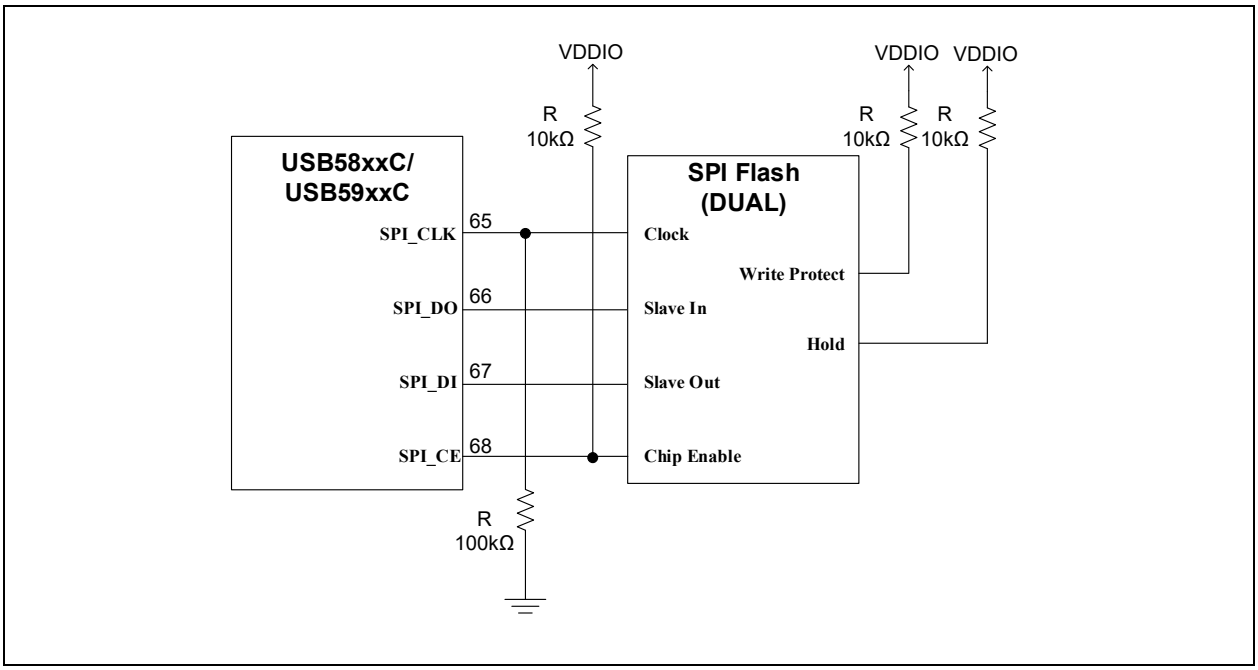
Other SPI Flash devices may be used, provided that they meet the following minimum requirements:

- 30 MHz or 60 MHz operation
- Mode 0 or Mode 3
- 256 KB or larger memory
- Utilize same OpCode commands as the devices in the above list of compatible devices
- Dual mode or Quad mode operation

8.3 SPI Connection Diagrams

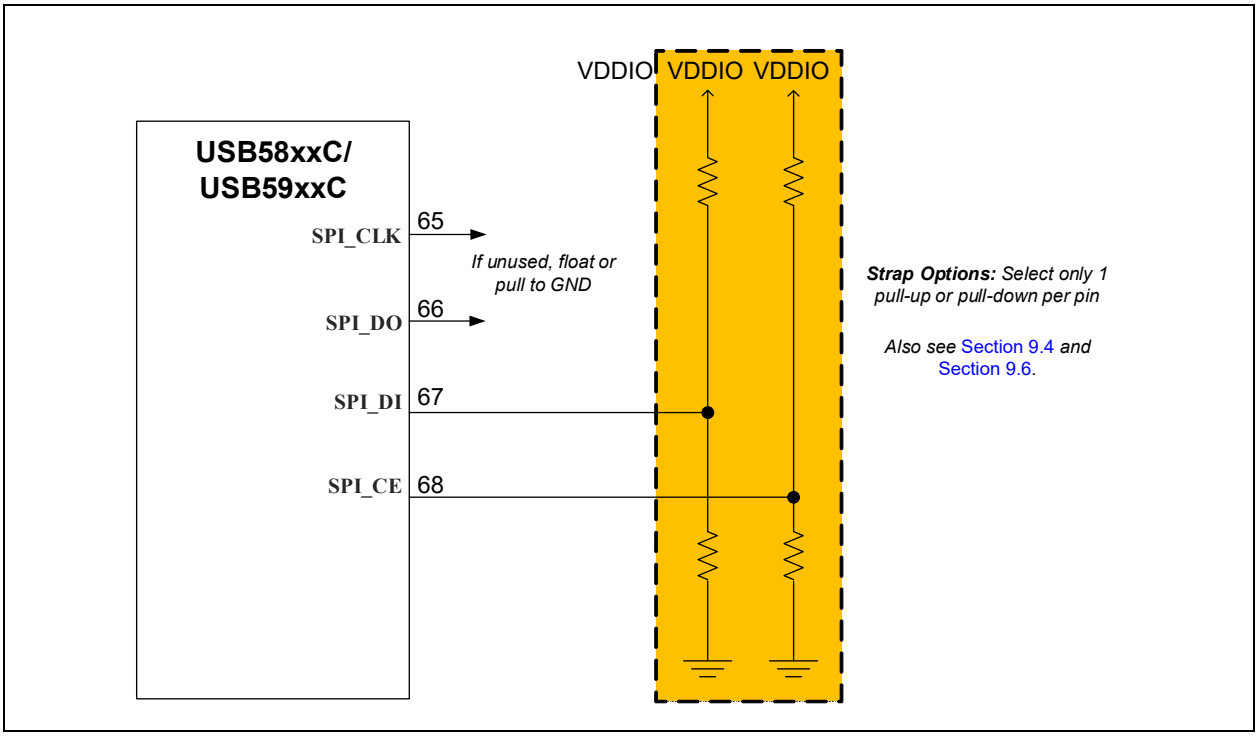
If a Dual SPI Flash device is used, the recommended schematic connections are shown in Figure 8-1.

FIGURE 8-1: DUAL SPI FLASH CONNECTIONS



If an SPI Flash device is not used, the recommended schematic connections are shown in Figure 8-2. Some of the SPI pins become configuration straps when an SPI Flash device is not connected. A configuration strap option must be selected, and these pins cannot be floated.

FIGURE 8-2: RECOMMENDED CONNECTIONS IF SPI FLASH IS NOT USED



9.0 MISCELLANEOUS

9.1 GPIOs

The USB5926C has 13 pins, which may be controlled from the USB host or from an embedded SOC/MCU as GPIOs. These GPIOs are available to be used without any additional configuration (more may be made available for use via additional configuration steps (see *AN1997 - USB-to-GPIO Bridging with Microchip USB3.1 Gen 1 Hubs*). By default, all of the GPIOs are configured as inputs. If a default output Power-on state is required, the default pin Output state can be configured in the hub's OTP memory or through the I^{2}C/SMBus slave interface during the configuration stage (SOC_CFG). See Table 9-1 for pin description.

TABLE 9-1: AVAILABLE GPIOS

Pin	Pin Name	GPIO	Configuration Requirements
60	GPIO3	GPIO3	Available by default
69	GPIO69	GPIO69	Available by default
71	GPIO66	GPIO66	Available by default

Instructions for operating these pins, including register definitions, are described in full in *AN1997 - USB-to-GPIO Bridging with Microchip USB3.1 Gen 1 Hubs*.

Ensure that the voltages applied to these pins are within the electrical specifications for the pins, and that any external loading is within the drive strength capabilities as described in the *USB5926C Data Sheet*.

9.2 I^{2}C/SMBus Connections

The USB5926C has one I^{2}C/SMBus interface that can operate in Master or Slave mode.The mode of operation is selected via the **CFG_STRAP** (pin 20) resistor selection.

TABLE 9-2: I^{2}C/SMBUS PINS

Pin	Name	Role	Configuration Requirements
74	SMBDATA/GPIO6	I^{2}C Slave or Master Data	**I^{2}C Slave mode:** CONFIG2 is selected on CFG_STRAP (pin 20) via a 200 kΩ pull-up resistor to 3.3V. **I^{2}C Master mode:** CONFIG1 is selected on CFG_STRAP (pin 20) via a 200 kΩ pull-down resistor to ground.
75	SMBCLK/GPIO8	I^{2}C Slave or Master Data	

9.2.1 SLAVE INTERFACE

The USB5926C may be configured by an embedded SOC/MCU during both the start-up and runtime stages. The **CFG_STRAP** pin must set the hub into CONFIG2 via a 200 kΩ pull-up resistor to 3.3V. Additionally, pull-up resistors must be detected on the **SMBDATA** and **SMBCLK** pins by the hub at start-up in order for the I^{2}C/SMBus slave interface to become active. The interface command specification and configuration register set are described in full in *AN2316 - Configuration Options for the USB58xx and USB59xx Application Note*.

Typically, a pull-up resistor of 1 kΩ to 10 kΩ is sufficient, depending on the interface speed and total capacitance on I^{2}C tree.

A pull-up voltage of 1.8V to 3.3V is supported.

Note:	If I^{2}C/SMBus pull-up resistors are detected by the USB5926C at start-up, the hub will wait indefinitely to be configured by the attached I^{2}C/SMBus master. For early prototyping, it may be necessary to physically remove the pull-up resistors until the I^{2}C/SMBus master is fully operational and able to properly configure the hub at start-up.

9.2.2 MASTER INTERFACE

The USB5926C has an I²C/SMBus master interface that can bridge USB commands to I²C/SMBus. Instructions for operating the I²C/SMBus master interface are described in *AN1998 - USB to I2C Bridging with Microchip USB 3.1 Gen 1 Hubs*.

In order to enter the I²C/SMBus Master mode, the **CFG_STRAP** pin must set the hub into CONFIG1 via a 200 kΩ pull-down resistor to ground.

Typically, a pull-up resistor of 1 kΩ to 10 kΩ is sufficient on the **SMDAT** and **SMCLK** pins, depending on the configured interface speed and total capacitance on the I²C tree.

A pull-up voltage of 1.8V to 3.3V is supported.

Ensure that all I²C/SMBus slave devices connected to the bus have unique addresses assigned.

Ensure that the USB5926C and all I²C/SMBus slave devices connected to the bus can support the target bus speed.

9.3 FlexConnect

The FlexConnect feature allows the USB2 and USB3 host role to be reassigned to downstream port 1 of the hub. For any FlexConnect application, the key design options to consider are:

- How FlexConnect will be controlled (initiated and terminated)
- How the **VBUS_DET** pin will be handled
- How the respective USB Type-C® port (if present in the system) roles will stay in sync with the FlexConnect state

FlexConnect can be initiated via one of three methods:

- The **FLEX_CMD** pin
- A USB command to the Hub Feature Controller (HFC)
- Direct register manipulation via the I²C/SMBus slave interface

This feature is highly implementation-specific and usually has numerous hardware design ramifications. If the FlexConnect feature is required in any specific application, it is recommended to reach out to a Microchip support representative early on in the design cycle to discuss the options available.

The FlexConnect feature and design guidelines are further explained in *AN4027 - USB58xx and USB59xx FlexConnect Operation.*

9.4 Non-Removable Port Settings

The USB5926C has a configuration strap option, **CFG_NON_REM**, which can be used to set the default non-removable port settings. **CFG_NON_REM** is located on pin 68. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI Flash device. These are described in Table 9-3.

TABLE 9-3: CFG_NON_REM

Setting	Effect
200 kΩ pull-down to GND	All ports are removable.
200 kΩ pull-up to 3.3V	Port 3 is non-removable. Only a valid selection if port 3 is connected directly to an embedded USB device.
10 kΩ pull-down to GND	Ports 3 and 4 are non-removable. Only a valid selection if ports 3 and 4 are connected directly to embedded USB devices.
10 kΩ pull-up to 3.3V	Ports 3, 4, and 5 are non-removable. Only a valid selection if ports 3, 4 and 5 are connected directly to embedded USB devices.
10Ω pull-down to GND	Ports 3, 4, 5, and 6 are non-removable. Only a valid selection if ports 3, 4, 5, and 6 are connected directly to embedded USB devices.
10Ω pull-up to 3.3V	Reserved

The following guidelines can be used to determine which setting to use:

- If the port is routed to a user-accessible USB connector, it is *removable*.
- If the port is routed to a permanently attached and embedded USB device on the same PCB, or non-user-accessi-

ble wiring or cable harness, it is *non-removable*.

Note:	The removable/non-removable device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors that the USB host may use to understand if a port is a user-accessible port, or if the device is a permanently-attached device. Under standard operating conditions, the USB host may or may not modify its operation based upon this information. Certain USB compliance tests are impacted by this setting, so designs that must undergo USB compliance testing and certification must ensure that the configuration settings are correct.

9.5 Self-Powered/Bus-Powered Settings

In a typical USB5926C application, the hub should be configured as self-powered, which is the default configuration setting.

The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is powered completely from the upstream USB connector's **VBUS** pin and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is *bus-powered*.
- If the entire system (hub included) is always powered by a separate power connector, then the hub system is *self-powered*.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely *self-powered* (even if all of the power is derived from the upstream USB connector's **VBUS** pin).

Note:	The self-powered/bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors that the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host will typically limit the downstream ports of a self-powered hub to 100 mA. Any device that connects to a self-powered hub that declares it needs more than 100 mA will be prevented from operating by the USB host.

9.6 Battery Charging Settings

The USB5926C hub includes built-in Dedicated Charging Port (DCP), Charging Downstream Port (CDP), and vendor-specific (SE1) battery charging support.

The USB5926C has a configuration strap option, **CFG_BC_EN**, which can be used to set the default configuration for port 1. **CFG_BC_EN** is located on pin 67. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI Flash device. The configuration strap options are described in Table 9-4.

TABLE 9-4: CFG_BC_EN

Setting	Effect	Additional Notes
200 kΩ pull-down to GND	Port 1 BC disabled	Battery Charging is not enabled. Select this option if configuration will be done in hub OTP, via I^2C/SMBus, or by external FW in SPI Flash. If SE1 charging is required, this strap option should be selected and SE1 must be enabled in hub OTP, via I^2C/SMBus, or by external FW in SPI Flash.

TABLE 9-4: CFG_BC_EN (CONTINUED)

Setting	Effect	Additional Notes
200 kΩ pull-up to 3.3V	Port 1 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream port 1 operates in Dedicated Charging Port (DCP) mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream port 1 operates in Charging Downstream Port (CDP) mode.
10 kΩ pull-down to GND	Ports 1 and 2 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream ports 1 and 2 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1 and 2 operate in CDP mode.
10 kΩ pull-up to 3.3V	Ports 1, 2, and 3 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream ports 1, 2, and 3 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1, 2, and 3 operate in CDP mode.
10Ω pull-down to GND	Ports 1, 2, 3, and 4 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream ports 1, 2, 3, and 4 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1, 2, 3, and 4 operate in CDP mode.
10Ω pull-up to 3.3V	Ports 1, 2, 3, 4, 5, and 6 BC enabled	Battery Charging is enabled. When no USB host is present (VBUS_DET = 0), downstream ports 1, 2, 3, 4, 5, and 6 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1, 2, 3, 4, 5, and 6 operate in CDP mode.

Note: The vendor-specific SE1 Charging mode uses the USB data lines to communicate charging capability. Hence, SE1 can only be active when no USB host is present. Additional vendor-specific charging modes exist for charging at elevated current levels when an active data connection is also present. This is handled by vendor-specific USB protocol between the USB host and the device. The USB5926C supports these vendor-specific protocol exchanges. These vendor-specific command specifications must be obtained from the respective device vendors.

10.0 HARDWARE CHECKLIST SUMMARY

TABLE 10-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.2, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.3, "Ground"	Verify that the grounds are tied together.		
	Section 2.4, "USB-IF Compliant USB Connectors"	Verify that USB-IF-compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"	Section 3.1, "Power and Bypass Capacitance"	• Ensure **VDD33** is in the range 3.0V to 3.6V, and a 0.1 µF capacitor is on each pin. • Ensure **VDD12** is in the range 1.08V to 1.32V, and a 0.1 µF capacitor is on each pin.		
Section 4.0, "USB Signals"	Section 4.1, "Upstream Port USB Signals"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D- data lines, and do not cross the USB3 TX and RX differential pairs. Also ensure an external Type-C controller capable of UFP operation is present.		
	Section 4.2, "Type-C Downstream USB3 Port Signals (Ports 1-2)"	Verify that the USB data pins are correctly routed to the USB Type-C Connectors connectors. Pay special attention to the polarity of the USB2.0 D+ and D- data lines, and do not cross the USB3 TX and RX differential pairs. Also ensure an external Type-C controller capable of DFP operation is present.		
	Section 4.3, "Type-A Downstream USB3 Port Signals (Ports 3-4)"	Verify that the USB data pins are correctly routed to the USB3 Type-A connectors. Pay special attention to the polarity of the USB2.0 D+ and D- data lines, and do not cross the USB3 TX and RX differential pairs.		
	Section 4.4, "Type-A Downstream USB2.0 Port Signals (Ports 5 and 6)"	Verify that the USB data pins are correctly routed to the USB2 Type-A connectors. Pay special attention to the polarity of the USB2.0 D+ and D- data lines.		
	Section 4.5, "Downstream Port Connections to Embedded Devices or Secondary Hub Tiers"	Verify that the USB data pins are correctly routed to any embedded USB devices or secondary hub tiers. Pay special attention to ensure that DC blocking/decoupling capacitors are placed on both USB3 differential pairs, and that USB3 transmitters are connected to receivers (i.e., not transmitter to transmitter, and not receiver to receiver).		
	Section 4.6, "Disabling Downstream Ports"	If any of the USB ports are unused, ensure they are properly disabled via pin strap. If pin strapping is not used, other methods may be used such as I^2C/SMBus configuration or OTP configuration.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
	Section 4.7, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB2 trace. Protection devices on USB3 traces should not add more than 0.5 pF on each line.		
Section 5.0, "USB Connectors"	Section 5.1, "Upstream Port VBUS and VBUS_DET"	Verify that the upstream port VBUS has no more than 10 µF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub. If the upstream port implements USB Power Delivery and VBUS may exceed 5V, then the **VBUS_DET** should be controlled directly from the upstream port Power Delivery controller device, not connected directly to VBUS.		
	Section 5.2, "Downstream Port VBUS and PRT_CTLx Connections for Standard Type-A Ports"	Verify that for any downstream Type-A ports, the **PRT_CTLx** pins are properly connected to both the 'Enable' pin of the downstream port power controller and the Fault indicator output of the port power controller. Ensure the port power controller current capability is sized appropriately (500 mA, 900 mA, 1.5A, or 3A), and that the overcurrent threshold is set appropriately.		
	Section 5.3, "Downstream Port VBUS and PRTCTLx Connections for Type-C Ports"	Verify that for any downstream Type-C ports, the **PRT_CTLx** pins are properly connected to both the 'Enable' pin of the downstream Type-C port controller and the Fault indicator output of the port switch or DC/DC regulator. Ensure the port power controller current capability is sized appropriately for the selected settings of the Type-C port power controller.		
	Section 5.4, "Type-C Port Control"	Ensure that a suitable external Type-C controller is selected and implemented such that the control mode configuration pins, **CC_POL** and **ALT_MUX_EN**, properly match the control behavior of the Type-C controller that drives the **AB0x/ATTACHMUXxA** and **C_ATTACHx/ATTACHMUXxB** signals.		
	Section 5.5, "GND and EARTH Recommendations"	Verify that the USB connector is properly connected to PCB ground on both the GND pins and the SHIELD pins. It is recommended that an RC filter be placed in between the SHIELD pins and PCB ground.		
Section 6.0, "Clock Circuit"	Section 6.1, "Crystal or External Clock Connection"	Confirm the crystal or clock is 25.000 MHz (±50 ppm). If a single-ended clock is used, ensure it is connected to **XTALI** while leaving **XTALO** floating. If a crystal is used, ensure the loading capacitors are appropriately sized for the crystal loading requirement.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Power and Startup"	Section 7.1, "RBIAS Resistor"	Confirm that a 12.0 kΩ 1% resistor is connected between the **RBIAS** pin and PCB ground.		
	Section 7.2, "Board Power Supplies"	Verify that the board power supplies deliver 3.0V to 3.6V, and 1.08V to 1.32V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet. If the rise time requirement cannot be met, ensure that the **RESET_N** line is held low until the power regulators reach a steady state.		
	Section 7.3, "Reset Circuit"	Ensure that the **RESET_N** signal has an external pull-up resistor, or is otherwise properly controlled by an external SOC, MCU, or Reset supervisor device.		
Section 8.0, "External SPI Memory"	Section 8.1, "SPI Operation Summary"	Determine if a custom SPI FW image is required, and which mode of operation the selected SPI Flash device must support.		
	Section 8.2, "Compatible SPI Flash Devices"	Ensure that the selected SPI Flash device is compatible with the hub.		
	Section 8.3, "SPI Connection Diagrams"	Verify that the SPI Flash device is connected according to the diagram in Figure 8-1. Follow Figure 8-2 if no SPI Flash device is connected in the design.		
Section 9.0, "Miscellaneous"	Section 9.1, "GPIOs"	Verify that any GPIO pins that will be used as GPIOs within the application are connected properly, and never exceed the voltage maximums/minimums or overload the current source/sink maximums as defined in the hub data sheet.		
	Section 9.2, "I2C/SMBus Connections" (Depending on design)	If the USB-to-I^2C/SMBus slave interface is implemented, ensure that appropriate pull-up resistors are connected and that the connections to the I^2C/SMBus master are correct. Note that pull-up resistors are detected on the I^2C/SMBus slave interface, the USB hub will not enumerate to a USB host until it receives the special “Attach” command from the I^2C/SMBus master.		
		If the USB-to-I^2C/SMBus Bridge feature is implemented, ensure that appropriate pull-up resistors are applied within the system only after the hub initialization and that the connections to the I^2C/SMBus slave devices are correct. Verify that all slave devices have a different I^2C/SMBus address. Verify that the hub and all slave devices can support the targeted bus speed.		
	Section 9.3, "FlexConnect"	If using the FlexConnect feature, refer to *AN1700 - FlexConnect Applications* and contact Microchip support for design and implementation assistance.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
	Section 9.4, "Non-Removable Port Settings"	Verify that the **CFG_NON_REM** configuration strap is set per application requirements.		
	Section 9.5, "Self-Powered/Bus-Powered Settings"	Verify the application requirements for Self-Powered or Bus-Powered operation. If Self-Powered operation is required, then no additional configuration or circuitry is required. If Bus-Powered operation is required, then the hub must be configured via OTP or I^2C/SMBus.		
	Section 9.6, "Battery Charging Settings"	Verify that the **CFG_BC_EN** configuration strap is set per application requirements.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004195C (03-21-25)	Figure 4-1, Figure 4-2, and Figure 4-3	Updated drawing to add 0.33 µF capacitors to the RX pins.
DS00004195B (11-30-23)	Figure 4-1	Corrected connections of upstream USB port signals.
DS00004195A (09-17-21)	Initial release	

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