PIC18(L)F25/26K83 Family Silicon Errata and Data Sheet Clarifications

PIC18(L)F25/26K83

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Introduction

The PIC18(L)F25/26K83 devices that you have received conform functionally to the current device data sheet (DS40001943**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18(L)F25/26K83 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		A2	A3
PIC18F25K83	0x6EE0	0xA002	0xA003
PIC18LF25K83	0x6F20	0xA002	0xA003
PIC18F26K83	0x6EC0	0xA002	0xA003
PIC18LF26K83	0x6F00	0xA002	0xA003

Important: Refer to the **Device/Revision ID** section in the device data sheet for more detailed information on Device Identification and Revision IDs for your specific device.

Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				A2	A3
Electrical Specifications	SMBus 3.0	1.1.1	SMBus 3.0 logic levels	X	X
	FVR Accuracy	1.1.2	FVR output voltage may be higher than specified in the data sheet	X	X
Direct Memory Access (DMA)	DMA in Doze Mode	1.2.1	DMA transfers may not work when the CPU is in Doze mode	X	
Analog-to-Digital Converter with Computation (ADCC)	Burst Average Mode	1.3.1	ADCC Burst Average Mode	X	
Nonvolatile Memory (NVM) Control	NVM Write Error	1.4.1	NVM Write Error (WRERR) bit is incorrectly set	X	
Windowed Watchdog Timer (WWDT)	WWDT Operation in Doze Mode	1.5.1	Window violation occurs when the WWDT is operated in Doze mode	X	
Power-Saving Operation Modes	Low-Power Sleep Mode	1.6.1	Low-Power Sleep mode does not operate at 3.1V < V_{DD} < 3.3V in PIC18**F**25/26K83 devices	X	
Program Flash Memory (PFM)	Endurance of PFM Cell for LF Devices	1.7.1	Endurance of the PFM cell is lower than specified in PIC18**LF**25/26K83 devices	X	X
In-Circuit Debugging (ICD)	Software Breakpoints	1.8.1	Software breakpoints are not available	X	X
Inter-Integrated Circuit (I^2C)	I^2C Start/Stop Flags	1.9.1	The I^2C Start and/or Stop flags may be set when I^2C is enabled	X	X
Instruction Set	`PUSHL` Instruction	1.10.1	The PUSHL instruction incorrectly executes	X	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Electrical Specifications

1.1.1 SMBus 3.0 Logic Levels

The SMBus 3.0 V_{IL} specification (Parameter D305) is temperature and V_{DD} dependent. Refer to the table below.

Temperature	V_{DD}	D305 SMBus 3.0 V_{IL} Specification
-40°C	1.8V	0.6V
-40°C	5.5V	0.8V
25°C	1.8V	0.6V
25°C	5.5V	0.8V
85°C	1.8V	0.6V
85°C	5.5V	0.6V
125°C	1.8V	0.5V
125°C	5.5V	0.6V

Work around

None.

Affected Silicon Revisions

A2	**A3**						
X	**X**						

1.1.2 FVR Output Voltage May Be Higher Than Specified in the Data Sheet

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This applies to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are:

- FVR01 (1X gain setting)
- FVR02 (2X gain setting)
- FVR03 (4X gain setting)

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A2	**A3**						
X	**X**						

1.2 Module: Direct Memory Access (DMA)

1.2.1 DMA Transfers May Not Work When the CPU is in Doze Mode

When the CPU is operated in Doze mode, DMA transfers may not work as expected.

Work around

None.

Affected Silicon Revisions

A2	**A3**						
X							

1.3 Module: Analog-to-Digital Converter with Computation (ADCC)

1.3.1 ADCC Burst Average Mode

When the ADCC is operated in Burst Average mode (MD = `0b011` in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = `0` in the ADCON0 register and DSEN = `1` in the ADCON1 register), the value in the ADCNT register does not increment beyond '`0b1`' toward the value in the ADRPT register.

Work around

When operating the ADCC in Burst Average mode with double-sampling, enable continuous module operation (CONT = `1` in the ADCON0 register) and set the Stop-on-Interrupt bit (SOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and retrigger ADCC as necessary.

Alternatively, if the CPU is in Low-Power Sleep mode, the ADCC in non-continuous Burst Average mode can be operated with a single ADC conversion (DSEN = `0` in the ADCON1 register). Doing so compromises noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A2	**A3**						
X							

1.4 Module: Nonvolatile Memory (NVM) Control

1.4.1 NMV Write Error (WRERR) Bit is Incorrectly Set

If a Reset occurs while a self-write operation is in progress, the Write Error (WRERR) bit is set. If the user clears the WRERR bit and another Reset occurs, even though no self-write operation is in progress, the WRERR bit will be incorrectly set again since the internal write latch has not been cleared.

Work around

A successful write operation will clear the WRERR condition.

Affected Silicon Revisions

A2	**A3**						
X							

1.5 Module: Windowed Watchdog Timer (WWDT)

1.5.1 Window Violation Occurs When the WWDT is Operated in Doze Mode

When the `CLRWDT` instruction is issued in Doze mode, a window violation error occurs even though the window is open and armed.

Work around

Do not operate the WWDT in Doze mode.

Affected Silicon Revisions

A2	**A3**						
X							

1.6 Module: Power-Saving Operation Modes

1.6.1 Low-Power Sleep Mode Does Not Operate at 3.1V < V_{DD} < 3.3V in PIC18F25/26K83 Devices

PIC18F25/26K83 devices reset when waking up from Sleep while in Low-Power mode (VREGPM = `1` in the VREGCON register) at 3.1V < V_{DD} < 3.3V.

Work around

Method 1:

If wake-up from Sleep is needed at 3.1V < V_{DD} < 3.3V, operate the device in Normal Power mode (VREGPM = `0`).

Method 2:

If wake-up from Sleep is needed at 3.1V < V_{DD} < 3.3V, enable the Fixed Voltage Reference (EN = `1` in the FVRCON register). This method increases the current in Sleep mode by typically 7 µA.

Affected Silicon Revisions

A2	**A3**						
X							

1.7 Module: Program Flash Memory (PFM)

1.7.1 Endurance of the PFM Cell is Lower than Specified in PIC18LF25/26K83 Devices

The Program Flash Memory (PFM) cell endurance specification (Electrical Specification Parameter MEM30) for PIC18LF25/26K83 devices is 1k cycles.

Work around

None.

Affected Silicon Revisions

A2	**A3**						
X	**X**						

1.8 Module: In-Circuit Debugging (ICD)

1.8.1 Software Breakpoints Are Not Available

When debugging code, software breakpoints will not be available.

Work around

None.

Affected Silicon Revisions

A2	**A3**						
X	**X**						

1.9 Module: Inter-Integrated Circuit (I^2C)

1.9.1 The I^2C Start and/or Stop Flags May Be Set When I^2C Is Enabled

When I^2C is enabled, erroneous Start and/or Stop conditions may be detected. This can generate erroneous I^2C interrupts if enabled.

Work around

Use the following procedure to correctly detect the Start and Stop conditions:

1. Disable the Start and Stop conditions interrupt functions.
2. Enable the I^2C module.
3. Wait 250 ns + six instruction cycles ($F_{OSC}/4$).
4. Clear the Start and Stop conditions interrupt flags.
5. Enable the Start and Stop conditions interrupt functions if used.

```
I2CxPIEbits.SCIE = 0;         // Disable Start condition interrupt
I2CxPIEbits.PCIE = 0;         // Disable Stop condition interrupt
I2CxCON0bits.EN = 1;          // Enable I2C
Delay();                      // Wait for 250 ns + 6 instruction cycles (FOSC/4)
I2CxPIRbits.SCIF = 0;         // Clear the Start condition interrupt flags
I2CxPIRbits.PCIF = 0;         // Clear the Stop condition interrupt flags
I2CxPIEbits.SCIE = 1;         // Enable Start condition interrupt if used
I2CxPIEbits.PCIE = 1;         // Enable Stop condition interrupt if used
```

Affected Silicon Revisions

A2	**A3**						
X	**X**						

1.10 Module: Instruction Set

1.10.1 The `PUSHL` Instruction Incorrectly Executes

The `PUSHL` instruction of the PIC18 Extended Instruction Set incorrectly executes when FSR2 is loaded with certain values.

Work around

Do not use `PUSHL` when FSR2 is loaded with any of the following values:

- 0xDB
- 0xDC
- 0xDE
- 0xE3
- 0xE4
- 0xE6
- 0xEB
- 0xEC
- 0xEE

Affected Silicon Revisions

A2	**A3**						
X	**X**						

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001943**C**):

Note:
Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 DS Clarification: Nonvolatile Memory (NVM) Control

Section 13.2 incorrectly states the writing access for User IDs. The corrected Section 13.2 is shown below with changes highlighted in **bold**:

13.2.2 Writing Access

Only the User IDs and CONFIG words have write access enabled. The user can write to these blocks by setting the REG bits to `'b01` or `'b11`. The WREN bit in NVMCON1 must be set to enable writes. This prevents accidental writes to the CONFIG words due to errant (unexpected) code execution. The WREN bit should be kept clear at all times, except when updating the CONFIG words. The WREN bit is not cleared by hardware. The WR bit will be inhibited from being set unless the WREN bit is set.

13.2.2.1 Writing to User IDs

The user needs to load the TBLPTR and TABLAT registers with the address and data byte respectively. **Writing to the User IDs does not include an implicit erase cycle like the EEPROM/CONFIG words; hence, the user needs to clear the memory location pointed by TBLPTR, first by setting the FREE bit and executing the write command.** An unlock sequence is required before setting the **writing command. A single User ID byte is cleared at once (set to `0xFF`). CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set and the CPU resumes operation.**

Once the User ID byte is cleared, the user can now write the new value to that location. To do this, the user needs to execute the TBLWT instruction, followed by executing the write command. An unlock sequence is required before setting the write command. A single User ID byte is written at once. CPU execution is stalled and, at the completion of the write cycle, the WR bit is cleared in hardware and the NVM Interrupt Flag bit (NVMIF) is set. The new User ID value takes effect when the CPU resumes operation.

During the above operations, if TBLPTR points to an invalid address location (see Table 13-1), the WR bit is cleared without any effect and WRERR is set.

2.2 Electrical Specifications

Table 45-11 incorrectly states values for RST06 and RST09. The corrected values are shown below with changes highlighted in **bold**:

Table 2-1. TABLE 45-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions
RST01*	T_{MCLR}	$\overline{MCLR}$ Pulse Width Low to Ensure Reset	2	—	—	µs	
RST02*	T_{IOZ}	I/O High-Impedance from Reset Detection	—	—	2	µs	
RST03	T_{WDT}	Watchdog Timer Time-out Period	—	16	—	ms	1:512 Prescaler

Table 2-1. TABLE 45-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS (continued)

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions
RST04*	T_{PWRT}	Power-up Timer Period	— — —	1 16 64	— — —	ms ms ms	PWRTS = 'b00 PWRTS = 'b01 PWRTS = 'b10
RST05	T_{OST}	Oscillator Start-up Timer Period(1,2)	—	1024	—	T_{OSC}	
RST06	V_{BOR}	Brown-out Reset Voltage(4)	2.7 2.55 2.3 2.3 1.8	2.85 2.7 2.45 2.45 1.9	3.0 2.85 2.6 2.6 **2.1**	V V V V V	BORV = 'b00 BORV = 'b01 BORV = 'b10 BORV = 'b11 (PIC18Fxxx) BORV = 'b11 (PIC18LFxxx)
RST07	V_{BORHYS}	Brown-out Reset Hysteresis	—	40	—	mV	
RST08	T_{BORDC}	Brown-out Reset Response Time	—	3	—	µs	
RST09	V_{LPBOR}	Low-Power Brown-out Reset Voltage	1.8	**2.0**	**2.5**	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Notes:

1. By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.
2. To ensure these voltage tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

3. Appendix A: Revision History

Doc Rev.	Date	Comments
G	03/2025	Updated the document format to the current Microchip publication standard, module numbers under silicon errata have been renumbered accordingly; added silicon issue 10.1.
F	02/2024	Data Sheet Clarifications: Added Module 2.
E	09/2021	Added Module 9.1: I^2C Start/Stop Flags.
D	02/2021	Added Module 8.1; Data Sheet Clarifications: Replaced previous Module 1 with new Module 1: Nonvolatile Memory (NVM) Control; other minor corrections.
C	01/2020	Removed Module 1.2, renumbered Module 1.3, updated Table 2; Data Sheet Clarifications: added Module 1.
B	02/2019	Added silicon revision A3; added Module 1.3: Fixed Voltage Reference (FVR) Accuracy, added Module 2: Direct Memory Access (DMA), Module 3: Analog-to-Digital Converter with Computation (ADC^2), Module 4: Nonvolatile Memory (NVM) Control, Module 5: Windowed Watchdog Timer (WWDT), Module 6: Power-Saving Operation Modes, and Module 7: Program Flash Memory.
A	011/2017	Initial release of this document.

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ISBN: 979-8-3371-0682-3

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