AVR32800: UC3L Schematic Checklist

Features

- **Power circuits**
- **Reset circuit**
- **Clock and crystal oscillators**
- **aWire™, JTAG and Nexus debug ports**
- **Capacitive Touch (CAT) Module**
- **Patents & Trademarks :**
  - **Atmel® QTouch® (patented charge-transfer method)**
  - **Atmel QMatrix™ (patented charge-transfer method)**

1 Introduction

A good hardware design comes from a proper schematic. Since UC3L devices have a fair number of pins and functions, the schematic for these devices can be large and quite complex.

This application note describes a common checklist which should be used when starting and reviewing the schematics for a UC3L design.

32-bit AVR® Microcontrollers

Application Note

Rev. 32129B-AVR32-06/10

2 Power circuit

2.1 Single 3.3 volt power supply

Figure 2-1. Single 3.3 volt power example schematic

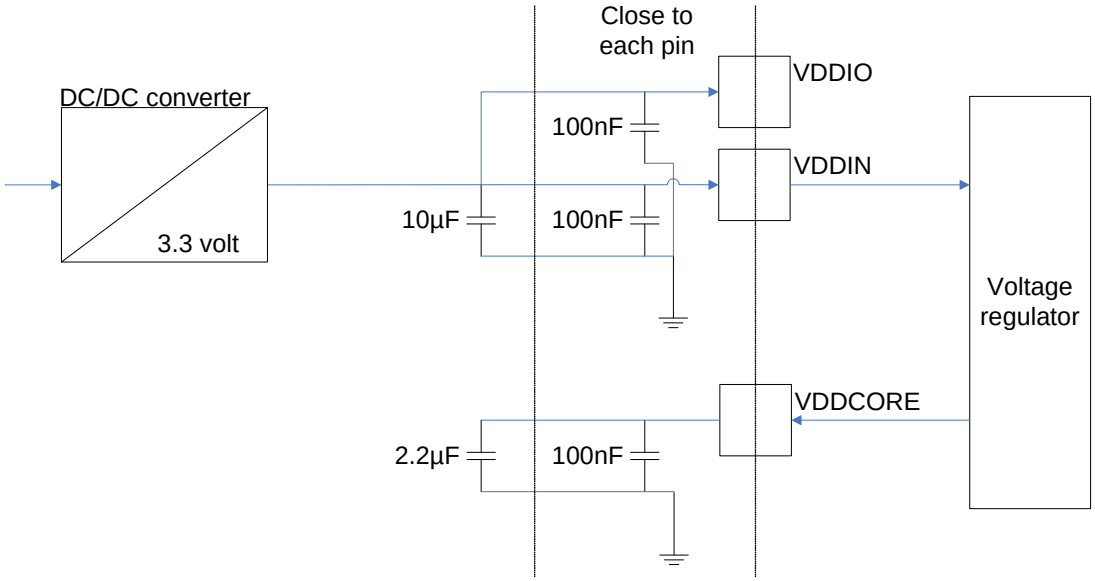

Table 2-1. Single 3.3 volt power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDIO	1.62 V to 3.6 V Decoupling/filtering capacitors 100 nF(1)(2) and 10 µF(1)	Powers I/O lines, OSC32K, RC32K, AST, wake, POR33 and SM33. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIN	1.98 V to 3.6 V Decoupling/filtering capacitors 100 nF(1)(2) and 10 µF(1)	Powers I/O lines and internal voltage regulator. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDCORE	Decoupling/filtering capacitors 100 nF(1)(2) and 2.2 µF(1)	Output of the on-chip 1.8V voltage regulator. Powers CPU, peripherals, memories, SCIF, BOD, RCSYS and DFLL. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.

Note 1: These values are given only as a typical example.

Note 2: Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

2.2 Single 1.8 volt power supply

Figure 2-2. Single 1.8 volt power example schematic

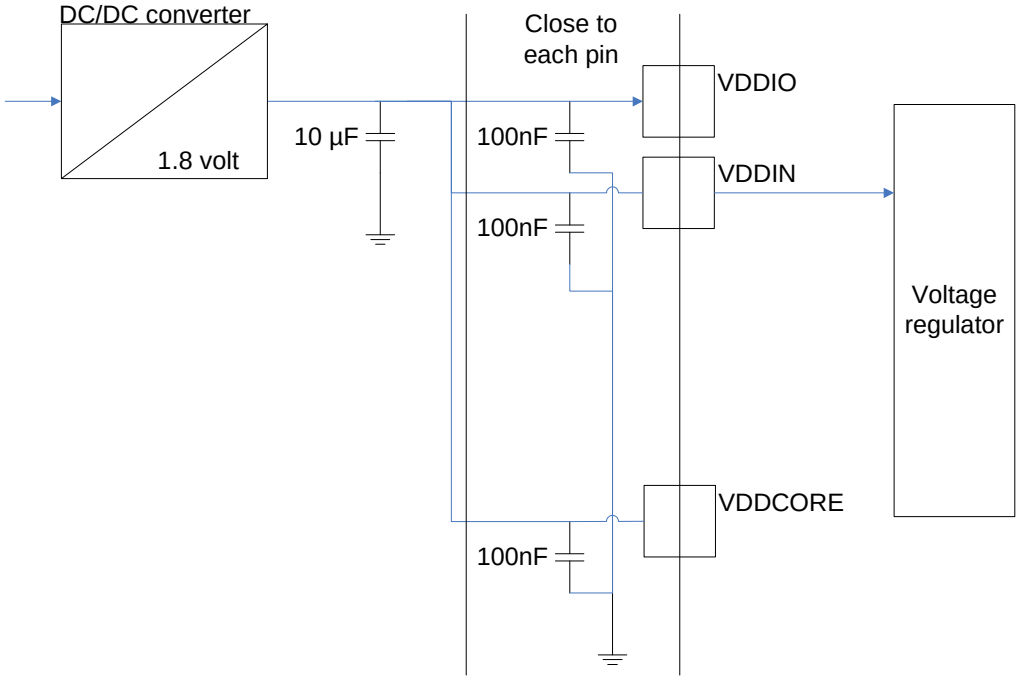

Table 2-2. Single 1.8 volt power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDIO	1.62 V to 1.98 V Decoupling/filtering capacitors 100 nF(1)(2) and 10 µF(1)	Powers I/O lines, OSC32K, RC32K, AST, wake, POR33 and SM33. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIN	1.62 V to 1.98 V Decoupling/filtering capacitors 100 nF(1)(2) and 10 µF(1)	Powers I/O lines, internal voltage regulator not in use. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDCORE	1.62 V to 1.98 V Decoupling/filtering capacitors 100 nF(1)(2) and 10 µF(1)	Powers CPU, peripherals, memories, SCIF, BOD, RCSYS and DFLL. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.

Note 1: These values are given only as a typical example.

Note 2: Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

2.3 Single 3.3 volt power supply with 1.8 V I/O lines

Figure 2-3. Single 3.3 volt power with 1.8 volt I/O lines example schematic

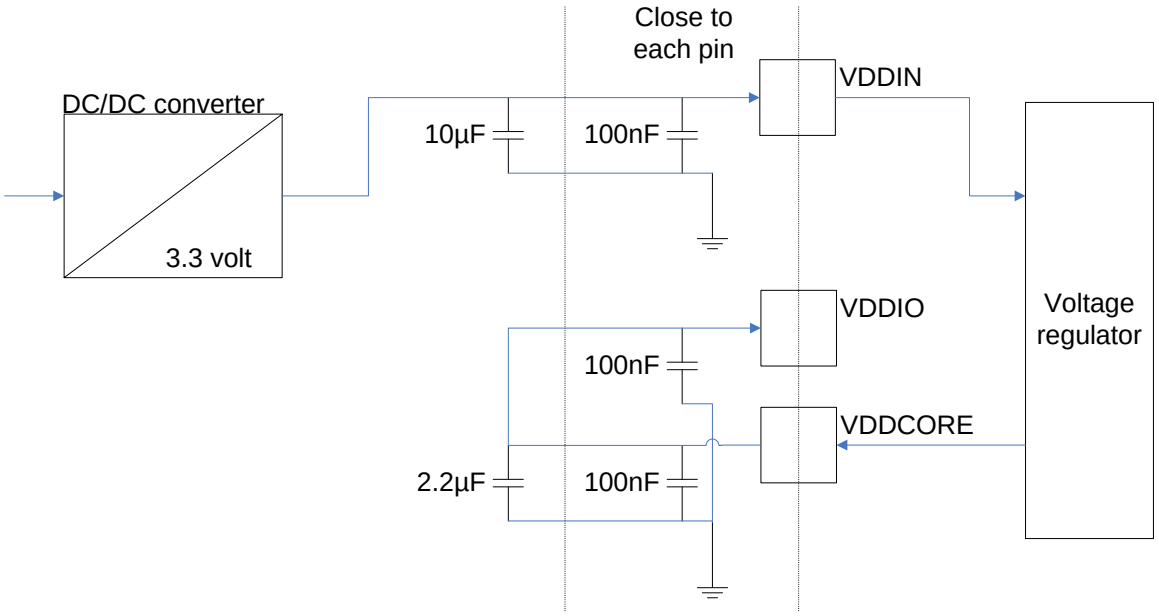

Table 2-3. Single 3.3 volt power supply with 1.8 volt I/O lines checklist

☑	Signal name	Recommended pin connection	Description
	VDDIO	Connected to VDDCORE. Decoupling/filtering capacitors 100 nF(1)(2) and 2.2 µF(1)	Powers I/O lines, OSC32K, RC32K, AST, wake, POR33 and SM33. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIN	1.98 V to 3.6 V Decoupling/filtering capacitors 100 nF(1)(2) and 10 µF(1)	Powers I/O lines and internal voltage regulator. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDCORE	Decoupling/filtering capacitors 100 nF(1)(2) and 2.2 µF(1)	Output of the on-chip 1.8V voltage regulator. Powers CPU, peripherals, memories, SCIF, BOD, RCSYS and DFLL. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop.

Note 1: These values are given only as a typical example.

Note 2: Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

2.4 ADC reference power supply

The following schematic checklist is mandatory even if the internal ADC is not in use.

Figure 2-4. ADC reference power supply example schematic

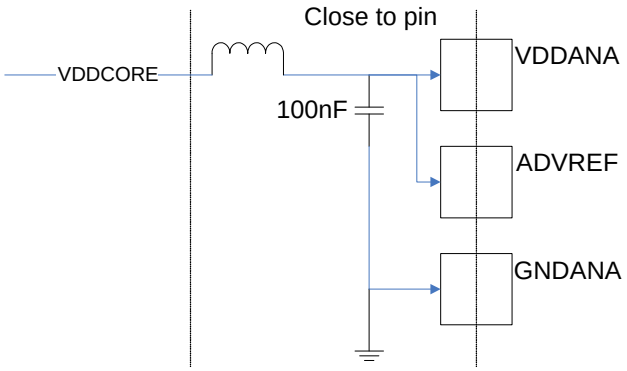

Table 2-4. ADC reference power supply checklist

☑	Signal name	Recommended pin connection	Description
	VDDANA	1.62 V to 1.98 V RF EMI inductor(3) Decoupling/filtering capacitor 100 nF(1)(2)	Powers the on-chip ADC, must always be powered since the analog multiplexer is powered by another domain. Decoupling/filtering capacitor must be added to improve startup stability and reduce source voltage drop.
	ADVREF	1.62 V to VDDANA Connect with VDDANA	ADVREF is a pure analog input.
	GNDANA	Connect to analog ground	

Note 1: These values are given only as a typical example.

Note 2: Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

Note 3: RF EMI inductor only needed if ADC is used in the design.

3 Reset circuit

Figure 3-1. Reset circuit example schematic

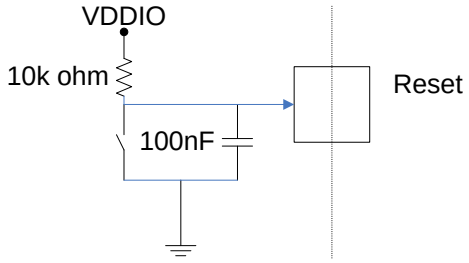

Table 3-1. Reset circuit checklist

☑	Signal name	Recommended pin connection	Description
	RESET[(1)]	Can be left unconnected in case no reset from the system needs to be applied to the product	The RESET_N pin is a Schmitt input and integrates a permanent pull-up resistor to VDDIO.

Note 1: RESET_N pin is used by aWire. Reset circuitry should be disabled when using RESET_N pin during aWire operation. Check section 5 of this document.

4 Clocks and crystal oscillators

4.1 External clock source

Figure 4-1. External clock source schematic

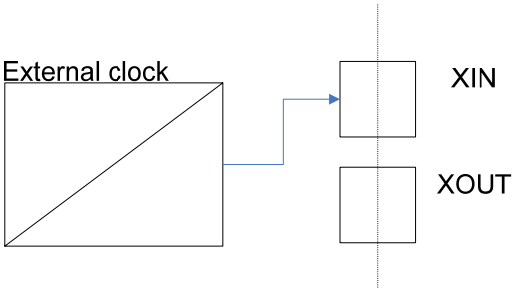

Table 4-1. External clock source checklist

☑	Signal name	Recommended pin connection	Description
	XIN	Connected to clock output from external clock source	Up to VDDIO volt square wave signal up to 50 MHz.
	XOUT	Can be left unconnected or used as GPIO	

4.2 Crystal oscillator

Figure 4-2. Crystal oscillator example schematic

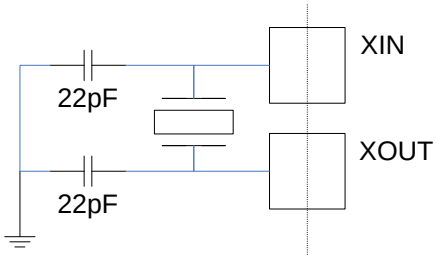

Table 4-2. Crystal oscillator checklist

☑	Signal name	Recommended pin connection	Description
	XIN	Biasing capacitor 22 pF[(1)(2)]	External crystal between 3 MHz and 16 MHz, powered by VDDIO.
	XOUT	Biasing capacitor 22 pF[(1)(2)]	Powered by VDDIO.

Note 1: These values are given only as a typical example. The capacitance C of the biasing capacitors can be computed based on the crystal load capacitance C_L and the internal capacitance C_i of the MCU as follows:

$C = 2 (C_L – C_i)$

The value of C_L can be found in the crystal datasheet and the value of C_i can be found in the MCU datasheet.

Note 2: Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

4.3 32 kHz Crystal oscillator

Figure 4-3. 32 kHz crystal oscillator example schematic

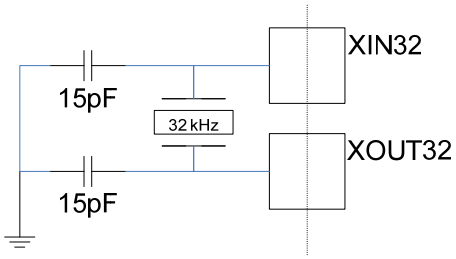

Table 4-3. 32 kHz crystal oscillator checklist

☑	Signal name	Recommended pin connection	Description
	XIN32	Biasing capacitor max 15 pF[(1)(2)]	External 32 kHz crystal.Primary (PA10) powered by VDDIO, Secondary (PA13- XIN32_2) powered by VDDIN.
	XOUT32	Biasing capacitor max 15 pF[(1)(2)]	Primary (PA12) powered by VDDIO, Secondary (PA20 – XOUT32_2) powered by VDDIN.

Note 1: These values are given only as a typical example. The capacitance C of the biasing capacitors can be computed based on the crystal load capacitance C_L and the internal capacitance C_i of the MCU as follows:

$C = 2 (C_L – C_i)$

The value of C_L can be found in the crystal datasheet and the value of C_i can be found in the MCU datasheet.

Note 2: Capacitor should be placed as close as possible to each pin in the signal group, vias should be avoided.

5 JTAG and Nexus debug ports

5.1 aWire port interface

Figure 5-1. aWire port interface example schematic

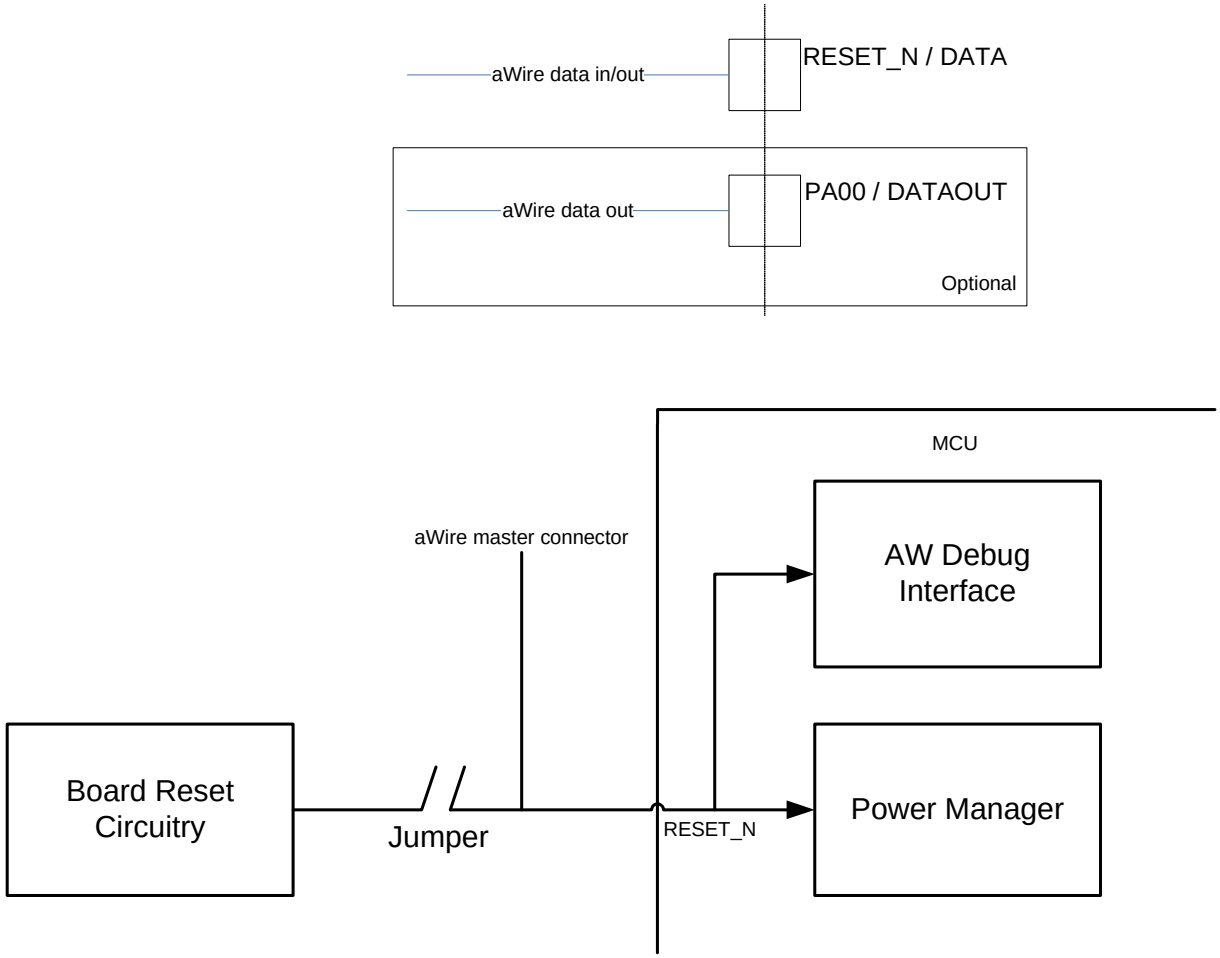

Table 5-1. aWire port interface checklist

☑	Signal name	Recommended pin connection	Description
	DATA	Connect to aWire DATA signal on external tool.	Device external reset line used for data input and output. Reset circuitry should be disabled as shown above when the RESET_N pin is used during aWire operation.
	DATAOUT	Optional, connect to aWire DATAOUT signal on external tool.	Data output is optional and only needed for aWire full duplex mode.

Note 1: The aWire needs an external pullup on the RESET_N pin to ensure that the pin is pulled up when the bus is not driven.

5.2 JTAG port interface

Figure 5-2. JTAG port interface example schematic

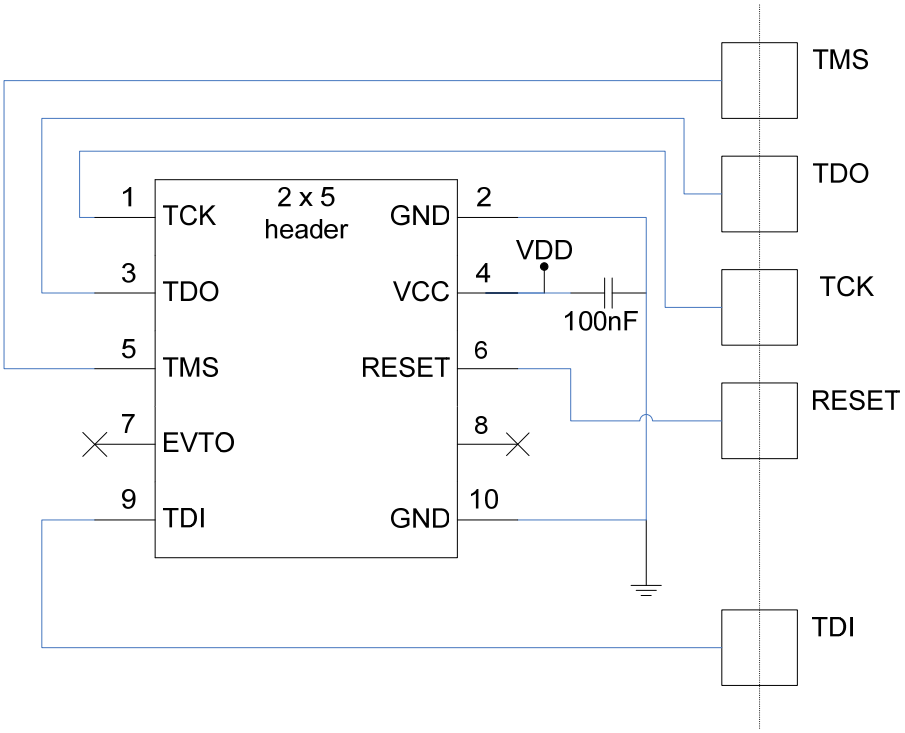

Table 5-2. JTAG port interface checklist

☑	Signal name	Recommended pin connection	Description
	TMS	PA01	Test mode select, sampled on rising TCK.
	TDO	PA02	Test data output, driven on falling TCK.
	TCK	PA00	Test clock, fully asynchronous to system clock frequency.
	RESET	RESET	Device external reset line.
	TDI	PA03	Test data input, sampled on rising TCK.
	EVTO		Event output, not used.

5.3 Nexus port interface

Figure 5-3. Nexus port interface example schematic

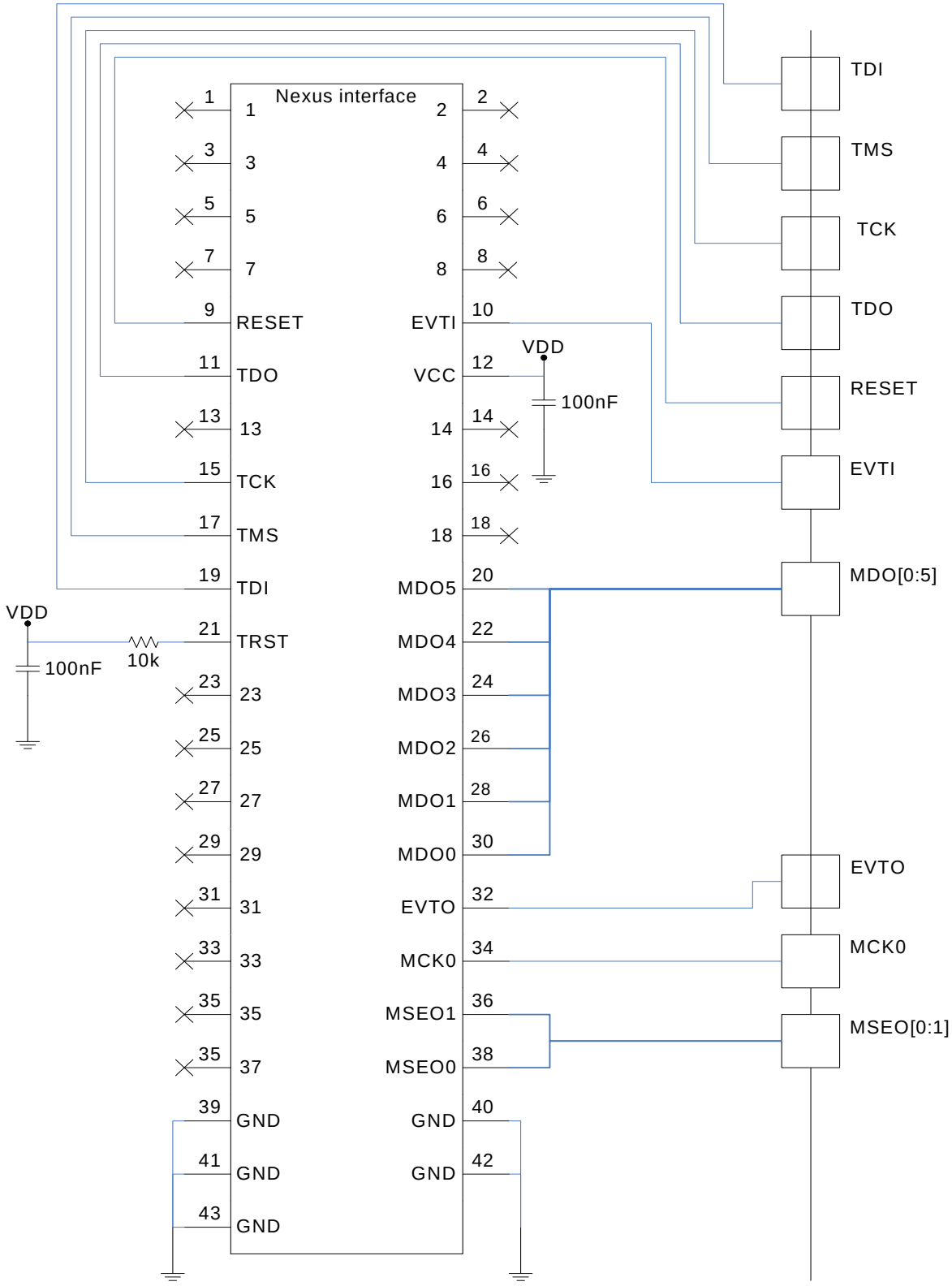

Table 5-3. Nexus port interface checklist

☑	Signal name	Recommended pin connection	Description
	TDI	PA03	Test data input, sampled on rising TCK.
	TMS	PA01	Test mode select, sampled on rising TCK.
	TCK	PA00	Test clock, fully asynchronous to system clock frequency.
	TDO	PA02	Test data output, driven on falling TCK.
	RESET	RESET	Device external reset line.
	EVTI(1)		Event input.
	MDO[0:5] (1)		Trace data output.
	EVTO	PA04	Event output.
	MCK0(1)		Trace data output clock.
	MSE[0:1] (1)		Trace frame control.

Note 1: Two different connections are possible based on the value of OCD AXS register. Please refer to MCU datasheet section Nexus OCD AUX Port Connections

6 Capacitive Touch (CAT) Module

6.1 QTouch

Figure 6-1. QTouch Typical connection

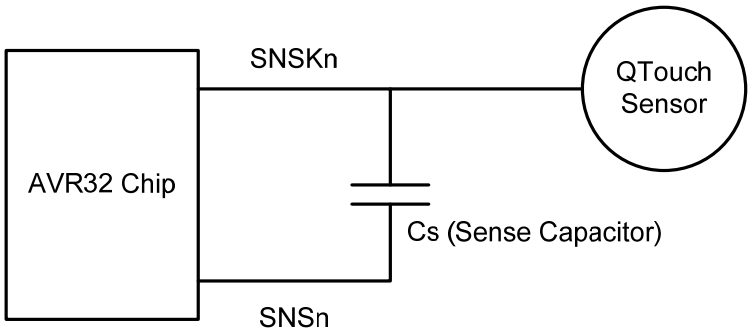

Table 6.1 QTouch Pin selection guide

☑	CAT module PIN name	PIN Name	QTouch Method Pin Name
	CSA0	PA13(5)	SNS0
	CSB0	PA18	SNSK0
	CSA1	PA01	SNS1
	CSB1	PA06	SNSK1
	CSA2	PA00	SNS2
	CSB2	PA07	SNSK2
	CSA3	PA02	SNS3
	CSB3	PA03	SNSK3
	CSA4	PA08(1)	SNS4
	CSB4	PA09(2)	SNSK4
	CSA5	PA10(3)	SNS5
	CSB5	PA12(4)	SNSK5
	CSA6	PA14	SNS6
	CSB6	PA15	SNSK6
	CSA7	PA04	SNS7
	CSB7	PA05	SNSK7
	CSA8	PA16	SNS8
	CSB8	PA17	SNSK8
	CSA9	PB00	SNS9

☑	CAT module PIN name	PIN Name	QTouch Method Pin Name
	CSB9	PB01	SNSK9
	CSA10	PA19	SNS10
	CSB10	PA22	SNSK10
	CSA11	PB03	SNS11
	CSB11	PB02	SNSK11
	CSA12	PA20(6)	SNS12
	CSB12	PB08	SNSK12
	CSA13	PB07	SNS13
	CSB13	PB06	SNSK13
	CSA14	PB04	SNS14
	CSB14	PB05	SNSK14
	CSA15	PB12	SNS15
	CSB15	PB09	SNSK15
	CSA16	PB11	SNS16
	CSB16	PB10	SNSK16

Note 1: This pin has an alternate function of XIN0
Note 2: This pin has an alternate function of XOUT0
Note 3: This pin has an alternate function of XIN32
Note 4: This pin has an alternate function of XOUT32
Note 5: This pin has an alternate function of XIN32_2
Note 6: This pin has an alternate function of XOUT32_2

6.2 QMatrix

There are three different ways of connecting QMatrix to the CAT module

1. Internal Current sources Disabled.
2. Internal Current sources Enabled with DICS.INTREFSEL= 0.
3. Internal Current sources Enabled with DICS.INTREFSEL= 1.

In all the three modes, Ra=10kohm, Rb=50ohm are recommended values. These two resistors should only be needed in some specialized applications (touch screens) where the sense capacitors are charged to low voltages (15 to 20 mV). In this case, we need to insure that the comparator threshold is 0 or slightly positive.

In a more typical QMatrix application with an array of buttons, the capacitors will be charged to 50 mV or more, and then a comparator offset of -15 mV is not a problem. In this case ACREFN can be grounded and it is unnecessary to use VDIVEN.

Figure 6-2 . QMatrix example schematic for Internal Current Sources Disabled

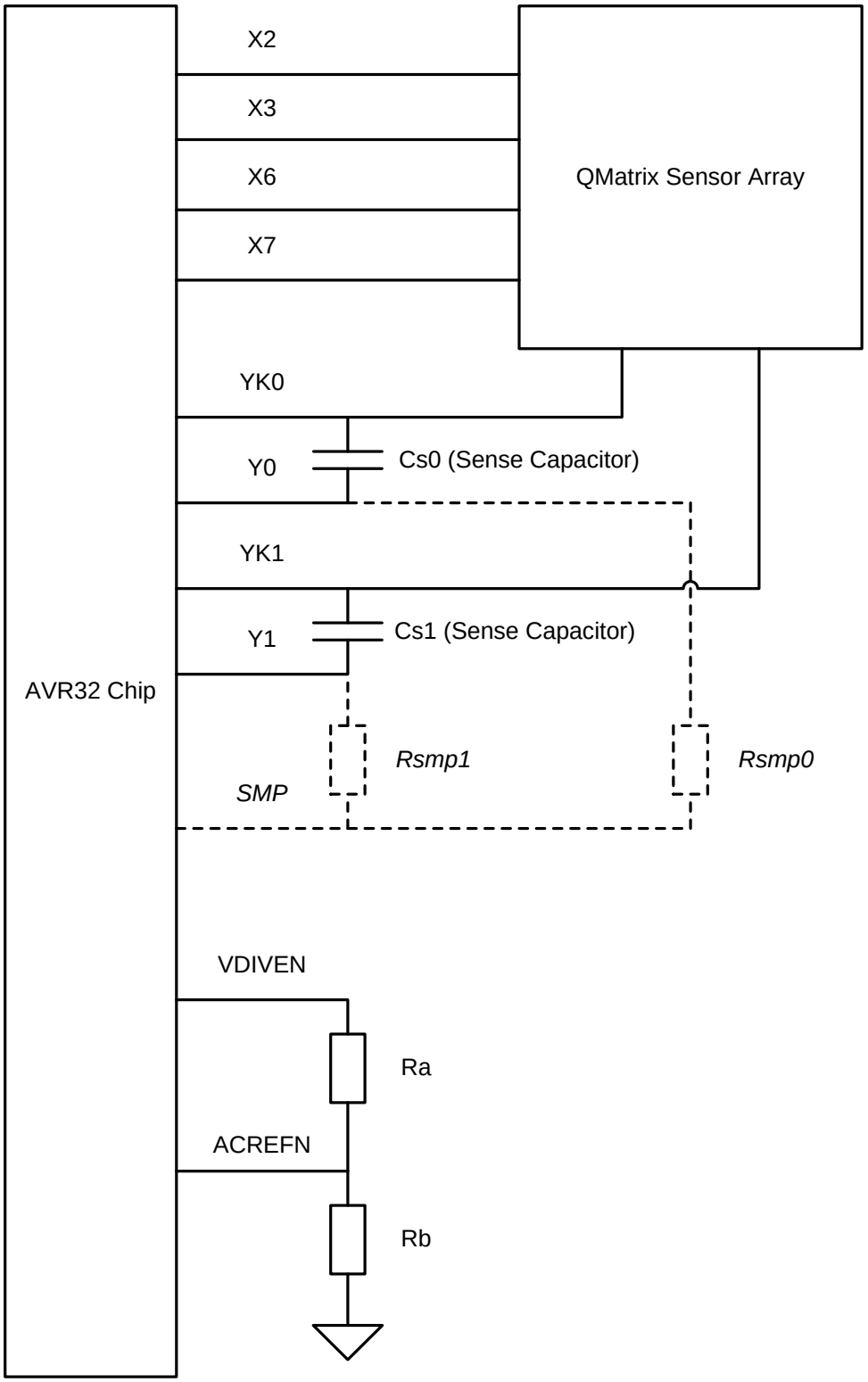

Table 6-2. Some of Maximum possible combination for QMatrix (Internal Current Sources Disabled).

☑	CAT module PIN name	PIN Name	QMatrix Method Pin Name	Internal Current Sources Disabled (Five different possible combination)					
				A	B	C	D	E	F
	CSA0	PA13[5]	X0	X0	SMP	X0	X0	X0	X0
	CSB0	PA18	X1	X1	X1	X1	X1	X1	X1
	CSA1	PA01	Y0	Y0	Y0	Y0	Y0	Y0	Y0
	CSB1	PA06	YK0	YK0	YK0	YK0	YK0	YK0	YK0
	CSA2	PA00	X2	X2	X2	X2	X2	X2	X2
	CSB2	PA07	X3	X3	X3	X3	X3	X3	X3
	CSA3	PA02	Y1	Y1	Y1	Y1	Y1	Y1	Y1
	CSB3	PA03	YK1	YK1	YK1	YK1	YK1	YK1	YK1
	CSA4	PA08[1]	X4	X4	X4	X4	X4	X4	X4
	CSB4	PA09[2]	X5	X5	X5	X5	X5	X5	X5
	CSA5	PA10[3]	Y2	Y2	Y2	Y2		Y2	Y2
	CSB5	PA12[4]	YK2	YK2	YK2	YK2	SMP	YK2	YK2
	CSA6	PA14	X6	X6	X6	X6	X6	SMP	X6
	CSB6	PA15	X7	X7	X7	X7	X7	X7	X7
	CSA7	PA04	Y3	Y3	Y3	Y3	Y3	Y3	Y3
	CSB7	PA05	YK3	YK3	YK3	YK3	YK3	YK3	YK3
	CSA8	PA16	X8	ACREFN	ACREFN	ACREFN	ACREFN	ACREFN	ACREFN
	CSB8	PA17	X9	SMP	X9	X9	X9	X9	X9
	CSA9	PB00	Y4	Y4	Y4	Y4	Y4	Y4	Y4
	CSB9	PB01	YK4	YK4	YK4	YK4	YK4	YK4	YK4
	CSA10	PA19	X10	X10	X10	X10	X10	X10	X10
	CSB10	PA22	X11	X11	X11	SMP	X11	X11	X11
	CSA11	PB03	Y5	Y5	Y5	Y5	Y5	Y5	Y5
	CSB11	PB02	YK5	YK5	YK5	YK5	YK5	YK5	YK5
	CSA12	PA20[6]	X12	X12	X12	X12	X12	X12	X12
	CSB12	PB08	X13	X13	X13	X13	X13	X13	X13
	CSA13	PB07	Y6	Y6	Y6	Y6	Y6	Y6	Y6
	CSB13	PB06	YK6	YK6	YK6	YK6	YK6	YK6	YK6
	CSA14	PB04	X14	X14	X14	X14	X14	X14	X14
	CSB14	PB05	X15	X15	X15	X15	X15	X15	X15
	CSA15	PB12	Y7	Y7	Y7	Y7	Y7	Y7	Y7
	CSB15	PB09	YK7	YK7	YK7	YK7	YK7	YK7	YK7
	CSA16	PB11	X16	X16	X16	X16	X16	X16	X16

☑	CAT module PIN name	PIN Name	QMatrix Method Pin Name	Internal Current Sources Disabled (Five different possible combination)					
				A	B	C	D	E	F
	CSB16	PB10	X17	X17	X17	X17	X17	X17	X17
		PA21							SMP

Note 1: This pin has an alternate function of XIN0
Note 2: This pin has an alternate function of XOUT0
Note 3: This pin has an alternate function of XIN32
Note 4: This pin has an alternate function of XOUT32
Note 5: This pin has an alternate function of XIN32_2
Note 6: This pin has an alternate function of XOUT32_2

Table 6-3. Some of Maximum possible combination for QMatrix with SYNC and DIVEN (Internal Current Sources Disabled).

☑	CAT module PIN name	PIN Name	QMatrix Method Pin Name	Table 6-2 "A" combination +SYNC					Table 6.2-1 "A" combination +VDIVEN
				I	J	K	L	M	
	CSA0	PA13(5)	X0	X0	X0	X0	X0	X0	X0
	CSB0	PA18	X1	X1	SYNC	X1	X1	X1	X1
	CSA1	PA01	Y0	Y0	Y0	Y0	Y0	Y0	Y0
	CSB1	PA06	YK0	YK0	YK0	YK0	YK0	YK0	YK0
	CSA2	PA00	X2	X2	X2	X2	X2	X2	X2
	CSB2	PA07	X3	X3	X3	X3	X3	X3	X3
	CSA3	PA02	Y1	Y1	Y1	Y1	Y1	Y1	Y1
	CSB3	PA03	YK1	YK1	YK1	YK1	YK1	YK1	YK1
	CSA4	PA08(1)	X4	X4	X4	X4	X4	X4	X4
	CSB4	PA09(2)	X5	X5	X5	X5	X5	X5	X5
	CSA5	PA10(3)	Y2	Y2	Y2	Y2	Y2	Y2	Y2
	CSB5	PA12(4)	YK2	YK2	YK2	YK2	YK2	YK2	YK2
	CSA6	PA14	X6	X6	X6	X6	X6	X6	X6
	CSB6	PA15	X7	SYNC	X7	X7	X7	X7	X7
	CSA7	PA04	Y3	Y3	Y3	Y3	Y3	Y3	Y3
	CSB7	PA05	YK3	YK3	YK3	YK3	YK3	YK3	YK3
	CSA8	PA16	X8	ACREFN	ACREFN	ACREFN	ACREFN	ACREFN	ACREFN
	CSB8	PA17	X9	SMP	SMP	SMP	SMP	SMP	SMP
	CSA9	PB00	Y4	Y4	Y4	Y4	Y4	Y4	Y4
	CSB9	PB01	YK4	YK4	YK4	YK4	YK4	YK4	YK4
	CSA10	PA19	X10	X10	X10	X10	X10	SYNC	X10
	CSB10	PA22	X11	X11	X11	X11	X11	X11	X11
	CSA11	PB03	Y5	Y5	Y5	Y5	Y5	Y5	Y5
	CSB11	PB02	YK5	YK5	YK5	YK5	YK5	YK5	YK5

☑	CAT module PIN name	PIN Name	QMatrix Method Pin Name	Table 6-2 "A" combination +SYNC					Table 6.2-1 "A" combination +VDIVEN
				I	J	K	L	M	
	CSA12	PA20[6]	X12	X12	X12	X12	X12	X12	X12
	CSB12	PB08	X13	X13	X13	SYNC	X13	X13	X13
	CSA13	PB07	Y6	Y6	Y6	Y6	Y6	Y6	Y6
	CSB13	PB06	YK6	YK6	YK6	YK6	YK6	YK6	YK6
	CSA14	PB04	X14	X14	X14	X14	X14	X14	X14
	CSB14	PB05	X15	X15	X15	X15	X15	X15	X15
	CSA15	PB12	Y7	Y7	Y7	Y7	SYNC	Y7	Y7
	CSB15	PB09	YK7	YK7	YK7	YK7		YK7	YK7
	CSA16	PB11	X16	X16	X16	X16	X16	X16	VDIVEN
	CSB16	PB10	X17	X17	X17	X17	X17	X17	X17

Note 1: This pin has an alternate function of XIN0

Note 2: This pin has an alternate function of XOUT0

Note 3: This pin has an alternate function of XIN32

Note 4: This pin has an alternate function of XOUT32

Note 5: This pin has an alternate function of XIN32_2

Note 6: This pin has an alternate function of XOUT32_2

Figure 6-3. Qmatrix example schematic for Internal Current Sources Enabled with DICS.INTREFSEL= 0 and DICS.INTREFSEL= 1

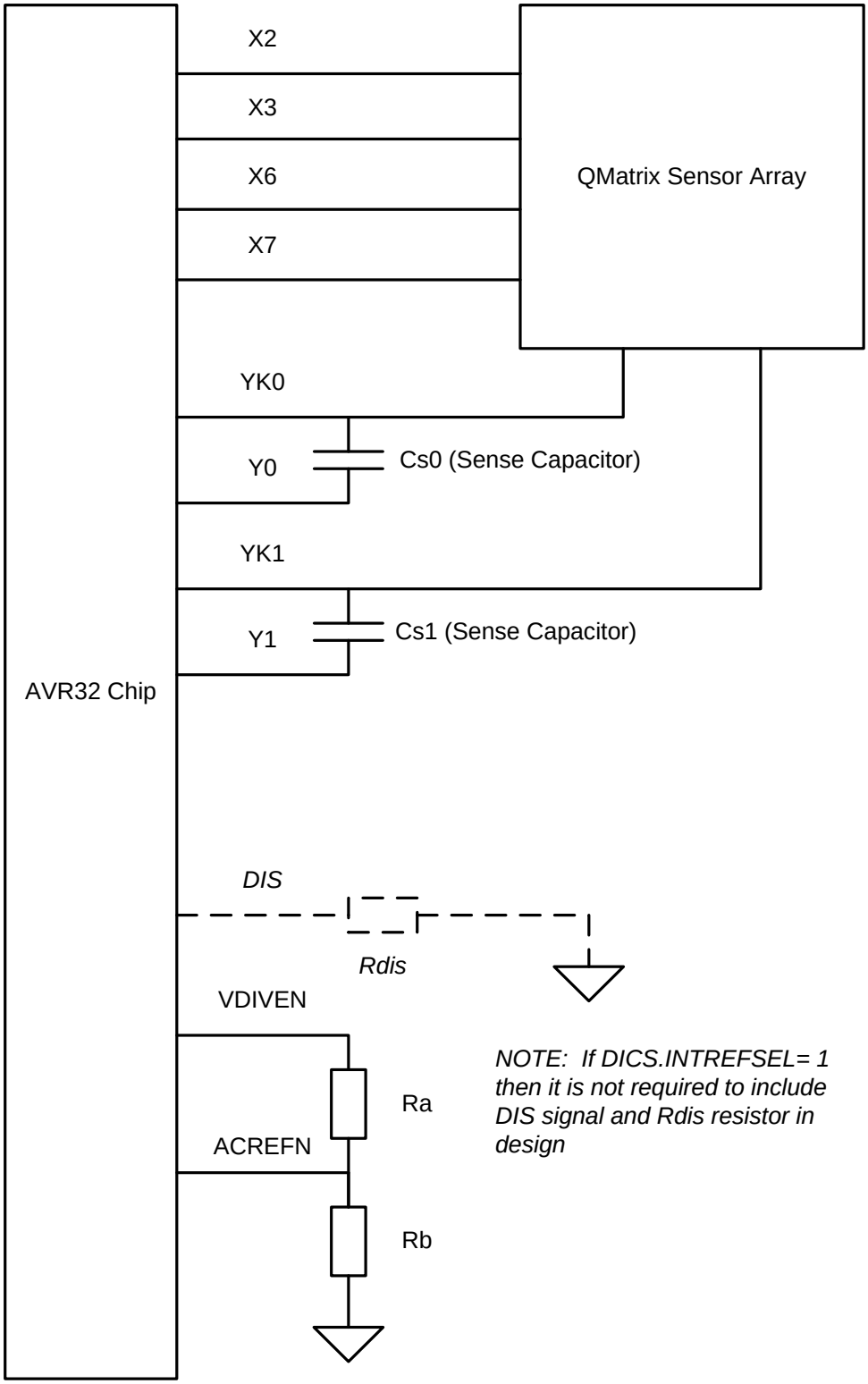

Table 6-4. Some of Maximum possible combination for QMatrix (Internal Current sources Enabled) with DICS.INTREFSEL= 0 and DICS.INTREFSEL= 1.

☑	CAT module PIN name	PIN Name	QMatrix Method Pin Name	DICS.INTREFSEL= 0	DICS.INTREFSEL= 1
	CSA0	PA13(5)	X0	X0	X0
	CSB0	PA18	X1	X1	X1
	CSA1	PA01	Y0	Y0	Y0
	CSB1	PA06	YK0	YK0	YK0
	CSA2	PA00	X2	X2	X2
	CSB2	PA07	X3	X3	X3
	CSA3	PA02	Y1	Y1	Y1
	CSB3	PA03	YK1	YK1	YK1
	CSA4	PA08(1)	X4	X4	X4
	CSB4	PA09(2)	X5	X5	X5
	CSA5	PA10(3)	Y2	Y2	Y2
	CSB5	PA12(4)	YK2	YK2	YK2
	CSA6	PA14	X6	X6	X6
	CSB6	PA15	X7	X7	X7
	CSA7	PA04	Y3	Y3	Y3
	CSB7	PA05	YK3	YK3	YK3
	CSA8	PA16	X8	ACREFN	ACREFN
	CSB8	PA17	X9	DIS	X9
	CSA9	PB00	Y4	Y4	Y4
	CSB9	PB01	YK4	YK4	YK4
	CSA10	PA19	X10	X10	X10
	CSB10	PA22	X11	X11	X11
	CSA11	PB03	Y5	Y5	Y5
	CSB11	PB02	YK5	YK5	YK5
	CSA12	PA20(6)	X12	X12	X12
	CSB12	PB08	X13	X13	X13
	CSA13	PB07	Y6	Y6	Y6
	CSB13	PB06	YK6	YK6	YK6
	CSA14	PB04	X14	X14	X14
	CSB14	PB05	X15	X15	X15
	CSA15	PB12	Y7	Y7	Y7
	CSB15	PB09	YK7	YK7	YK7
	CSA16	PB11	X16	X16	X16
	CSB16	PB10	X17	X17	X17

Note 1: This pin has an alternate function of XIN0

Note 2: This pin has an alternate function of XOUT0

☑	CAT module PIN name	PIN Name	QMatrix Method Pin Name	DICS.INTREFSEL= 0	DICS.INTREFSEL= 1

Note 3: This pin has an alternate function of XIN32

Note 4: This pin has an alternate function of XOUT32

Note 5: This pin has an alternate function of XIN32_2

Note 6: This pin has an alternate function of XOUT32_2

7 Resistive Touch Screen

Refer to "Resistive Touch Screen" of MCU data sheet for more details.

8 Miscellaneous Topics

8.1 I/O Line considerations

The device datasheet contains subsection " I/O Line Considerations" under section "Package and Pinout" .

8.2 Bootloader pin

If a pin is used to enter in the bootloader mode provided by the default bootloader programmed on all chips, that pin should be pulled-up or pulled-low depending on the chosen bootloader pin configuration.

9 Suggested reading

9.1 Device datasheet

The device datasheet contains block diagrams of the peripherals and details about implementing firmware for the device. The datasheet is available on http://www.atmel.com/AVR32 in the *Datasheets* section.

9.2 Touch design documents

Touch design documents contain the principles required for designing with Buttons, sliders and wheels. They are available on,

http://www.atmel.com/dyn/products/app_notes_v2.asp?family_id=697 .

9.3 Hardware – QT600

QT600 is a complete touch development kit for buttons, sliders and wheels. They are available on http://www.atmel.com/dyn/products/tools_card_v2.asp?tool_id=4658.

9.4 Hardware – STK600 Routing card for 48 pin AT32UC3L0 - STK600-RCUC3L0-34

STK600-RCUC3L0-34 is the correct Routing card for using with STK600. Schematics of same is available on http://www.atmel.com/dyn/resources/prod_documents/A09-0644_STK600-RCUC3L0-34_sch.PDF

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