VSC8574
User Guide
VSC8574 Evaluation Board

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 was published in April 2014. This revision includes changes regarding ZL30143 output drive compatibility and hyperlinks.

1.2 Revision 1.0

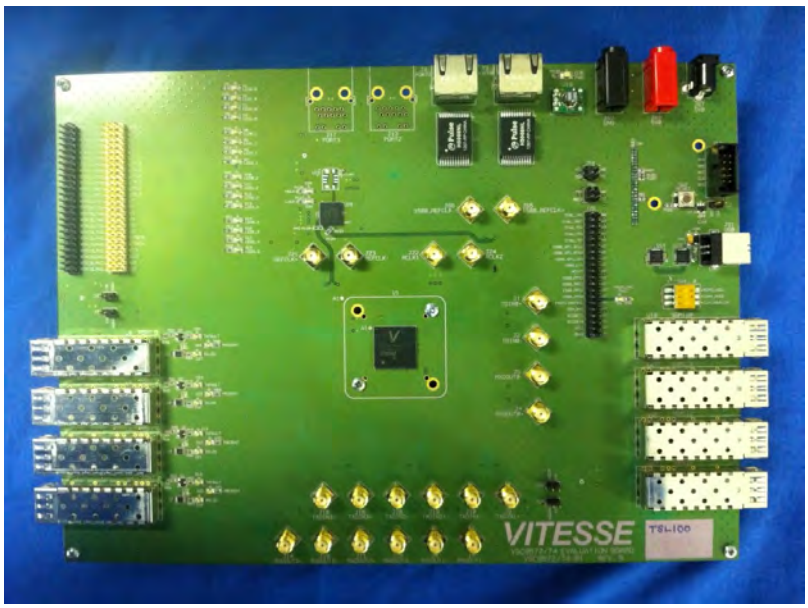
Revision 1.0 was the first release of this document. It was published in June 2012.

2 Introduction

The VSC8574 device is a low-power, quad-port Gigabit Ethernet transceiver with four SerDes interfaces for quad-port dual media capability. It also includes an integrated quad port I²C multiplexer (MUX) to control SFPs or PoE modules. The VSC8574 device also includes Vitesse's unique IEEE 1588 time-stamping engine with dual encapsulation support. It also includes dual recovered clock outputs to support Synchronous Ethernet applications.

This document describes the architecture and usage of the VSC8574 Evaluation Board (VSC8574EV). The VSC8574EV may be used to evaluate a family of devices which include the VSC8504, VSC8552, VSC8572, and VSC8574. These devices vary with respect to the number of ports, supported interfaces, and available features. This document specifically addresses the VSC8574 device. The Quick Start section describes how to bring-up the evaluation board along with install and run the graphical user interface (GUI), used to control the evaluation board.

Figure 1 • VSC8574EV Evaluation Board



2.1 References

The following reference documents provide additional information about the operation of the VSC8574 evaluation board.

- VSC8504 Datasheet
- VSC8552 Datasheet
- VSC8572 Datasheet
- VSC8574 Datasheet
- IEEE1588v2 and SyncE – Applications and Operation Using Vitesse's Synchronization Solution
- VSC8475 GUI
- VSC8574 Evaluation Board Schematic

3 General Description

The evaluation board (Figure 1) provides the user a way to evaluate the VSC8574 device in multiple configurations. Four RJ-45 connectors are provided for copper media interfaces. The four SFP cages allow for evaluation of the fiber media interconnects. The MAC interface is provided via SMA connectors or alternatively through SFP ports.

For access to all of the features of the device, an external microcontroller is used to configure the on-board clock chip via a two wire serial bus and the VSC8574 via the MDIO bus. The graphical user interface (GUI) enables the user to access the registers.

The evaluation board uses a Zarlink device to synthesize a 125MHz reference clock signal from a 20MHz crystal which serves as the REFCLK input.

3.1 Key Features

3.1.1 Copper Port RJ45 Connections

PHY Ports 2 and 3 use UDE RTA 1648BAK1A with integrated magnetic while PHY Ports 0 and 1 use generic RJ45 connectors with discrete Pulse H5008 magnetics.

3.1.2 SGMII/QSGMII MAC SMA

SGMII SMA connections are provided for all PHYs while the QSGMII SMA connection is available only on PHY0. Optional MAC side SFP port connections are provided for PHY0 and 3. To use these, 0 Ω resistors must be removed and re-installed on the board.

3.1.3 Switch Block Control

Set the SW1 switch as shown in the figure below.

Figure 2 • SW1 Switch Control

3.1.4 Zarlink ZL30143 SyncE G.8262/SETS

The Zarlink ZL30143 is initialized by default to provide a 125MHz differential LVPECL clock to the VSC8574 REFCLK inputs. The ZL30143 can be programmed to provide an LVDS differential clock in conjunction with an LVDS termination provided for REFCLK. See the Zarlink manual for output drive programming details. The ZL30143 can support synchronization with the VSC8574 PHY recovered clock for SyncE operation.

3.1.5 External 1588 Clock Option

The user may choose to provide an external 1588 REFCLK via SMA connections to J65 and J66. Zero ohm jumpers may need to be removed and or installed to connect via these clock inputs.

3.1.6 External RefClk Option

The user may choose to provide an external PHY REFCLK via SMA connections to J21 and J23. Zero Ohm jumpers may need to be removed and or installed to connect via these clock inputs.

3.1.7 Network Interface Microcontroller Card

A “Rabbit” microcontroller card is included to facilitate a software interface to the registers on the VSC8574. The controller card has a hard coded static IP address. See the label on the card for the value. This address is required by the user to initiate communications via the board and the GUI.

Note: The factory programmed Rabbit board IP address is 10.9.70.193.

4 Quick Start

4.1 Connecting the Power Supply

The evaluation board uses +5VDC to power the on-board regulators creating the +3.3V, +2.5V, and +1. 0V rails which drive the devices as well as modules. The evaluation board can be powered up using the power pack which provides the +5VDC. Simply plug the AC adaptor into a wall socket and the barrel end into J67 (see the upper right corner of Figure 1). Immediately the user should see several LEDs turn on.

The user may alternately connect the board to a bench style power supply by connecting the red banana plug to +5VDC and the black banana plug to ground. If the supply provides 3A the board should come alive as described above.

4.2 PC Software Installation

1. Download the ZIP file to the PC's root directory, normally C:\.
2. Extract to C:\
3. Double click the icon to launch the GUI (It is acceptable to drag the icon to the desktop)

4.3 Connecting the Board to the PC

The Rabbit board can interface with a PC either through a direct connection to the PC or if configured properly through a local area network. The latter option requires the user to configure the Rabbit's IP address so as to properly reside on the user's network.

The IP address of the board should be written on the Rabbit network interface daughter board card. The default value should be 10.9.70.193. You will need to use this IP address to initially access the board for operation or to change its IP address.

4.3.1 Changing the IP Address of the Board

1. Determine and write down the new unique IP address you wish to change the board to.
2. Directly connect an Ethernet cable from a PC to the Rabbit board.
   Note: Some older PCs do not support auto-crossover on the Ethernet connection so a cross-over cable may be needed.
3. Launch a DOS command window by clicking on the Start->Run button and typing "cmd".
4. Within the DOS command window type "Telnet"
5. In Telnet, connect to the Rabbit board's address using the open command by typing "open^10.9.70. XXX".
6. 10.9.70.xxx where xxx is the value on your board from the factory (typically 193).
7. You should have a prompt and be able to type help to get a list of commands available on the Rabbit.
   a. If you are unable to connect, then most likely you will need to change the IP address of the connected PC to have the first 3 octets similar to the board by following the subsequent steps.
   b. On the PC under Windows -> Control Panel → Network Connections → Local Area Connection, right mouse click for Properties. Under the General tab highlight Internet Protocol (TCP/IP) and click on Properties. From there enter the new PC IP address such as 10.9.70.yyy where yyy is a unique value and NOT the same as the Rabbit board. Once complete, return to step 4.
8. Command the board to change its IP address to the new one by typing into Telnet now connected to the board the command: set ip <new IP address> <Enter> where <new IP address> is in the form xxx. xxx.xxx.xxx. Once you hit <Enter> the IP address will be changed and the Rabbit will save the value and reboot which may take approximately 1 minute. The Telnet session will disconnect from the board.
9. Change your PC IP address to the same IP network as the Rabbit board.
10. Telnet to the Rabbit board.

11. Use the following commands to complete configuration of the Rabbit board:
    a. Set netmask xxx.xxx.xxx.xxx
    b. Set gateway xxx.xxx.xxx.xxx
    c. Save env
12. Please record and inform Vitesse of the new IP address of the board when you return so that Vitesse can connect to and reconfigure the board.
13. Re-label the Rabbit board with the new IP.

4.4 Using the Control Software

Connect the VSC8574EV Rabbit microcontroller RJ-45 directly to the PC or through a network switch if properly configured. Apply +5VDC to the EVB.

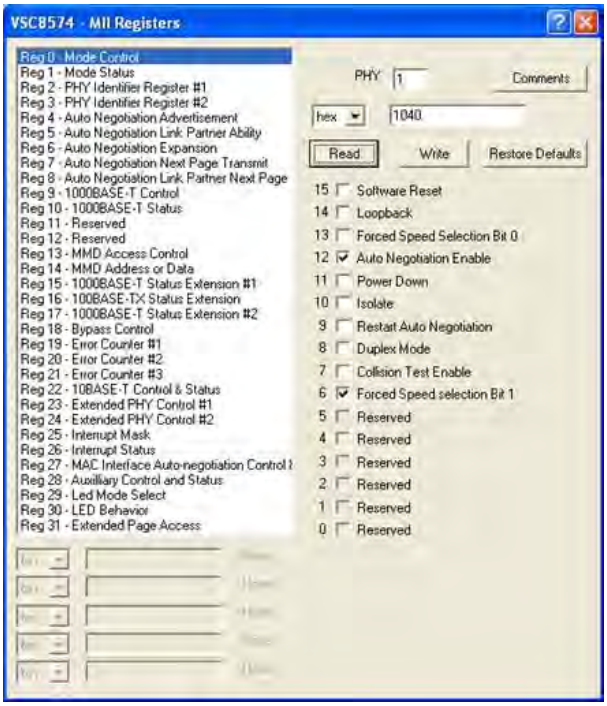
Launch the GUI by double-clicking the GUI shortcut located in C:\TeslaGUI_4_65 or on the desktop if it has been moved there. The GUI Connection window shown in Figure 3 should appear.

Figure 3 • GUI Connection Window

To make a connection to the EVB, click “Rabbit” and enter the IP address of the EVB, then click on “Connect”. The display next to the IP address window should change to “Connected”. If it does not, check the IP address, or your network configuration until connection with the EVB can be successfully established.

Double-click on “MII Registers” and the window shown in Figure 4 should appear:

Figure 4 • MII Registers GUI Window



Verify the device is up and running by reading MII Register 0. It should read back 0x1040. Reading back all 0’s or all 1’s indicates a problem. A checked box means the bit is set to “1”, if unchecked it is “0”.

4.4.1 Copper Media Operation (1000BASE-T)

A single register write and some external coax cables enables 1G Ethernet traffic to be received by the VSC8574 RJ-45 port, routed through the VSC8574 and externally via coax loopback cables through the SGMII interface and transmitted back to the traffic source on the same copper port. First configure the SerDes in SGMII mode by writing to Micro page 18’d. This is a global setting and does not need to be applied per port.

1. Set up the Copper traffic source (ie: IXIA or Smartbits)
2. Connect an Ethernet cable to an RJ-45 Port 0.
3. Connect two matched coax cables, J1 – J4 and J2 – J3.
4. Write using the “Micro Page Registers” window: 18’d 0x80F0.
5. When “Micro Page” 18’d is read back, bit 15 will clear.
6. Linkup bit is in MII Reg 1, bit 2 (MII 1.2), read twice to update

Traffic should be flowing.

4.4.2 Fiber Media Operation (100BASE-FX)

Follow all steps in section 2.53 with fiber media connection to (IXIA) and add the following steps.

1. Write using the “Micro Page Registers” window: 18’d 0x8FD1. (Global)
2. When “Micro Page” 18’d is read back, bit 15 will clear.
3. Write “MII Register” (PHY 0) 23’d 0x0304 (Sets Media Mode)
4. Write “MII Register” (PHY0) 0’d 0x9040 (SW Reset for media mode setting to have effect)

5. Write “Extended MII Register” (PHY0) 19’d 0x0001 (Flip SIGDET polarity if necessary)
6. Write “MII Register” (PHY0) 0’d 0x0004 (Disable Auto Neg if necessary)

4.4.3 Fiber Media Operation (1000BASE-X)

Follow all steps in section 3.4.1 with fiber media connection to (IXIA) and add the following steps.

1. Write using the “Micro Page Registers” window: 18’d 0x8FC1. (Global)
2. When “Micro Page” 18’d is read back, bit 15 will clear.
3. Write “MII Register” (PHY 0) 23’d 0x0204 (Sets Media Mode)
4. Write “MII Register” (PHY0) 0’d 0x9040 (SW Reset for media mode setting to have effect)
5. Write “Extended MII Register” (PHY0) 19’d 0x0001 (Flip SIGDET polarity if necessary)
6. Write “MII Register” (PHY0) 0’d 0x0004 (Disable Auto Neg if necessary)

Traffic should be flowing.

4.5 Useful Registers

4.5.1 Ethernet Packet Generator

ExtMII 29E is the Ethernet Packet Generator register. Refer to the datasheet for configuration options.

A Good CRC packet counter is in ExtMII 18.13:0. A read of the register reads back the good CRC packets and then clears the register so the subsequent reads will be 0 if no traffic has been received. If traffic has been received since the last read, bit 15 will be set.

4.5.2 Copper PHY Error Counters

Idle errors = MII 10.7:0

RX errors = MII 19.7:0

False carrier = MII 20.7:0

Disconnects = MII 21.7:0

CRC errors = ExtMII 23.7:0

4.5.3 Fiber PHY Error Counters

Good RX CRC packets = Ext3MII 28.13:0

Bad RX CRC packets = Ext3MII 29.7:0

Good TX CRC packets = Ext3MII 21.13:0

Bad TX CRC packets = Ext3MII 22.7:0

5 Additional Information

For any additional information or questions regarding the device(s) mentioned in this document, contact your local sales representative.

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