

REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		1-20-16
B	Increased +1.2V Capacitor Value & VDD12A Cap Requirement		1-16-17

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DOCUMENT DESCRIPTION
Component Placement Checklist for the LAN7800, 48-pin SQFN Package

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Component Placement Checklist for LAN7800

Information Particular for the 48-pin SQFN Package

LAN7800 SQFN Phy Interface:

1. There are no component placement issues associated with the Phy Interface of the LAN7800 SQFN.

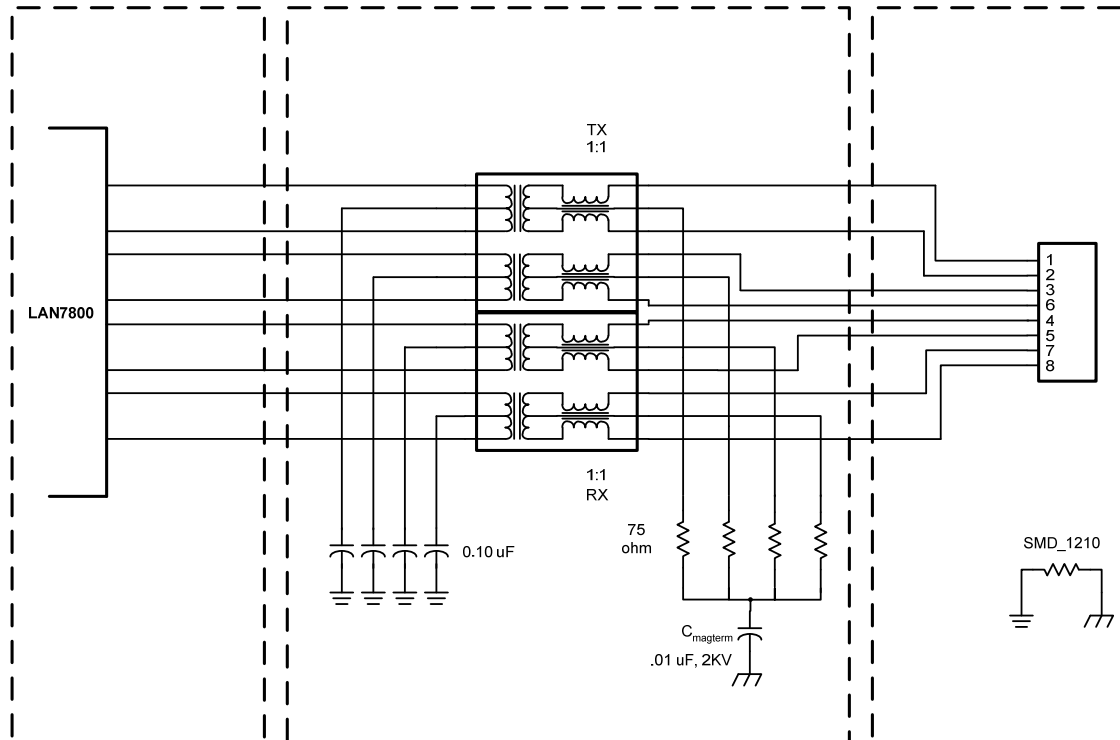
LAN7800 SQFN Magnetics:

1. Place the 0.10 μ F TX/RX Channel Center Tap termination capacitors as close to the magnetics as possible.
2. Place the 75 Ω cable side center tap termination resistors and the 1000 pF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible.

RJ45 Connector:

1. Place the RJ45 connector, the magnetics and the LAN7800 SQFN as close together as possible.
2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN7800 SQFN.
3. Select and place the magnetics as to set up the best routing scheme from the LAN7800 SQFN to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.
4. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.





Locate these four
resistors and five caps
close to the magnetics

Locate the shorting
component close to the
RJ45 connector

Figure No.1 Indicating Component Placement

+3.3V Power Supply Connections:

1. Place the VDD33A decoupling capacitor for the LAN7800 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.
2. Place the VDD33_REG_IN decoupling capacitor for the LAN7800 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.
3. Place the VDD_SW_IN decoupling capacitor for the LAN7800 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

VDDVARIO Power Supply Connections:

1. Place the (3) VDDVARIO decoupling capacitors for the LAN7800 SQFN as close to each power pin as possible. Using an SMD_0603 package will make this task easier.

+2.5V Power Supply Connections:

1. Place the VDD25_REG_OUT low ESR capacitor for the LAN7800 SQFN as close to the power pin as possible.
2. Place the VDD25_REG_OUT bypass capacitor for the LAN7800 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.
3. Place the (4) VDD25A decoupling capacitors for the LAN7800 SQFN as close to each power pin as possible. Using an SMD_0603 package will make this task easier.



+1.2V Power Supply Connections:

1. Place the 3.3 uH inductor as close as possible to the VDD12_SW_OUT (pin 13) on the LAN7800.
2. Also place the 22 uF Low ESR capacitor as close as possible to the 3.3 uH inductor and the VDD12_SW_OUT (pin 13) on the LAN7800.
3. Place the VDD12_SW_OUT bypass capacitor for the LAN7800 SQFN as close to the 3.3 uH inductor as possible. Using an SMD_0603 package will make this task easier.
4. Keep the VDD12_SW_OUT node away from any other sensitive circuitry (address lines, data lines, Ethernet traces, other components, etc.) as this node is very noisy.
5. Place the VDD12_SW_FB decoupling capacitor for the LAN7800 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.
6. Place the (2) VDD12CORE decoupling capacitors for the LAN7800 SQFN as close to each power pin as possible. Using an SMD_0603 package will make this task easier.
7. Place the ferrite bead associated with the VDD12A power rail as close as possible to the (3) VDD12A power pins on the LAN7800.
8. Place the (3) VDD12A decoupling capacitors for the LAN7800 SQFN as close to each power pin as possible. Using an SMD_0603 package will make this task easier.
9. Place the VDD12A 1.0 uF, low ESR cap close to pin 25 in the board design.

Ground Connections:

1. There are no component placement issues associated with the LAN7800 SQFN ground connections. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible.

Crystal Connections:

1. Place the 25.000 MHz crystal and the associated 15 – 33 pF capacitors as close together as possible and as close to the LAN7800 SQFN (XI, pin 40 & XO, pin 41) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.)
2. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all the crystal components are referenced to the same reference plane.



EEPROM Interface:

1. There are no component placement issues associated with the Phy Interface of the LAN7800 SQFN.

REF_REXT Resistor:

1. Place the REF_REXT resistor as close to pin 47 of the LAN7800 SQFN as possible.

REF_FILT Capacitor:

1. Place the REF_FILT capacitor as close to pin 48 of the LAN7800 SQFN as possible.

USBRBIAS Resistor:

1. Place the USBRBIAS resistor as close to pin 37 of the LAN7800 SQFN as possible.

Required External Pull-ups/Pull-downs:

1. There are no component placement issues associated with the External Pull-ups / Pull-downs of the LAN7800 SQFN.

USB Interface:

1. For board applications where the USB 3.0 link is between two devices intra-board, the SSTX and SSRX channels must be crossed over. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3DP_TXDNx & USB3DM_TXDNx on the USB7800 device. Two more DC blocking caps should be placed on the transmit pins of the other USB 3.0 device.
2. For board applications where the USB 3.0 link uses a USB connector, the RX and TX channels must not be crossed over to the connector. The cross over function is accomplished in the USB cable. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3DP_TXDNx & USB3DM_TXDNx on the USB connector. Two more DC blocking caps should exist on the transmit pins of the other USB 3.0 device on the other side of the cable.



Miscellaneous:

1. Bulk capacitors for each power plane can reside anywhere on the plane they serve.
2. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes.
3. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the USB connector in a logical place to short the two planes.

