TB3182

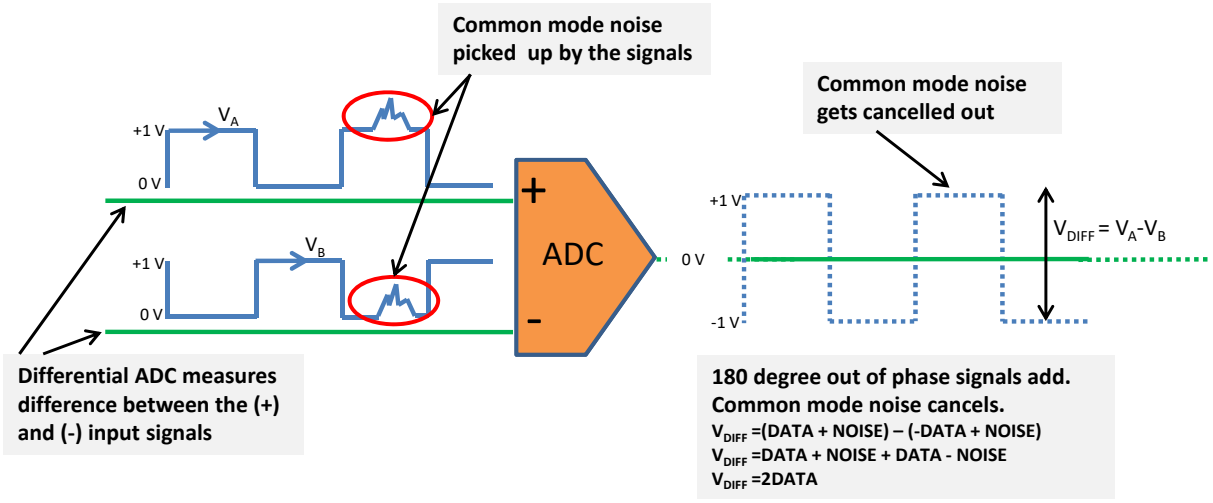
How to Use Differential ADC on Cortex® M7 MCUs

Introduction

A differential ADC measures the voltage between the two inputs. In a differential ADC system, two lines carry the desired signals of 180 degrees out of phase with respect to each other, and the signals run parallel to each other. As a result, an equal amount of noise occurs in both the lines. When a signal is applied to the A(+) and the A(-) inputs of a differential ADC, the voltage difference between the desired signals adds up as the desired signals are 180 degrees out of phase with respect to each other. The in-phase signals, such as the common-mode noise are rejected by the differential ADC. This results in an improved signal-to-noise ratio. Other advantages include cancellation of harmonics in the even order.

The following figure shows the cancellation of common mode noise in a differential ADC. The output signal is the analog representation of the digital value converted by the ADC.

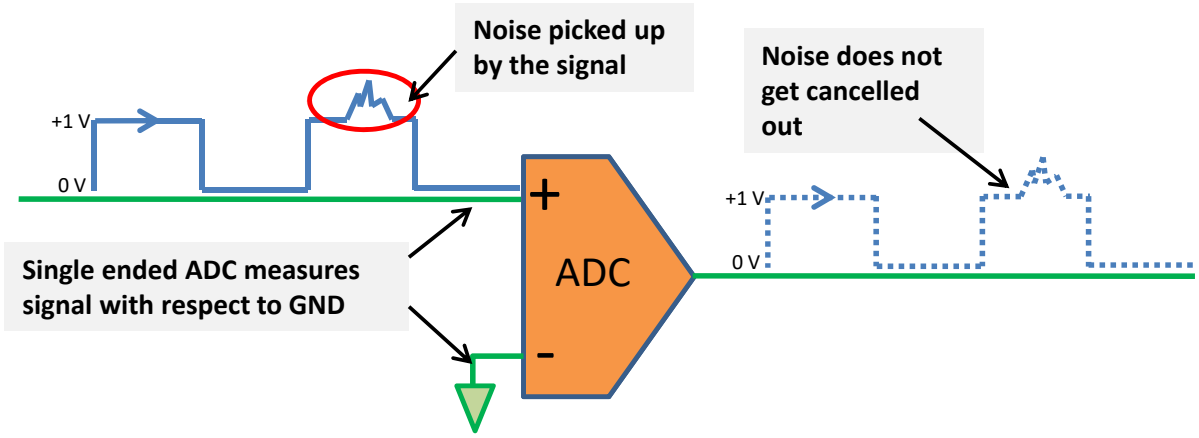
Figure 1. Cancellation of Common-Mode Noise in a Differential ADC



On the other hand, a single-ended Analog-to-Digital Converter (ADC) measures the signal voltage with respect to the ground. A single-ended ADC is sufficient when the signal source and ADC are close enough. However, in a noisy environment a single-ended system becomes more susceptible to noise.

The following figure shows the effect of noise in a single-ended ADC.

Figure 2. The Effect of Noise in a Single-Ended ADC



ARM® Cortex® -M7 based Microchip's MCUs, such as SAM V7x/E7x/S7x have an analog front-end controller (AFEC) which consists of a 12-bit ADC with two 6-to-1 analog multiplexers interfaced with two sample and hold (S&H) circuits, namely SH-1 and SH-2. It also consists of an internal Digital-to-Analog Converter (DAC), programmable-gain amplifiers (PGA), digital averaging with oversampling, therefore the resolution can be extended up to 16-bit. This document describes how to use the differential mode of ADC on Microchip's Cortex-M7 based MCUs.

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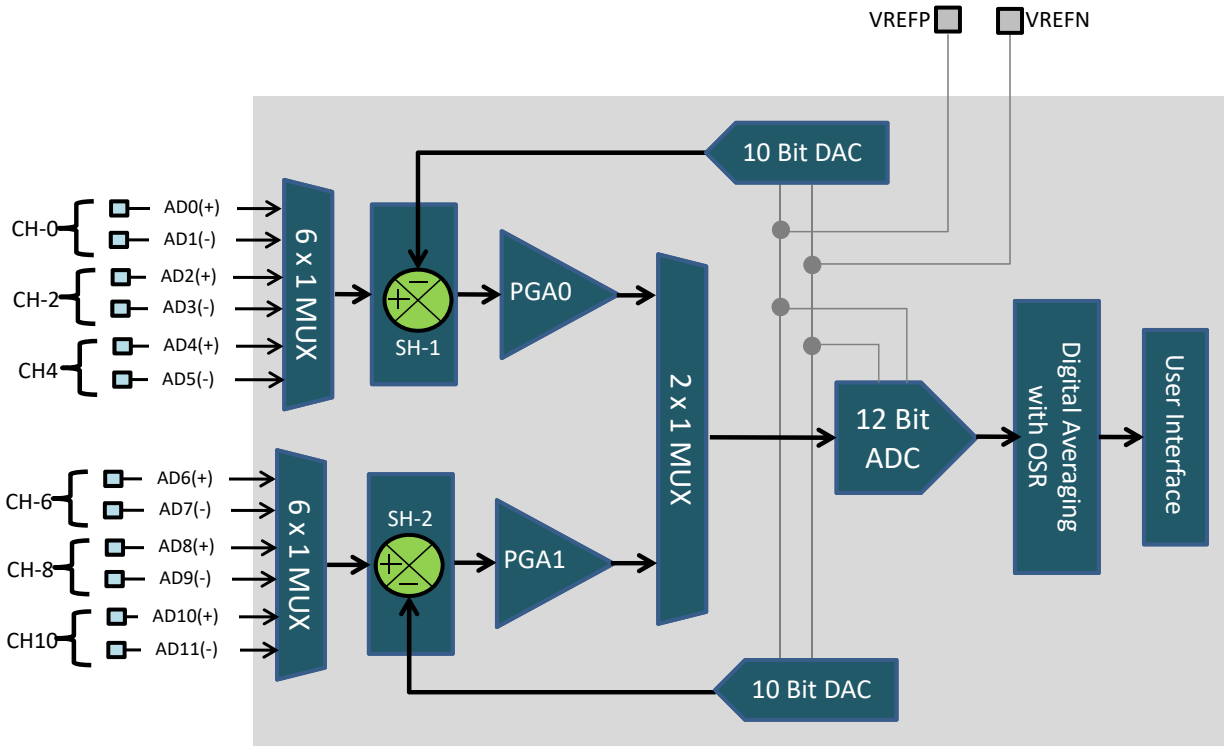
1. Enabling Differential Mode

Analog inputs can be configured either as Single-Ended mode or Differential mode. In Differential mode, consecutive analog inputs, such as AD0-AD1, AD2-AD3 form a pair of positive and negative analog inputs. The following figure shows a simplified AFEC block diagram, where six pairs of analog channels are shown in Differential mode.

Figure 1-1. Simplified AFEC Block Diagram with Analog Channels Configured in Differential Mode

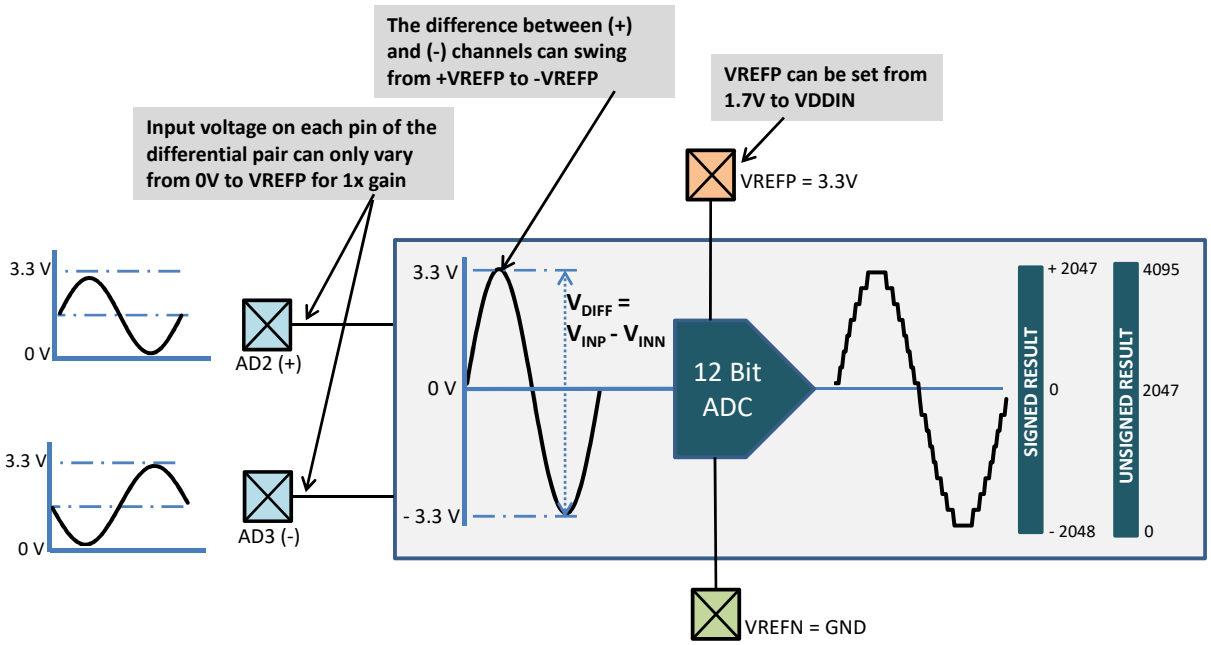


The input voltage on each pin of the differential pair is limited from 0V to V_{REFP}, where V_{REFP} is the positive voltage reference for the ADC, and it can vary from 1.7V to V_{DDIN}. The negative voltage reference pin V_{REFN} must be connected to GND. The following figure shows the input voltage range with V_{REFP}= 3.3V and a gain of 1. The differential voltage witnessed by the ADC can vary from -V_{REFP} to +V_{REFP} (that is, -3.3V to +3.3V); however, the voltage on individual inputs of the differential pair must be between 0 to V_{REFP}.

The result of the conversion depends on the Sign mode. For signed results, –V_{REFP} corresponds to -2048 and +V_{REFP} corresponds to +2047. For unsigned results, -V_{REFP} corresponds to 0 and + V_{REFP} corresponds to 4095.

Differential voltages smaller than –V_{REFP} results in negative saturation (-2048 for Signed mode and 0 for Unsigned mode) and differential voltages greater than +V_{REFP} results in positive saturation (+2047 for Signed mode and 4095 for Unsigned mode).

Figure 1-2. Input Signal Ranges When Channels are Configured in Differential Mode



Differential mode can be configured by setting the Channel Enable bit (AFEC_CHER.CHx) to 1 and then by setting the Differential Mode bit (AFEC_DIFFR.DIFFx) to 1, where x is the even channel number of the differential pair. To configure the AD2 and AD3 in Differential mode, the AFEC_CHER.CH2 and AFEC_DIFFR.DIFF2 bits must be set to 1. The AD3 will be automatically enabled for differential operation, see table below. Once the conversion is complete, the Conversion bit (AFEC_ISR.EOC2) is set to 1, and the result can be read either from the AFEC_LCDR.LDATA register or from the internal multiplexed AFEC_CDR.DATA register by configuring the channel in the Channel Selection register, AFEC_CSELR.CSEL, to 0x02.

Table 1-1. Register Configuration for AFEC_AD2 and AFEC_AD3 in Differential Mode

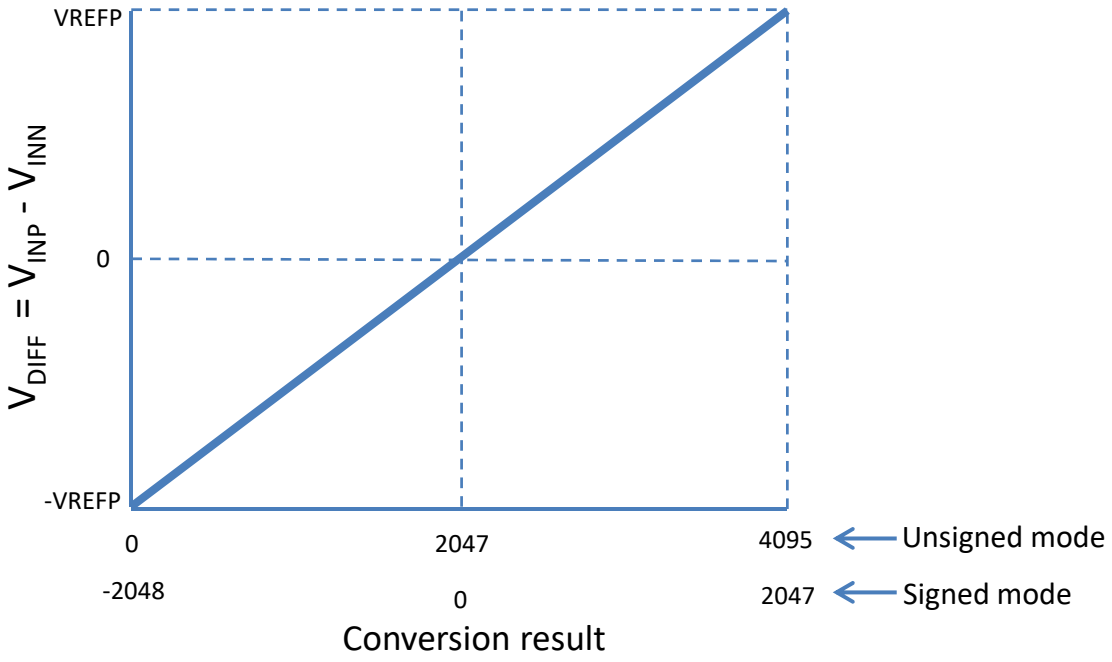
	Configuration		Status	Results	
x	DIFFR.DIFFx	CHER.CHx	ISR.EOCx	CSELR.CSEL	CDR.DATA
2	1	1	1	0x02	Valid
3	0	0	0	-	-

Note:

1. For a detailed description of the AFEC registers, refer to the respective SAM V7x/E7x/S7x data sheet.
2. Additionally, in Differential mode, the DAC output must be programmed to mid-scale or 512 when there is no DAC offset error to compensate. To compensate the DAC offset error of n LSB (positive or negative), it must be set to 512+n. When AD2-AD3 are configured in Differential mode, the DAC output must be set to 512+n by configuring the channel in the AFEC_CSELR.CSEL register to 0x02 and then setting the AFEC_COCR.AOFF bits to 512+n.
3. To enable the analog inputs, AFE_ADx, the pull-up resistors on the I/O lines must be disabled in the PIO user interface prior to writing the register either AFEC_CHER or DACC_CHER.

By default, the results of differential channels are provided in Signed mode (AFEC_EMR.SIGNMODE = 0x00). Unsigned mode can be enabled by setting the AFEC_EMR.SIGNMODE bits to 0x01.

Figure 1-3. Conversion Result



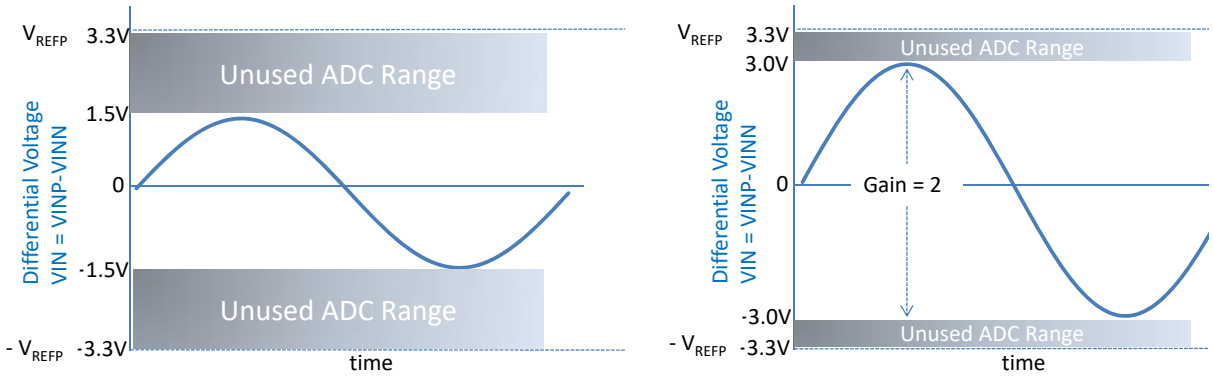
Note: The result of the conversion depends on Signed or Unsigned mode which are set through the AFEC_EMR.SIGNMODE bit.

2. Programmable Gain

The AFEC module provides a programmable gain which can be used to amplify small-signal voltages and to utilize the complete ADC range.

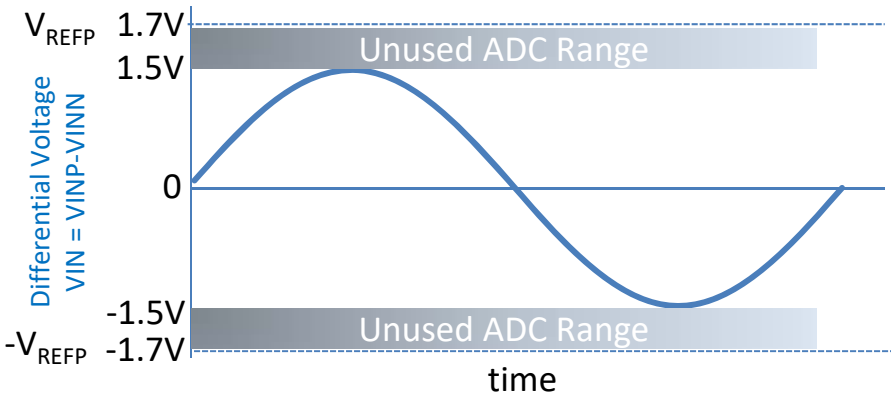
A sensor with a differential output voltage range of +1.5V to -1.5V is interfaced to a 12-bit ADC with V_{REFP} set to 3.3V. In this case, almost half of the ADC range from +1.5V to +3.3V and -1.5V to -3.3V are unused. Using a programmable gain, the amplitude of the input signal can be increased, such that it utilizes the complete ADC range. In this case, programming a gain value of 2 will result in the input voltage varying from +3.0V to -3.0V, thereby improving the resolution of the measured input voltage.

Figure 2-1. The Amplification of a Signal Using the Internal Programmable Gain Amplifier to Utilize the Full Range of ADC



Alternatively, the ADC reference can be lowered to match the sensor output range. The precision of the voltage measured by the ADC can also be increased by lowering the ADC reference V_{REFP}. The reference voltage of the AFEC module can be set by applying an external voltage on the V_{REFP} pin in the range of 1.7V to V_{DDIN}. The V_{REFN} pin must be connected to a ground. With the V_{REFP} set to 1.7V, 4096 steps will now be applied to the -1.7V to +1.7V voltage range resulting in a step size of 0.83mV (3.4V/ 4096 ≈ 830uV). With the V_{REFP} set to 3.3V, the step size will be 1.61mV.

Figure 2-2. Adjusting the ADC Reference Voltage to Utilize the Full Range of the ADC

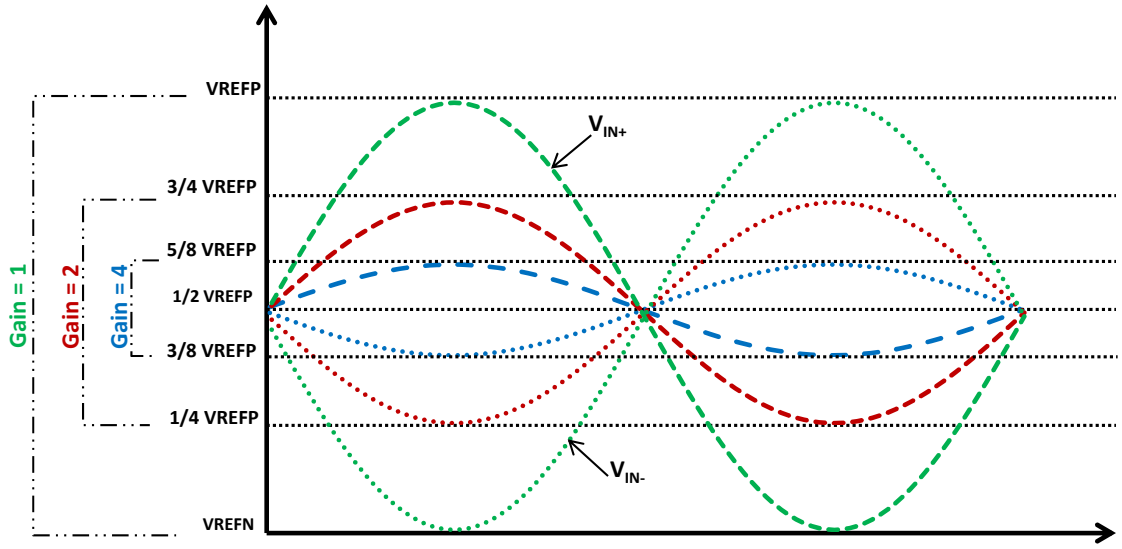


Note: Both of the above methods, that is, applying gain and reducing ADC reference voltage, enable users to measure an analog signal with better voltage precision using a lowered input voltage range.

Many sensors have a dynamic range higher than a 12-bit ADC can support. In such cases, the dynamic range can be increased by controlling the gain dynamically through software. In this case, the entire range of sensor output can be divided into sub-ranges where the highest gain is applied to the smallest sensor output voltage, and the lowest gain is applied to the highest sensor output voltage at run-time through the software.

The below figure shows the maximum differential analog input voltage allowed in each gain range. For example, if V_{REFP} = 3.3V and Gain = 4, the maximum differential input voltage must be between [0V, ± 0.825V].

Figure 2-3. Maximum Differential Input Voltage Ranges for 1x, 2x, and 4x Gains



To enable gain, the programmable gain amplifiers must be enabled by setting the AFEC_ACR.PGA0EN (for AN0-AN5) and AFEC_ACR.PGA1EN (for AN6-AN11) bits to 1. To set the gain on a differential pair of channels, the AFEC_CGR.GAINx bit must be set between 0-3, where x is the even channel number of the differential pair. To set the gain of the differential channels AD4-AD5 to 2, the AFEC_CGR.GAIN4 bit must be set to 0x01.

Table 2-1. Register Configuration for AFEC_AD4 and AFEC_AD5 in Differential Mode with a 2x Gain

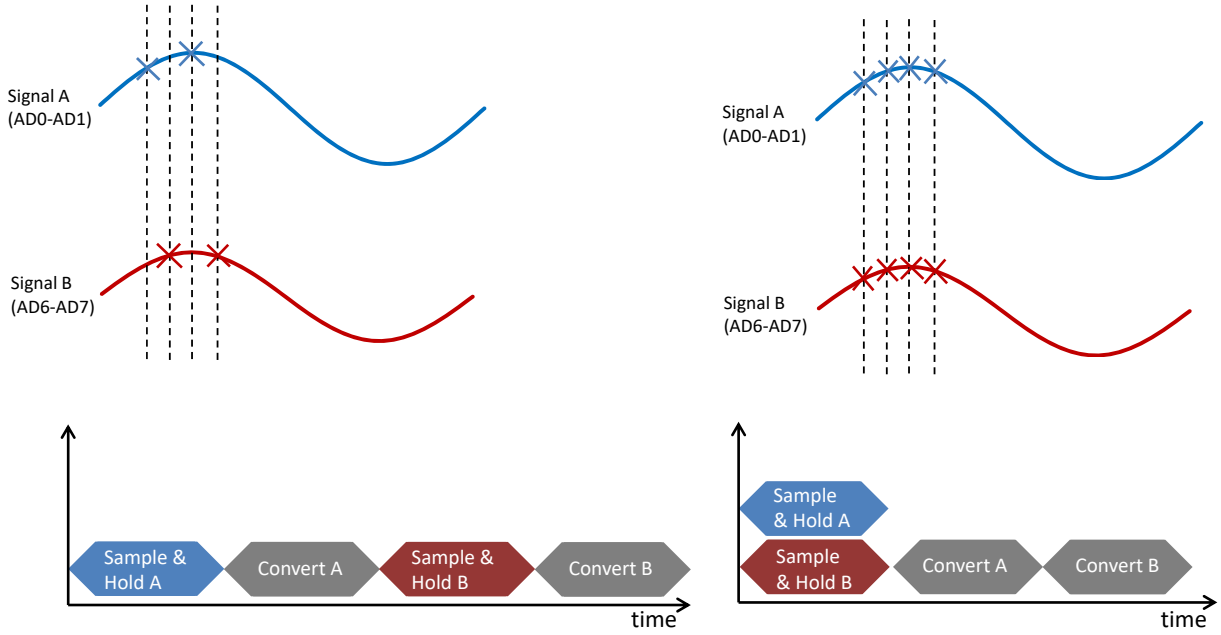
	Configuration			Status	Results	
x	DIFFR.DIFFx	CHER.CHx	CGR.GAINx	ISR.EOCx	CSELR.CSEL	CDR.DATA
4	1	1	1 **(See Note)**	1	0x04	valid
5	0	0	-	0	-	-

Note: The programmable gain amplifiers must be enabled by setting the ACR_PGA0EN and ACR_PGA1EN bits to 1 irrespective of whether the gain is used or not.

3. Simultaneous Sampling of ADC Channels

All analog inputs connected to a sample and hold circuit are multiplexed and sampled sequentially. However, some applications in motor control and metering require analog inputs to be sampled simultaneously to preserve the phase information between them.

Figure 3-1. Sampling ADC Channels with a Single Sample and Hold, and a Dual Sample and Hold Circuit

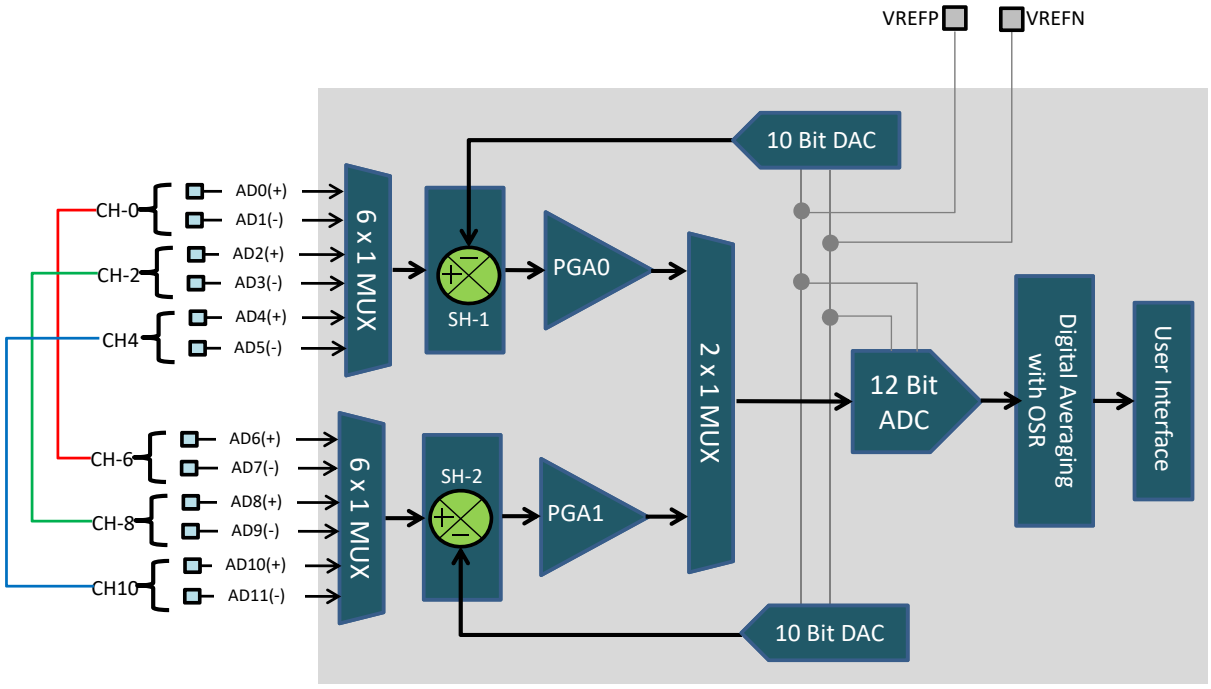


Note:

1. The left part of the figure illustrates analog inputs which are sampled sequentially with one sample and hold circuit.
2. The right part of the figure illustrates the concurrent sampling of analog inputs with two sample and hold circuits.

The AFEC module has two sample and hold circuits to enable concurrent sampling of analog inputs. The following figure illustrates pairs of differential channels configured in Concurrent Sampling mode, also known as Dual Sample and Hold mode.

Figure 3-2. Simplified AFEC Block Diagram with Pairs of Differential Channels Configured in Dual Sample and Hold Mode



Note: The following pairs of differential channels can be configured in Dual Sample and Hold mode:

1. AD0 - AD1 and AD6 - AD7 (Red line).
2. AD2 - AD3 and AD8 - AD9 (Green line).
3. AD4 - AD5 and AD10 - AD11 (Blue line).

Dual Sample and Hold mode is enabled by setting the AFEC_SHMR.DUALx bit to 1. The following table summarizes the configuration bits to be set to enable simultaneous sampling of the differential channels, AD0-AD1 and AD6-AD7. Once the conversion is complete, the AFEC_ISR.EOC0 and AFEC_ISR.EOC6 bits are set to 1, and the results of each differential channel can be read from the multiplexed AFEC_CDR.DATA register by first selecting the channel 0x00 and then channel 0x06 in the AFEC_CSELR.CSEL register.

Table 3-1. Register Configuration to Enable Concurrent Sampling of Differential Channels AFEC_AD0-AD1 and AFEC_AD6-AD7

	Configuration				Status	Results	
x	DIFFR.DIFFx	CGR.GAINx	SHMR.DUALx	CHER.CHx	ISR.EOCx	CSELR.CSEL	CDR.DATA
0	1	0-3	1	1	1	0x00	valid
1	0	-	0	0	0	-	-
6	1	0-3	0	0	1	0x06	valid
7	0	-	0	0	0	-	-

4. Using Sequencer in Differential Mode

The AFEC module can convert the channels in any sequence as provided by the user and the sequencer can be enabled by setting the AFEC_MR.USEQ bit to 1. Up to 12 channels can be sequenced by writing the channel numbers in the AFEC_SEQ1R and AFEC_SEQ2R registers and these channel numbers can be written in any order and repeated several times.

When Sequencer mode is enabled by setting the AFEC_MR.USEQ bit to 1, the behavior of the AFEC_CHER.CHx register is slightly different. In Sequencer mode, the AFEC_CHER.CHx register corresponds to the xth channel of the sequence programmed in the AFEC_SEQ1R and AFEC_SEQ2R registers. That is, if the sequencer is configured to convert differential channels AD4-AD5 and AD6-AD7 then CHER.CH0 and CHER.CH1 should be enabled (set to 1) instead of enabling CHER.CH4 (corresponding to AD4-AD5) and CHER.CH6 (corresponding to AD6-AD7).

The table below provides the register configurations required to convert the differential channels, such as AD2-AD3, AD0-AD1, AD6-AD7, AD0-AD1 and AD2-AD3 in sequence.

Table 4-1. Register Configuration to Convert Differential Channels in Sequence

	Configuration		Status			Results	
x	SEQ1R.USCHx	CHER.CHx	ISR.EOC0	ISR.EOC2	ISR.EOC6	CSELR.CSEL	CDR.DATA
0	0x02 (AD2-AD3)	0x01	0	1	0	0x02	valid
1	0x00 (AD0-AD1)	0x01	1	0	0	0x00	valid
2	0x06 (AD6-AD7)	0x01	0	0	1	0x06	valid
3	0x00 (AD0-AD1)	0x01	1	0	0	0x00	valid
4	0x02 (AD2-AD3)	0x01	0	1	0	0x02	valid

The results of the conversion can be read by selecting the channel number in the AFEC_CSELR.CSEL register and then reading the AFEC_CDR.DATA register.

To disable the third channel (AFEC_SEQ1R.USCH2) in the sequence, the AFEC_CHER.CH2 bit must be set to 0 as shown in the following table.

Table 4-2. Register Configuration to Disable 3rd Channel (AFEC_AD6-AD7) From the Conversion Sequence

	Configuration		Status			Results	
x	SEQ1R.USCHx	CHER.CHx	ISR.EOC0	ISR.EOC2	ISR.EOC6	CSELR.CSEL	CDR.DATA
0	0x02 (AD2-AD3)	0x01	0	1	0	0x02	valid
1	0x00 (AD0-AD1)	0x01	1	0	0	0x00	valid
2	0x06 (AD6-AD7)	0x00	0	0	0	-	-
3	0x00 (AD0-AD1)	0x01	1	0	0	0x00	valid
4	0x02 (AD2-AD3)	0x01	0	1	0	0x02	valid

5. Other Relevant Resources

For additional Information, refer to the "Using the Analog Front End in the SAM V7/E7/S7 MCUs Application Note"' which is available for download from the following location:

- http://ww1.microchip.com/downloads/en/AppNotes/Atmel-44046-Cortex-M7-Microcontroller-Using-the-Analog-Front-End-in-the-SAM-V7-E7-S7-MCUs_Application-Note.pdf

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