



**ECE1200 ESPI TO LPC BRIDGE EVALUATION BOARD
USER'S GUIDE**

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Preface

NOTICE TO CUSTOMERS

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Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXA”, where “XXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This document describes the Microchip ECE1200 demo. It details the demo setup and execution. This chapter contains general information that will be useful to know before using the ECE1200 eSPI to LPC Bridge Evaluation User's Guide. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document is written for anyone who wants to run the Microchip ECE1200 demo using an Intel RVP, a MCHP SCH3223 board, and a MCHP ECE1200 board. The manual layout is as follows:

- **Chapter 1. “Overview”** - Explains purpose and scope of this guide.
- **Chapter 2. “Hardware and Software Requirements”** - Provides hardware and software requirements for demo.
- **Chapter 3. “Demo Setup”** - Explains general purpose of the demo.
- **Chapter 4. “Running the Demo”** - Provides steps with illustrations for running the demo.
- **Appendix A. “Troubleshooting”** - Provides solutions for any potential issues.
- **Appendix B. “Pin-Outs for the Loopback Plugs”** - Provides pin-out detail.
- **Appendix C. “RVP J9G2 CFL Header”** - Diagram for RVP J9G2 CFL header pin-out.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	<i>MPLAB[®] IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<u><i>File>Save</i></u>
Bold characters	A dialog button	Click OK
	A tab	Click the Power tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	<i>file.o</i> , where <i>file</i> can be any valid filename
Square brackets []	Optional arguments	mcc18 [options] <i>file</i> [options]
Curly brackets and pipe character: { }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- **Emulators** – The latest information on Microchip in-circuit emulators. This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at:

<http://www.microchip.com/support>

DOCUMENT REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS50002972C (01-21-21)	Section 2.1 “Hardware Requirements”	Added in single and two board solutions.
	Section 4.7 “Step 7: Plug the ECE1200 EVB into header J9G2”	Added information and a figure.
	Section 4.10 “Step 10: Connect the Loopback Plug to SCH3223, and Verify Tera Term is Working”	Added a figure.
DS50002972B (05-21-20)	Section 2.1 “Hardware Requirements”	Replaced bullet, added second bullet.
	Section 2.3 “References”	Document reference added.
	Section 4.2 “Step 2: Modify Stock Board to Support ESPI Connectivity to the J9G2 Header”	Added second paragraph.
DS50002972A (03-24-20)	Document Release	

Chapter 1. Overview

The intent of the demo is to take a stock Intel Coffee Lake Platform (CLP) running the stock BIOS, and do a basic demonstration of UART activity using the onboard UART resources within the MEC142X and the onboard UART header with a loopback connector. Tera Term can be used to send characters over the UART and displayed in the Tera Term window. The loopback connector can then be removed to demonstrate that the characters are really being transmitted using the onboard UART in the MEC142X.

The final goal is to have the Tera Term UART activity to be directed to the SCH3223 add-in board to demonstrate that the ECE1200 successfully bridges ESPI cycles to LPC.

The final goal requires several steps:

1. Make small modifications to the stock motherboard to route ESPI signals to header J9G2. Must then retest to make sure no harm was done.
2. Replace the stock BIOS with a custom BIOS that reduces the ESPI bus to 1X, and ESPI frequency to 20MHZ. This is necessary when using the ESPI header due to noise considerations. After this test, retest the onboard UART with Tera Term to confirm that the board is still functional. (This step can be skipped, but it is highly recommended)
3. Load a different custom BIOS. This BIOS again reduces the bus width to 1X and speed to 20Mhz, and it also enables the PCH to enable ESPI chip select 1 (CS1), and routes it to the ESPI header. Once this is done, without the ECE1200 and SCH3223 plugged into the ESPI header, the motherboard will fail to even start to POST.
4. Once windows boots with the custom BIOS, the UART resources (0x3FX and IRQ4), are still routed to the onboard MEC142X. Tera Term can be used to confirm this.
5. Many registers within the PCH, MEC142X, ECE1200, and SCH3223 need to be modified to get the system to route the UART resources to the SCH3223 via the ECE1200 instead of the onboard MEC142X. A small test program needs to be run which will reconfigure things.
6. Once the test program is run, Tera Term can again be used, except this time it will be using the UART in the SCH3223. This can be confirmed by removing the loopback connector from the SCH3223 board.

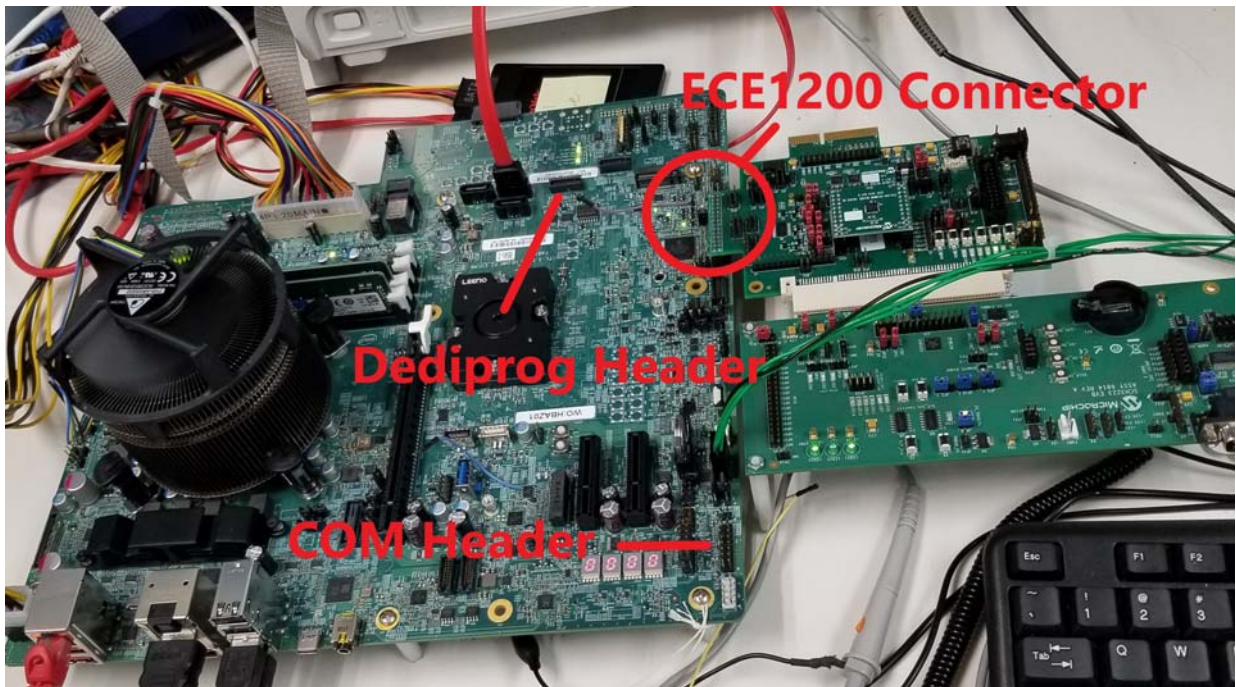
Chapter 2. Hardware and Software Requirements

2.1 HARDWARE REQUIREMENTS

The following is the hardware list for the demo.

- A stock CFL S RVP Board from Intel.
- An Intel PCH component, **SKU number C246**, ordered separately from the RVP board.

2.1.1 ECE1200 EVB + SCH3223 EVB Two Board Solution



Hardware and Software Requirements

- SCH3223 board



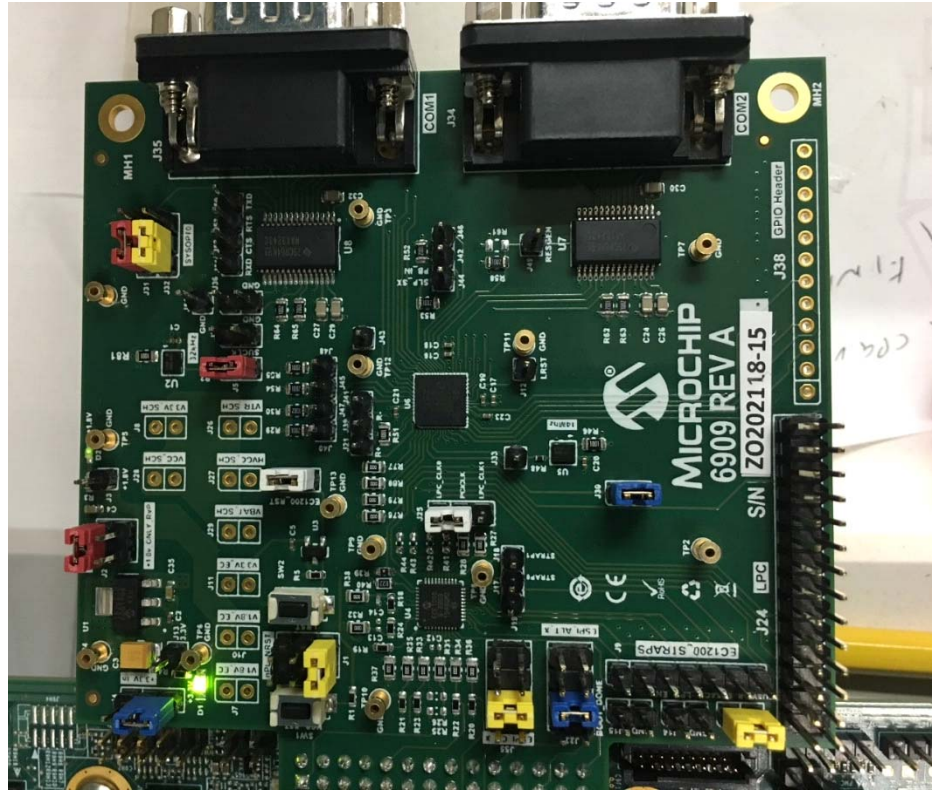
- ECE1200 board



2.1.2 ECE1200/SCH3223 Single Board Solution



Hardware and Software Requirements



- RS232 DB-9 serial loopback plug
See section **Section 3.2 “DP9 Loopback Plug”**.
- Dediprog SF100 ISP IC Programmer
<https://www.dediprog.com/product/SF100>

2.2 SOFTWARE REQUIREMENTS

- Windows 10
- Microchip provided BIOS for baselining, outimage_1x_20mhz_noslave.bin
- Microchip provided BIOS to enable the ECE1200, outimage_1x_20mhz_noslave_add_CS1.bin
- Microchip provided script for rerouting the UART resources (IO 3FX and IRQ4) from the onboard MEC142X to the external SCH3223 via the ECE1200
- Terminal emulator software, such as Tera Term

2.3 REFERENCES

The following documents should be referenced when using this user’s guide. Please contact your Microchip representative for availability.

- <https://www.microchip.com/wwwproducts/en/ECE1200>
- Intel Document #620778, Tiger Lake - UP3 for IoT Platforms COMe Type 6 Module Proof-of-Concept White Paper, March 2020

Chapter 3. Demo Setup

The general purpose of the demo is to show UART functionality using the onboard UART in the MEC142X using ESPI connected via CS0, or the UART in the SC3223 using ESPI connected to the ECE1200 via CS1, which will bridge to LPC and connect to the LPC SCH3223.

3.1 SETTING UP LOOPBACK ON THE RVP ONBOARD COM PORT HEADER

In order to baseline the system, the onboard COM port must be wired for loopback. See **Section B.1 “Setting Up Loopback on the RVP onboard COM Port Header”** for details on how to do this.

3.2 DP9 LOOPBACK PLUG

For the second phase of the demo, a DP9 loopback plug is used. See **Section B.2 “Pin-out for the DP9 Loopback Plug”** for details on how to do this.

3.3 SETTING UP TERA TERM

A terminal emulator program is required for this demo. The one used for this demo is Tera Term, and it will be described in this document. You are not restricted to Tera Term and may use any terminal emulator that you want.

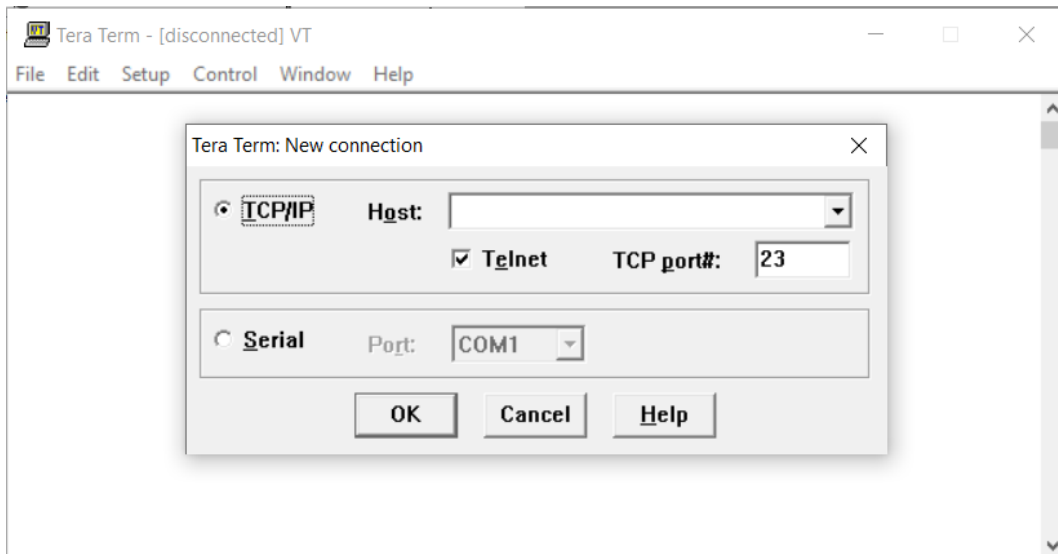
Tera Term can be downloaded at <https://tssh2.osdn.jp/>. Download the zip file and extract the contents to a directory. Then execute setup.exe and install to a directory of your choosing. Start the program by executing ttermpro.exe.

Chapter 4. Running the Demo

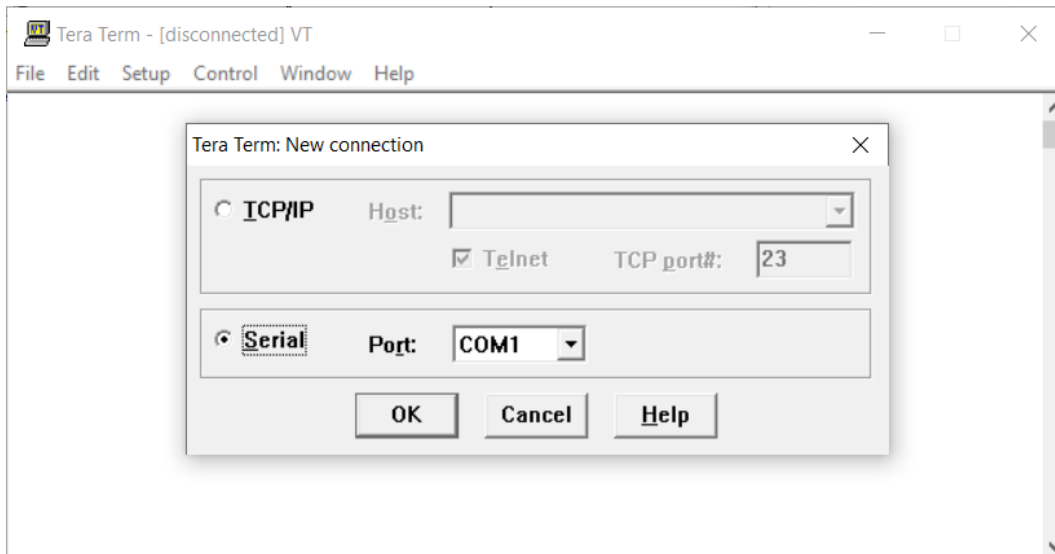
The purpose of the demo is to use Tera Term to verify a single com port (COM1) will be always selected with Tera Term. For the stock BIOS, the onboard MEC142X is used for COM1. For the modified BIOS, with the board modifications and a script being run to manipulate various registers on the RVP, COM1 resides in the SCH3223.

4.1 STEP 1: SERIAL COMMUNICATIONS USING THE ONBOARD MEC142X

- First, install a terminal emulator. For this demo, Tera Term is used. See **Section 3.3 “Setting Up Tera Term”** on how to install it.
- Then, wire the onboard COM header for loopback. See **Section 3.1 “Setting Up Loopback on the RVP onboard COM Port Header”**.
- Start Tera Term and you should see the following:



- Select 'Serial' and the desired COM port and press 'OK'.



- Type characters and see that they are echoed. See below.



Note: If desired, the loopback connector can be removed and when you type, characters will no longer be echoed. This will prove the COM port being used is the onboard COM PORT.

4.2 STEP 2: MODIFY STOCK BOARD TO SUPPORT ESPI CONNECTIVITY TO THE J9G2 HEADER

The below modifications will preserve ESPI connectivity to the MEC142X, but will also bring the ESPI signals to header J9G2 to allow connection the ECE1200 board.

First, ensure that you have replaced the CFL RVP board's PCH component with the C246 PCH component that was ordered separately. This specific PCH is required in order to generate a second eSPI Chip Select signal, which this demo uses to communicate with the ECE1200.

Modifications on Intel CFL RVP to bring ESPI signals to the ESPI Header.

- Stuff R9G1 with 0 Ohm
- Stuff R9G4 with 0 Ohm
- Stuff R9G13 with 0 Ohm
- Stuff R9G16 with 0 Ohm
- Stuff R9G19 with 0 Ohm
- Stuff R9F26 with 0 Ohm
- Empty R9G26
- Stuff R9G27 with 15 Ohm resistor for ESPI_CLK
- Populate R9F34 with a zero ohm resistor

4.3 STEP 3: RERUN TEST ON THE MODIFIED BOARD USING ONBOARD MEC142X TO MAKE SURE BOARD CHANGES HAVEN'T BROKEN ANYTHING

Execute the Tera Term test described in **Section 4.1 "Step 1: Serial Communications Using the onboard MEC142X"** to make sure everything is still in working order.

4.4 STEP 4: LOAD BIOS OUTIMAGE_1X_20MHZ_NOSLAVE.BIN WITH DEDIPROG USING CONNECTOR J7H1

It is strongly recommended that the onboard STOCK BIOS be "ripped" (copied) into a file using the DEDIPROG before loading any new BIOS. This will allow you to restore the board to STOCK condition if required.

This BIOS is a simple modification of the Stock BIOS. It restricts ESPI bus width to 1X and speed to 20mhz due to the challenges of connecting the ECE1200 board to a header.

To flash the BIOS, use the Dediprogrammer and program the provided BIOS file outimage_1x_20mhz_noslave.bin.

RVP should be powered down when loading a BIOS with DEDIPROG.

4.5 STEP 5: RERUN TERA TERM TEST

Boot to Windows. On the board modified in **Section 4.4 "Step 4: Load BIOS outimage_1x_20mhz_noslave.bin with Dediprogrammer Using Connector J7H1"**, using onboard MEC142X, execute the Tera Term test as in **Section 4.1 "Step 1: Serial Communications Using the onboard MEC142X"** to make sure loading the new BIOS hasn't broken anything.

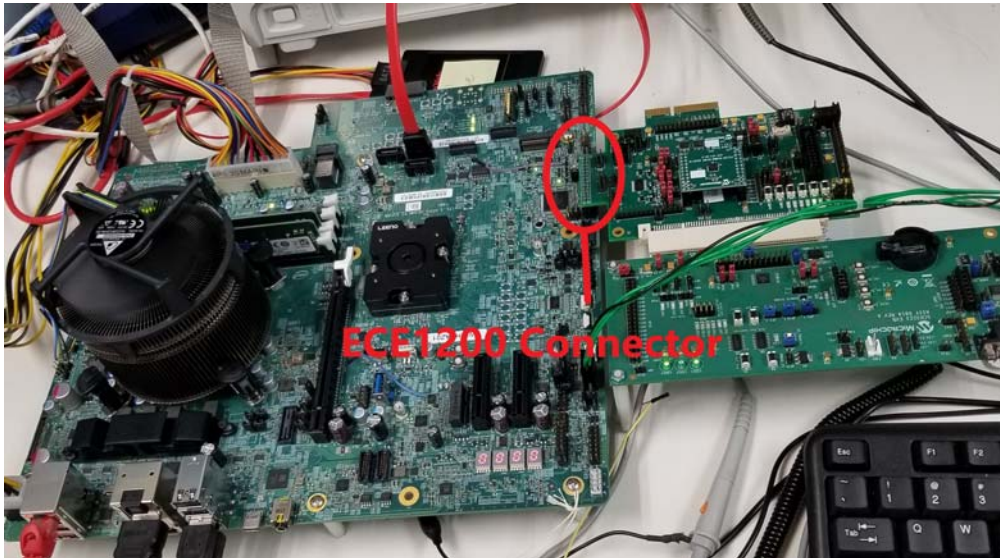
4.6 STEP 6: LOAD BIOS OUTIMAGE_1X_20MHZ_NOSLAVE_ADD_CS1.BIN WITH DEDIPROG USING CONNECTOR J7H1

This BIOS is a simple modification of the Stock BIOS. It restricts the ESPI bus width to 1X and speed to 20mhz due to the challenges of connecting the ECE1200 board to a header. This BIOS enables CS1, **and without a ECE1200 EVB plugged into header J9G2, RVP will not POST.**

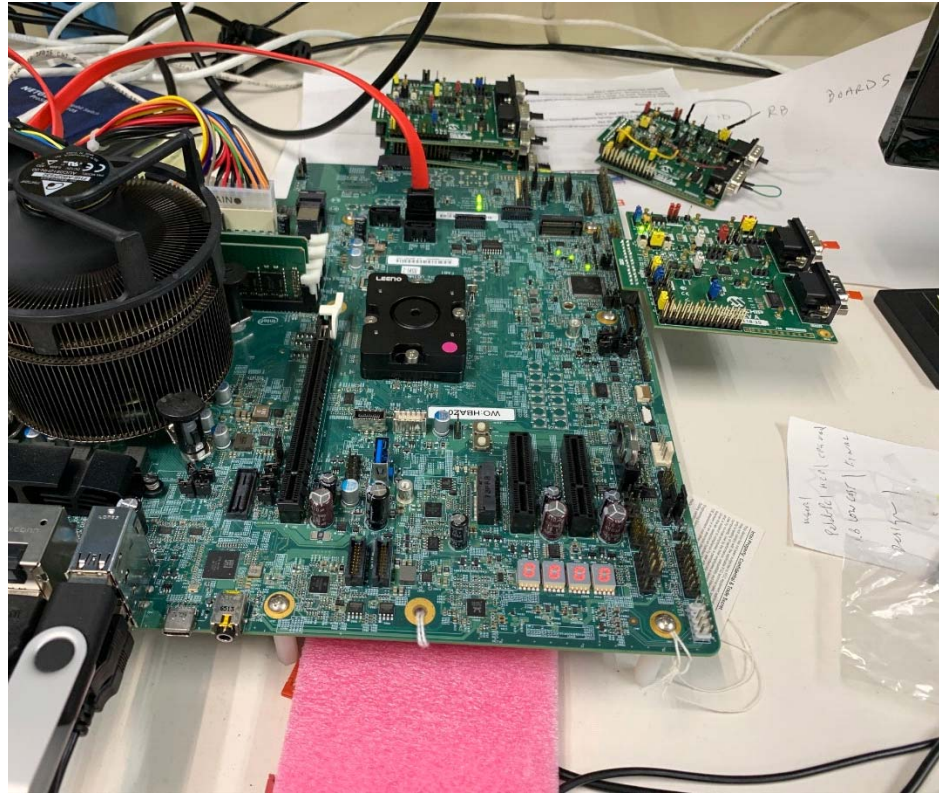
To flash the BIOS, use the Dediprogrammer and program the provided BIOS file outimage_1x_20mhz_noslave_add_CS1.bin.

4.7 STEP 7: PLUG THE ECE1200 EVB INTO HEADER J9G2

Plug the ECE1200 EVB into the header J9G2 as seen below.



Before powering up with new BIOS, plug the SCH3223 board into the ECE1200 board via the LPC male and female connector, then plug the ECE1200 into the RVP via the J9G2 header. As received from Microchip, the SCH3223 and ECE1200 should be properly jumper-ed. Optionally, plug the ECE1200/SCH3223 Single board into the header J9G2 as seen below.



Turn on the power and the board should boot to Windows. Once the ECE1200 is being used, all power cycling of the board should be done via the external supply by mechanically turning the supply off and on. Typically turning the supply mechanically on will allow the system to boot. To turn it off, shut down from windows, then turn off the power supply and wait for all LEDs on RVP to go off before turning back on (takes about ten seconds).

4.8 STEP 8: RERUN TERA TERM TEST

From within Windows, test with Tera Term communicating to a second test PC as in **Section 4.1 “Step 1: Serial Communications Using the onboard MEC142X”**. This will be using the onboard MEC142X.

4.9 STEP 9: RUN RVP.EXE

Place the files related to the script in a directory on the Windows 10 platform (corefiles.dll, LibFT260-64.dll, LibFT4222-64, mcp2221_dll_um_x64.dll, and RVP.exe). Right click on RVP.exe and run as administrator.

A small dialog will come up with a single button called "Test1", press it and a pop up will occur indicating that the MEC142X was found at 0x2E.

Close the pop up and the dialog and run Tera Term.

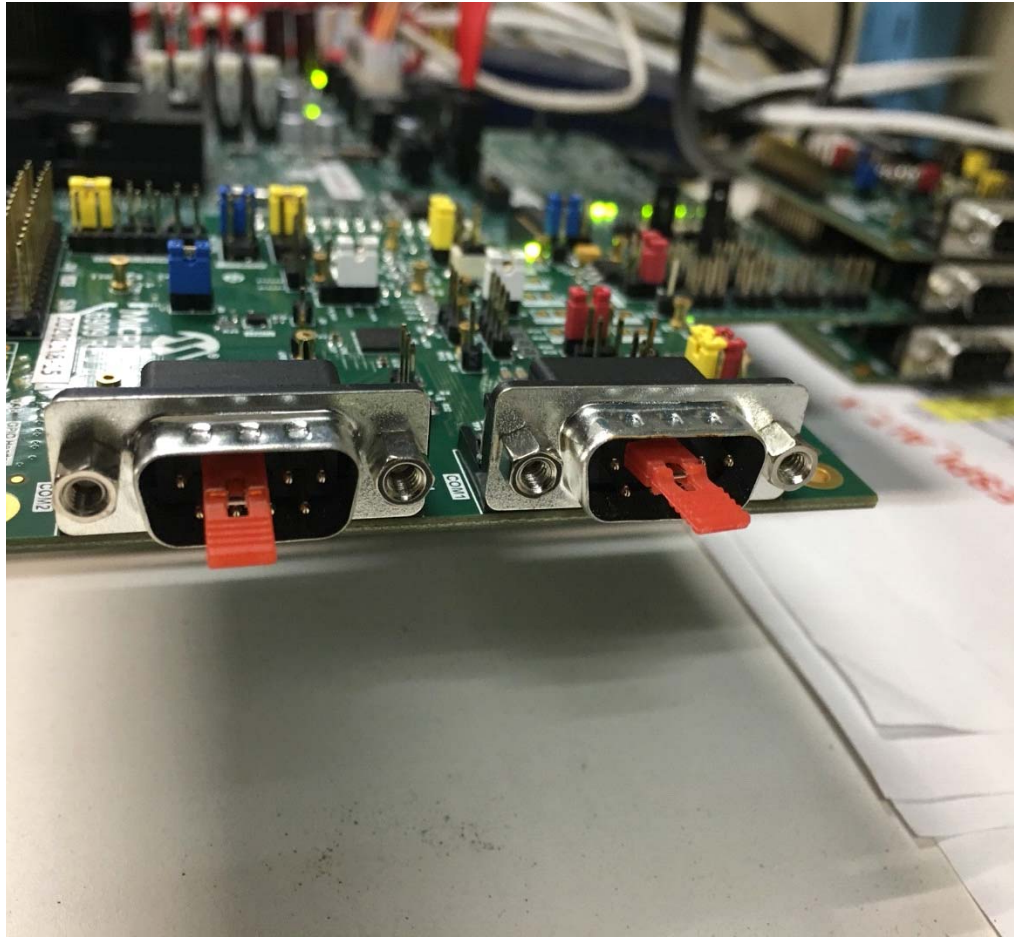
This will reconfigure the PCH, RB, onboard MEC142X, and SCH3223 such that IO addresses 0x3FX and IRQ4 get routed to SCH3223 instead of to the MEC142X.

4.10 STEP 10: CONNECT THE LOOPBACK PLUG TO SCH3223, AND VERIFY TERA TERM IS WORKING

Connect the loopback plug, as described in section **Section 3.2 “DP9 Loopback Plug”**, to the SCH3223, as seen below. And rerun the Tera Term test to verify that it's working.



Note: If desired, the loopback connector can be removed and when you type, characters will no longer be echoed. This will prove the COM port being used is the SCH3223 COM PORT.



Appendix A. Troubleshooting

This section details how to troubleshoot any potential issues that may occur.

No POST codes:

The most common way for the PORT80 display not to power up is if the outimage_1x_20mhz_noslave_add_CS1.bin BIOS is being used but the ECE1200 board isn't plugged into J9G2. Make sure with the outimage_1x_20mhz_noslave_add_CS1.bin BIOS that the ECE1200 board is plugged into J9G2.

If the ECE1200 board is plugged into J9G2 and there is still no PORT80 display activity with the outimage_1x_20mhz_noslave_add_CS1.bin BIOS, then load the STOCK BIOS or the outimage_1x_20mhz_noslave.bin as a baseline.

POST codes but no video:

In general, if POST codes are happening, but there is no video, a PCIe video card can be used. This often fixes this issue.

No characters in Tera Term:

Put a scope probe on the appropriate TX/RX loopback pin for either the onboard loopback or the SCH3223 loopback connector and see if there is any activity when a key is pressed.

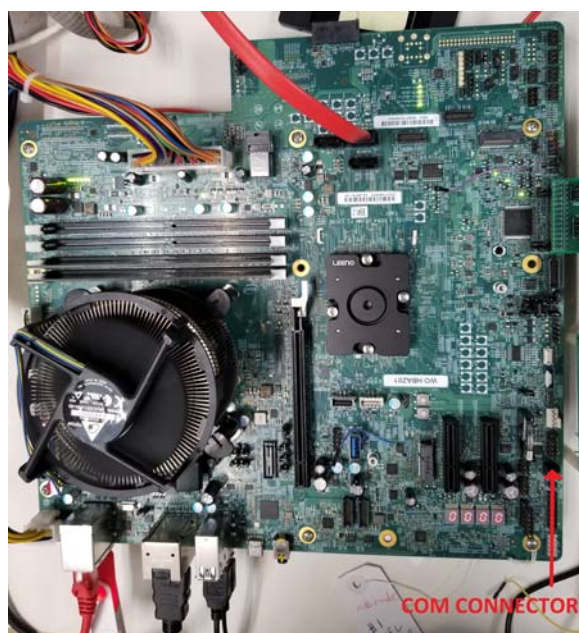
Teraterm fails to show characters when typing:

Make sure the appropriate loopback connector is installed for either on board UART or external ECE1200/SCH3223 UART. Please see **Section 3.1 "Setting Up Loopback on the RVP onboard COM Port Header"** and **Section 3.2 "DP9 Loopback Plug"**.

Appendix B. Pin-Outs for the Loopback Plugs

B.1 SETTING UP LOOPBACK ON THE RVP ONBOARD COM PORT HEADER

The COM header (J9B7) is located on the lower right as seen in the image below.

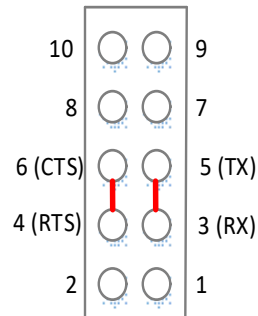


The pin-out is detailed below.

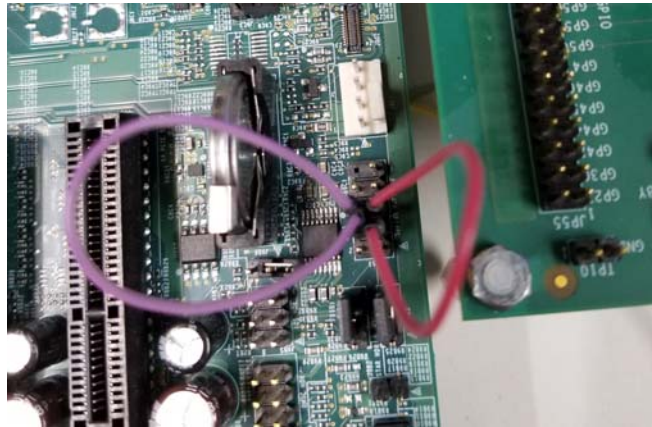
How to Loopback the Onboard COM Header

To loopback the onboard COM header:

- Connect the receive and transmit pins (3-5)
- Connect the request to send and clear to send pins (4-6)



Below is an image of the header wired for loopback.



The loopback wires can be removed to show that Tera Term stops working. This will prove that the onboard MEC142X is being used for COM1.

Pin-Outs for the Loopback Plugs

B.2 PIN-OUT FOR THE DP9 LOOPBACK PLUG

To construct an RS232 loopback plug used in this demo see below.

FIGURE 1: LOOPBACK PLUG PIN-OUT

How to Construct an RS232 Loopback Plug

To make an RS232 loopback plug:

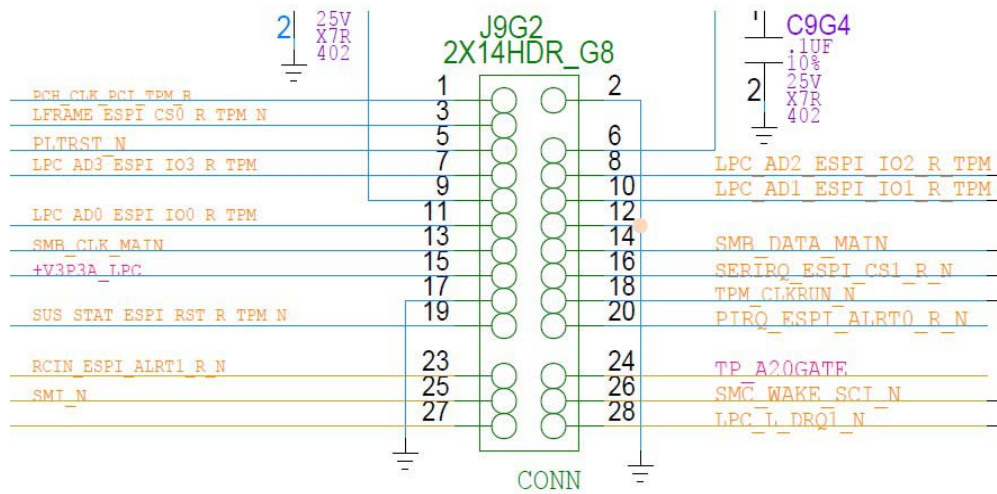
- Connect the receive and transmit pins (2-3)
- Connect the request to send and clear to send pins (7-8)
- Connect data carrier detect, data set ready and data terminal ready (1, 6 & 4)

The diagram shows a DB-9 connector with pins 1 through 9. Red lines indicate the following connections: Pin 1 to Pin 6, Pin 2 to Pin 3, Pin 4 to Pin 6, Pin 7 to Pin 8, and Pin 9 to Pin 4.

DB-9 Pin	EIA abbreviation	Description
1	DCD	Data carrier detect
2	RXD	Receive data
3	TXD	Transmit data
4	DTR	Data terminal ready
5	GND	Signal ground
6	DSR	Data set ready
7	RTS	Request to send
8	CTS	Clear to send
9	RI	Ring Indicator

Appendix C. RVP J9G2 CFL Header

Below is the pin-out for the RVP J9G2 CFL header.





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