dsPIC33CK512MP608

dsPIC33CK512MP608 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CK512MP608 family devices that you have received conform functionally to the current Device Data Sheet (DS70005452**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CK512MP608 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CK512MP608 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision	Number	Device ID(1)	Revision ID for Silicon Revision
		A0			A0
dsPIC33CK512MP608	0x9F54	0x0001	dsPIC33CK512MP308	0x9F14	0x0001
dsPIC33CK512MP606	0x9F53		dsPIC33CK512MP306	0x9F13	
dsPIC33CK512MP605	0x9F52		dsPIC33CK512MP305	0x9F12	
dsPIC33CK256MP608	0x9F44		dsPIC33CK256MP308	0x9F04	
dsPIC33CK256MP606	0x9F43		dsPIC33CK256MP306	0x9F03	
dsPIC33CK256MP605	0x9F42		dsPIC33CK256MP305	0x9F02	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]
				A0
I2C	Idle	1.	Address cannot be received in Idle mode.	X
CPU	DIV.SD Instruction	2.	Overflow bit is not getting set when an overflow occurs.	X
PWM	Time Base Capture	3.	PWM Capture Status (CAP) flag will not set again under certain conditions.	X
MCCP	Timer Interrupt	4.	Timer interrupt not working in Capture mode.	X
I2C	Collision Detection	5.	Bus collision is not detected during Host reception if there is a Start/Stop condition.	X
I2C	Client Mode	6.	Unexpected Client interrupt if there is a Stop bit in the 9th clock, followed by a Start bit.	X
I2C	Client Mode	7.	When data hold is enabled and software sends a NACK, a Client interrupt is asserted if there are more bytes on the bus.	X
ADC	Differential-Mode	8.	Errors may occur when enabling Differential-mode when F_{SRC} is greater than 50 MHz.	X
Reset	BOR	9.	BOR may stop functioning when V_{DD} drops into the window between the BOR level and BOR-25 mV.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**).

1. Module: I^2C

In Client mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A0							
X							

2. Module: CPU

When using the Signed 32/16-bit Division instruction, DIV.SD, the Overflow bit may not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the DIV.SD instruction.

Affected Silicon Revisions

A0							
X							

3. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status flag, CAP, will not set again.

Work around

Read the PWM Generator Capture (PGxCAP, x = 1 to 8) register at a known time to avoid the condition. The timing of the PGxCAP read operation can be scheduled by using the PWM Generator x (1-8) interrupt or any of the six PWM Event (A-F) interrupts corresponding to the PCI event, which triggered the time base capture. Read the PGxCAP value after the CAP bit has set within the interrupt.

Affected Silicon Revisions

A0							
X							

4. Module: MCCP

The CCP Timer Interrupt, _CCTxInterrupt, may not occur in Capture mode (CCSEL = 1) with the timer time base prescale set to anything other than zero (TMRPS[1:0] ≠ 0).

Work around

None.

Affected Silicon Revisions

A0							
X							

5. Module: I²C

Bus collision detection can fail during a Start/ Stop condition when a Host is receiving data from a Client. This condition can occur in a noisy environment or hot swapping I²C.

Work around

None.

Affected Silicon Revisions

A0							
X							

6. Module: I²C

An unexpected Client interrupt will occur if the Host sends a NACK and a Stop bit, followed by a Start bit in the ACK phase (9th clock) during Client transmit.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A0							
X							

7. Module: I²C

In Client mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, the Client interrupt is asserted if there are any bytes on the bus.

Work around

Software should ignore the Client interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A0							
X							

8. Module: ADC

When operating ADC with an Input Frequency (F_{SRC}) above 50 MHz, conversion errors may occur when enabling Differential-mode (DIFFx = 1).

Work around

During initialization of the ADC to write the ADMODxL/H registers, use a slower input frequency of 50 MHz or less. After completion of the first conversion of each channel in Differential-mode, Input Frequency, F_{SRC}, can be increased to the maximum specified in the “Electrical Characteristics” section of the device data sheet.

Affected Silicon Revisions

A0							
X							

9. Module: Reset

After startup, if V_{DD} decreases to a value between VBOR-25mV and VBOR, the BOR may unintentionally disable. The device may incorrectly operate down to 1.8V. However, while operating at a V_{DD} between 3-3.6V, the device will operate as expected. A tristate IO can be used to observe this behavior. The VBOR specification is listed in the “Electrical Characteristics” section of the device data sheet.

Work around

An external voltage monitor IC may be used as a workaround. MCP111-300E and similar devices are recommended for this purpose.

Affected Silicon Revisions

A0							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005452**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Flash Program Memory

The following section and table have been added to **Section 5.5 Flash OTP by ICSP™ Write Inhibit**:

5.5.1 Activating Flash OTP by ICSP Write Inhibit

Caution: It is not possible to deactivate ICSP Write Inhibit.

ICSP Write Inhibit is activated by executing a pair of NVMCON double-word programming commands to save two 16-bit activation values in the configuration memory space. The target NVM addresses and values required for activation are shown in Table 5-1. Once both addresses contain their activation values, ICSP Write Inhibit will take permanent effect on the next device Reset.

Only the lower 16 data bits stored at the activation addresses are evaluated; the upper eight bits and second 24-bit word written by the double-word programming should be written as ‘0’s. The addresses can be programmed in any order and also during separate ICSP/Enhanced ICSP/RTSP sessions, but any attempt to program an incorrect 16-bit value or use a row programming operation to program the values will be aborted without altering the existing data.

5-1. ICSP Write Inhibit Activation Addresses and Data

	Configuration Memory Address	ICSP™ Write Inhibit Activation Value
Write Lock 1	0x801034	0x006D63
Write Lock 2	0x801038	0x006870

2. Module: I/O Ports

In Table 8-5, the following rows have been added, as shown in **bold**.

Table 8-5. Remappable Output Pin Registers

Register	RP Pin	I/O Port
RPOR18[5:0]	RP68	Port Pin RD4
RPOR18[13:8]	RP69	Port Pin RD5
RPOR19[13:8]	RP71	Port Pin RD7
RPOR20[5:0]	**RP72**	**Port Pin RD8**
RPOR20[13:8]	**RP73**	**Port Pin RD9**
RPOR21[5:0]	**RP74**	**Port Pin RD10**
RPOR21[13:8]	**RP75**	**Port Pin RD11**
RPOR22[5:0]	**RP76**	**Port Pin RD12**
RPOR22[13:8]	**RP77**	**Port Pin RD13**
RPOR23[5:0]	**RP78**	**Port Pin RD14**
RPOR23[13:8]	**RP79**	**Port Pin RD15**
RPOR24[5:0]	**RP176**	**Virtual Pin RPV0**
RPOR24[13:8]	**RP177**	**Virtual Pin RPV1**
RPOR25[5:0]	**RP178**	**Virtual Pin RPV2**
RPOR25[13:8]	**RP179**	**Virtual Pin RPV3**
RPOR26[5:0]	**RP180**	**Virtual Pin RPV4**
RPOR26[13:8]	**RP181**	**Virtual Pin RPV5**

3. Module: I/O Ports

In Table 8-6, the following rows have been added.

Table 8-6. Output Selection for Remappable Pins (RPn)

Function	RPnR[5:0]	Output Name
MCCP9B	51	RPn tied to MCCP9B output
MCCP9C	52	RPn tied to MCCP9C output
MCCP9D	53	RPn tied to MCCP9D output
MCCP9E	54	RPn tied to MCCP9E output
MCCP9F	55	RPn tied to MCCP9F output
CLC3OUT	59	RPn tied to CLC3 Output
CLC4OUT	60	RPn tied to CLC4 Output
U1DTR	61	Data Terminal Ready Output 1
U2DTR	62	Data Terminal Ready Output 2
U3DTR	63	Data Terminal Ready Output 3

4. Module: Direct Memory Access (DMA) Controller

In Table 10-1, the following corrections and additions have been added, as shown in **bold**.

Table 10-1. DMA Channel Trigger Sources

CHSEL[6:0]	Trigger (Interrupt)	CHSEL[6.0]	Trigger (Interrupt)	CHSEL[6.0]	Trigger (Interrupt)
19h	PWM Event A	3Fh	ADC Done AN23	64h	SI2C3 – I2C3 Client Event
1Bh	PWM Event B	40h	**AD1FLTR1 – Oversample Filter 1**	65h	MI2C3 – I2C3 Host Event
1Ch	PWM Generator 1	41h	**AD1FLTR2 – Oversample Filter 2**	66h	SPI3 – Fault Interrupt
1Dh	PWM Generator 2	42h	**AD1FLTR3 – Oversample Filter 3**	67h	MCCP9
1Eh	PWM Generator 3	43h	**AD1FLTR4 – Oversample Filter 4**	68h	UART3 Receiver
1Fh	PWM Generator 4	44h	CLC1 Positive Edge Interrupt	69h	UART3 Transmitter
20h	PWM Generator 5	45h	CLC2 Positive Edge Interrupt	6Ah	ADC Done AN24
21h	PWM Generator 6	46h	SPI1 – Fault Interrupt	6Bh	ADC Done AN25
22h	PWM Generator 7	47h	SPI2 – Fault Interrupt	6Ch	PMP Event
23h	PWM Generator 8	48h	**ADC Done AN26**	6Dh	PMP Error
24h	PWM Event C	49h	**ADC Done AN27**	6Eh-7Fh	(Reserved, do not use)

5. Module: Controller Area Network Flexible Data Rate (CAN FD) Modules

Corrected the CLKSEL bit description in the C1CONL register, as shown in **bold**.

Bit 7 — CLKSEL Module Clock Source Select bit

Value	Description
1	Auxiliary clock is active when module is enabled
0	**CAN clock is active when module is enabled**

6. Module: High-Resolution PWM with Fine Edge Placement

In registers PGxFPCIL, PGxCLPCIL and PGxFFPCIL, the bit value description for Bits 4:0 – PSS[4:0] PCI Source Selection bits has been changed to `11110` = CLC2.

7. Module: High-Speed, 12-Bit Analog-to-Digital Converter

Adds the following missing register definitions to the ADC Register Summary:

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x0B96	ADTRIG5H	15:8				TRGSRC23[4:0]				
		7:0				TRGSRC22[4:0]				
0x0B98	ADTRIG6L	15:8				TRGSRC25[4:0]				
		7:0				TRGSRC24[4:0]				
0x0B9A	ADTRIG6H	15:8				TRGSRC27[4:0]				
		7:0				TRGSRC26[4:0]				
0x0B9C ... 0x0B9F	Reserved									

8. Module: Electrical Characteristics

In Table 33-26, the Internal FRC Accuracy Temperature Range has been changed as shown in **bold**.

Table 33-26. Internal FRC Accuracy

Param No.	Characteristic	Min.	Max.	Units	Conditions
F20a	FRC	-2(2)	+2	%	-40°C ≤ TA ≤ **-5**°C
		-1.5	+1.5	%	-5°C ≤ TA ≤ +85°C
		-2	+2	%	+85°C ≤ TA ≤ +125°C

9. Module: Electrical Characteristics

In Table 33-10, the following corrections have been made as shown in **bold**.

Table 33-10. DC Characteristics: Watchdog Timer Delta Current (ΔI_{WDT})(1)

DC Characteristics	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	Typ.	Max.	Units	Conditions	
DC61c	**130**	**300**	µA	-40°C	3.3V
DC61b	**125**	**600**	µA	+25°C	
DC61a	**125**	**600**	**µA**	+85°C	
DC61d	**100**	**3100**	**µA**	+125°C	

Note:
1. The ΔI_{WDT} current is the additional current consumed when the module is enabled. This includes the LPRC/BFRC clock source current. This current should be added to the base IPD current. All parameters are characterized but not tested during manufacturing.

10. Module: Special Features

Corrected the RCLKSEL bit description in the FWDT Configuration Register, as shown in **bold**.

Bits 6:5 – RCLKSEL[1:0] Watchdog Timer Clock Select bits

Value	Description
11	LPRC Clock
10	**FRC Clock**
01	**Peripheral Clock**
00	Reserved

11. Module: Product Identification System

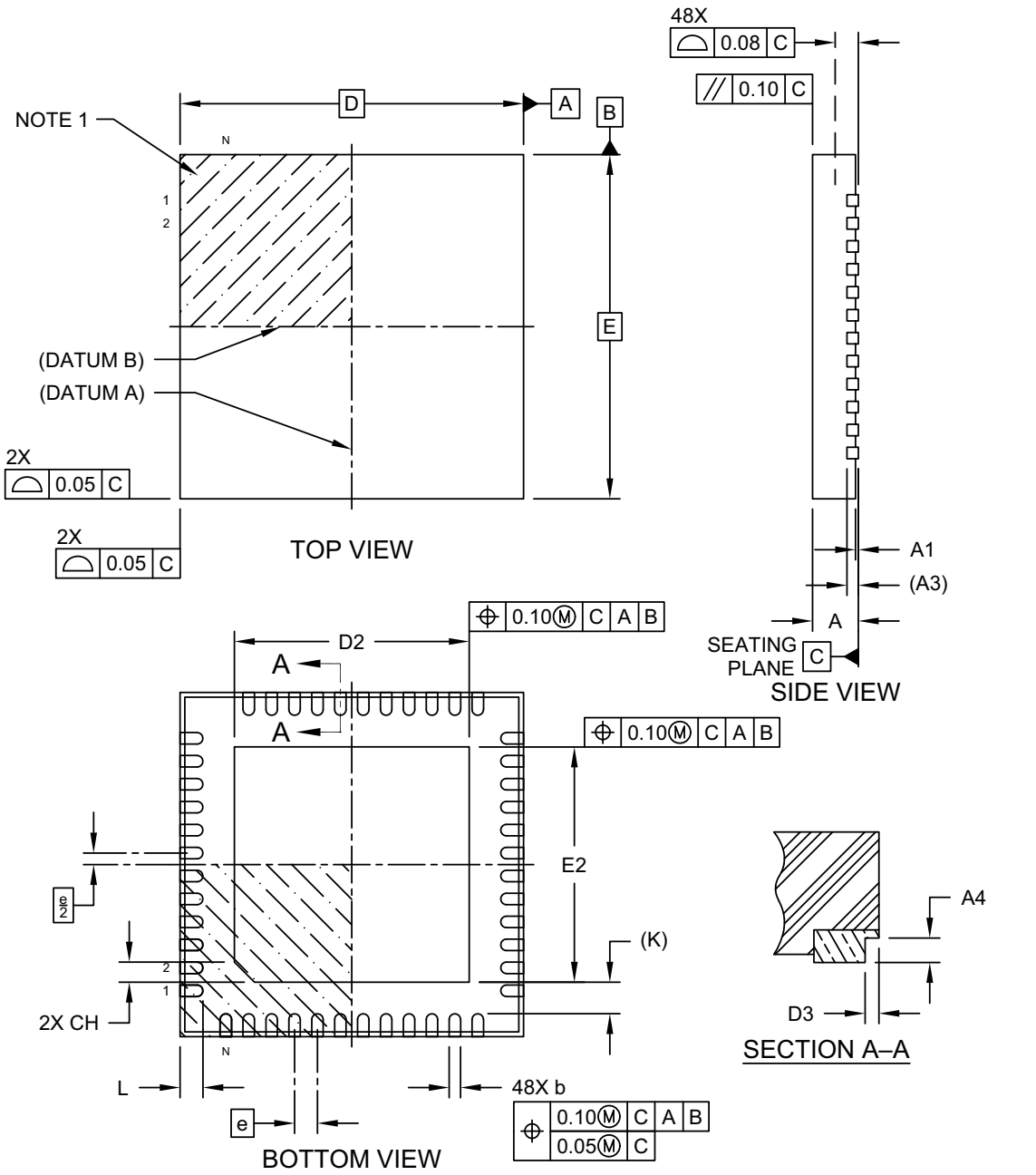
In the Product Identification System, the 6MX package has been changed to M7.

12. Module: Packaging Information

In Packaging Information, the 6MX drawings have been replaced with M7 drawings as shown below.

48-Lead Very Thin Plastic Quad Flat, No Lead Package (M7) - 6x6 mm Body [VQFN] With 4.1x4.1 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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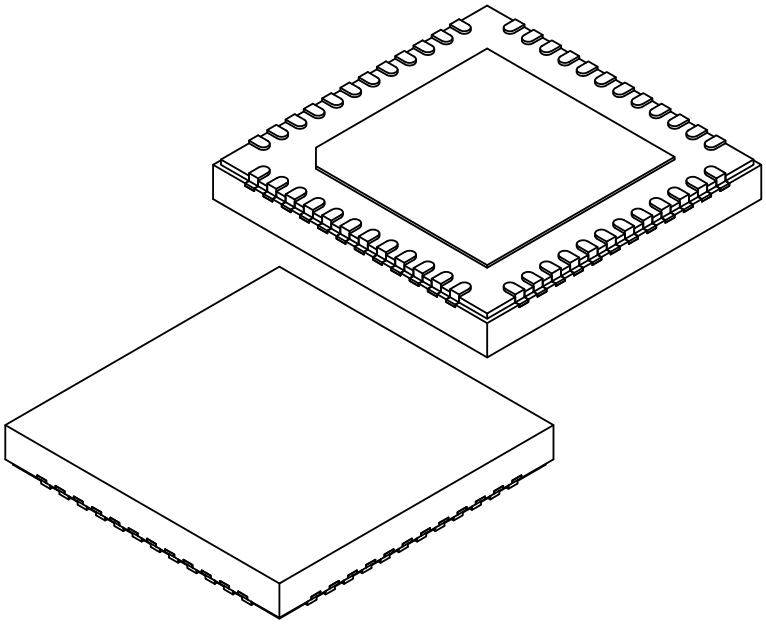
48-Lead Very Thin Plastic Quad Flat, No Lead Package (M7) - 6x6 mm Body [VQFN] With 4.1x4.1 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.00	4.10	4.20
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.00	4.10	4.20
Exposed Pad Corner Chamfer	CH		0.35 REF	
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.55 REF	
Wettable Flank Step Length	D3	-	-	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

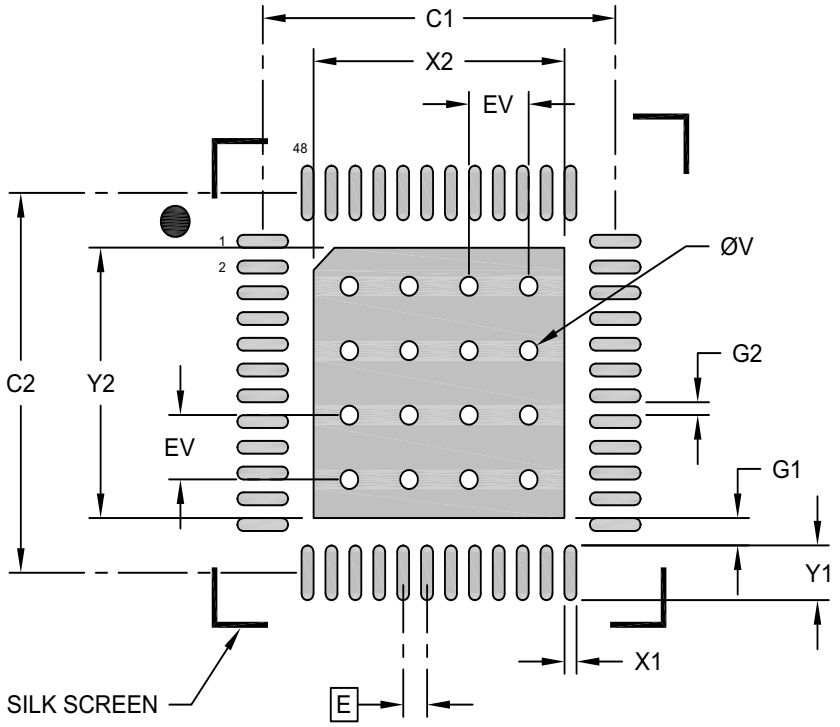
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-504-M7 Rev B Sheet 2 of 2

48-Lead Very Thin Plastic Quad Flat, No Lead Package (M7) - 6x6 mm Body [VQFN] With 4.1x4.1 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			4.20
Optional Center Pad Length	Y2			4.20
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Width (X48)	X1			0.20
Contact Pad Length (X48)	Y1			0.85
Contact Pad to Center Pad (X48)	G1	0.20		
Contact Pad to Contact Pad (X44)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2504-M7 Rev B

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (7/2021)

Initial version of this document; issued for revision A0.

Rev B Document (1/2022)

Updated data sheet references to current revision C.

Rev C Document (1/2024)

Added silicon issue 9 (Reset).

Added data sheet clarifications 1 (Flash Program Memory), 2 (I/O Ports), 3 (I/O Ports), 4 (Direct Memory Access (DMA) Controller), 5 (Controller Area Network Flexible Data Rate (CAN FD) Modules), 6 (I2C), 7 (I2C), 8 (Electrical Characteristics), 9 (Electrical Characteristics), 10 (Special Features), 11 (Product Identification System), and 12 (Packaging Information).

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