TB3221

Core Independent Voltage Window Signal Detection Using a Single Comparator Technical Brief

Introduction

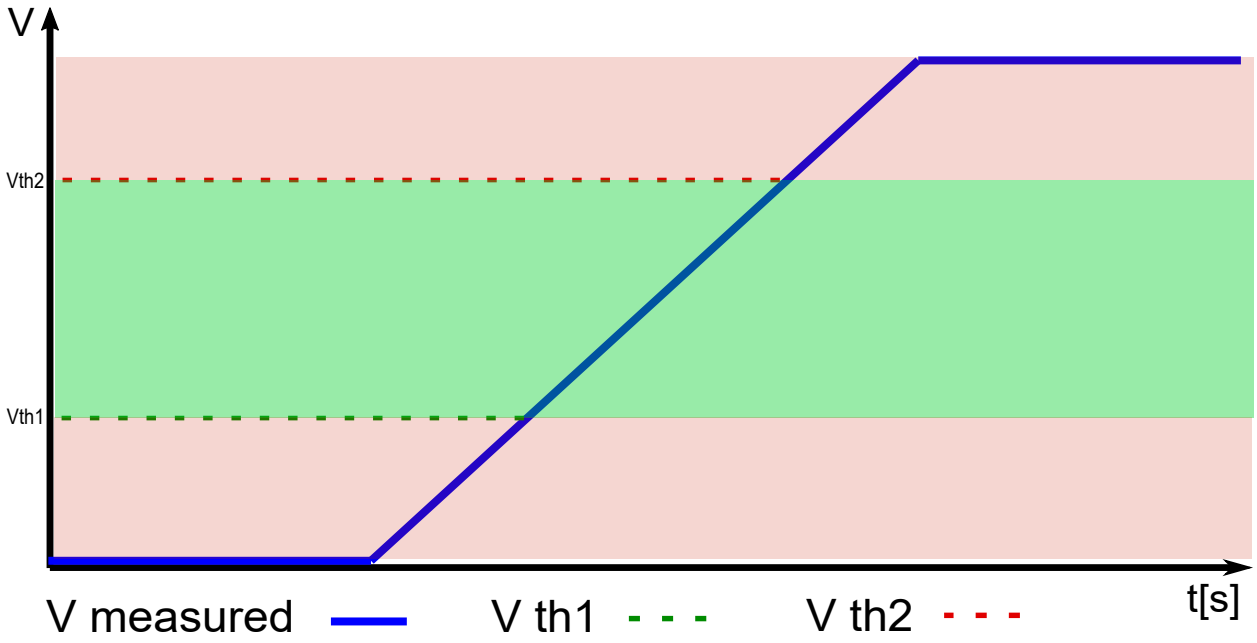
It is possible to find out whether a measured signal is below or above a certain value/reference using a single comparator. But, what if the desired interval is between two values, the undervoltage and overvoltage protection?

The most convenient and fastest solution is to use two comparators and two references. The results are analyzed to decide which of the three intervals houses the measured signal. Using an Analog-to-Digital Converter (ADC) and core post-processing will yield the same result, but the process is slower and dependent on core availability.

This technical brief presents an alternative method of implementing a core independent voltage window signal level detection (without software core supervision, as in the case of the ADC), using a single comparator and the Core Independent Peripherals (CIPs) of a PIC® microcontroller. For example, the method is used to implement an Undervoltage Protection (UVP) and Overvoltage Protection (OVP). The representation of the needed voltage window signal level between two thresholds is depicted in the figure below.

This solution has the advantage of using only CIPs. It does not need core usage, it is considerably faster than an ADC measurement, and it still provides all the configurability advantage for the user.

Figure 1. Voltage Window Interval of a Measured Signal



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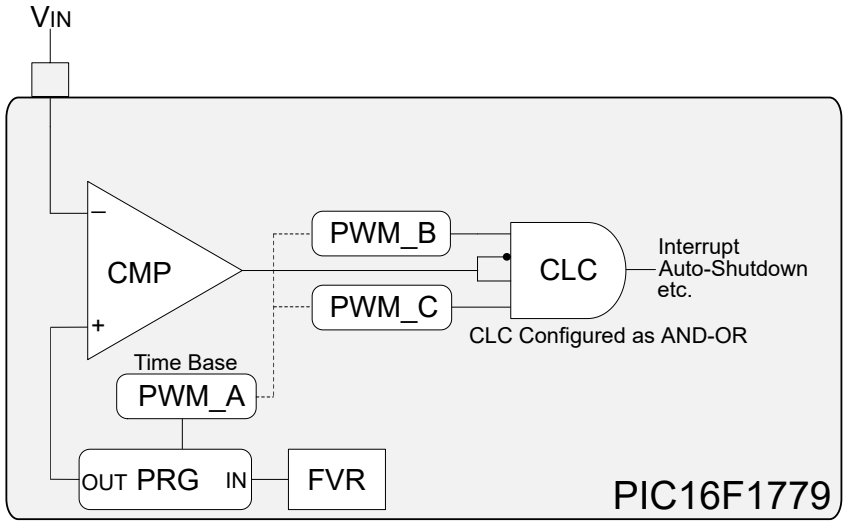
1. Detailed Description

The solution presented here uses a single comparator to convert the voltage level into a Pulse-Width Modulated (PWM) signal, with the help of the Programmable Ramp Generator (PRG) CIP as reference. The obtained signal is then used as two of the inputs to the Configurable Logic Cell (CLC) CIP configured as a four-input AND-OR that acts as a PWM signal comparator. The CLC has an output of logic '1', whenever an undervoltage or overvoltage event occurs and an output of logic '0', when the measured signal is in the desired interval. The output of the CLC is connected to the auto-shutdown of the Complementary Output Generator (COG) CIP, which in consequence will protect against OV and UV. The internal CIP connections are depicted in the figure below and the signals, in the figure following.

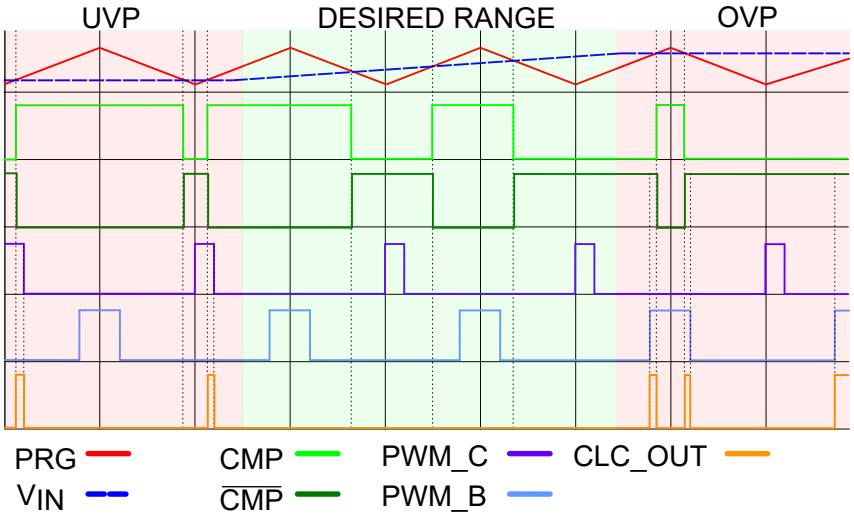
Figure 1-1. 1CMP Input UV and OV Protection Schematic



The intended usage of the solution is, in this case, an input undervoltage and overvoltage protection of a Switched Mode Power Supply (SMPS) control system implemented using CIPs, so other CIPs outside the needed ones will be referenced.

The comparator has as negative input, the measured voltage V_{IN} and as positive input, the PRG output signal configured as a sawtooth or triangular waveform. The output of the comparator converts the targeted measured voltage level as a duty cycle value to a PWM.

Figure 1-2. 1CMP Input UV and OV Protection Signals



The PRG triangular signal frequency dictates the comparator output signal period, so it can be considered as the sampling speed. The user has control over the slope, the rising and falling times, thus allowing them to decide on the sampling frequency and accepted magnitude of the measured voltage.

The Fixed Voltage Reference (FVR) is used to power the generated triangular wave.

The CLC is configured as an 'AND-OR' and acts as the PWM signals comparator. The output will go to logic '1' whether the monitored input voltage level is lower or higher than the desired limits and will remain as logic '0' when the voltage level is within the desired boundaries.

The first 'AND' has as inputs the PWM_C signal and CMP signal, so the output is generating a logic '1' only when the measured input voltage level is lower than the desired value. The second 'AND' has as inputs the negated CMP signal and PWM_B signal, so the output is generating a logic '1' only when the measured input voltage level is higher than the desired value.

PWM_C is used to set the desired minimum accepted input voltage level (UVP level, or the lower threshold reference) and is in sync with the comparator output PWM signal. The user can control the limit by changing the PWM_C duty cycle.

PWM_B is used to set the desired maximum accepted input voltage level (OVP level, or the higher threshold reference) and is also in sync with the comparator output PWM signal. The user can control the limit by changing the PWM_B duty cycle.

2. Test Setup

The following are used to test this function:

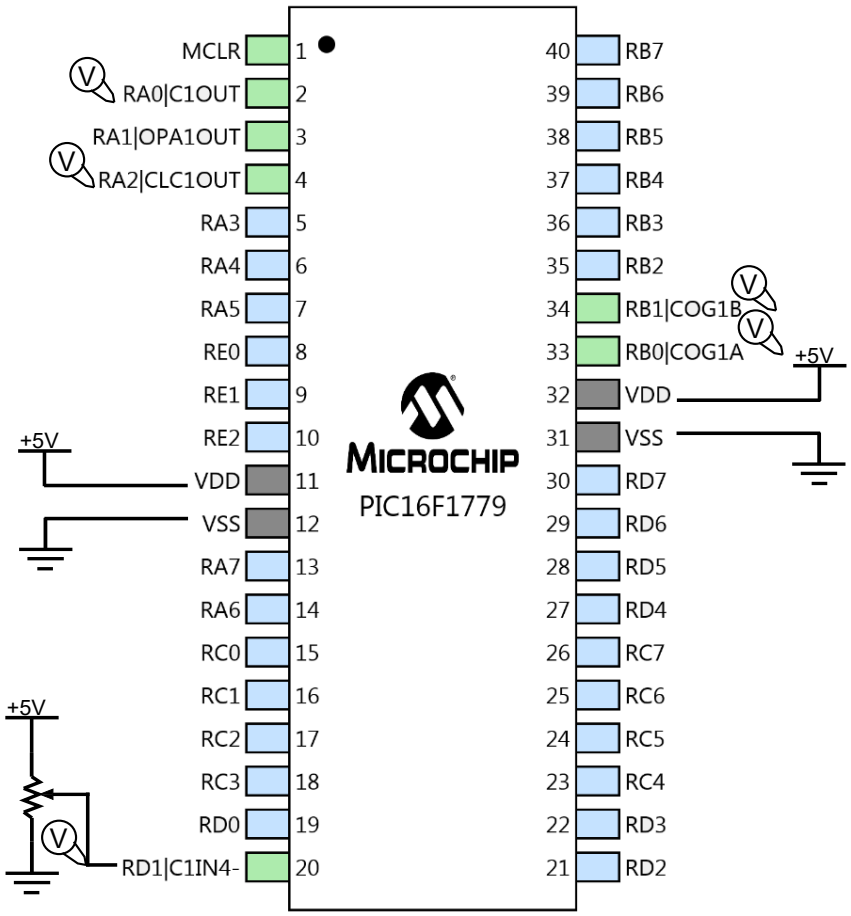
- One PICDEM™ LAB II board (or a prototyping board)
- One PIC16F1779 (any PIC16F176X/7X can be used as well)
- One potentiometer to simulate the variable input voltage, wires, MPLAB® PICkit™ 4 (any other PIC device programmer will work)
- One oscilloscope to verify the signals

The software used at the time of the tests are:

- MPLAB® X IDE v5.15
- MPLAB® Code Configurator v3.75
- MPLAB® XC8 compiler v2.05

The following figure depicts the test setup, where V_{DD} and GND are provided by PICkit 4. To power the board from the PICkit 4, right click on the current project, followed by Properties/PICkit 4/Option categories: Power, and check the box '**Power target circuit from PICkit 4**', then select **OK**.

Figure 2-1. Test Setup



The configurations are set using the MPLAB Code Configurator plug-in from MPLAB X with minor code intervention to start the PRG. After the configuration is done, the functions work independently of any core intervention.

PIC MCU Configurations:

- System module: System clock select – F_{OSC}, Internal Clock – 8 MHz_HF, PLL Enable

CIPs used:

- **TMR2**: Clock source – $F_{OSC}/4$, time period – 2 us (500 kHz switching frequency) – decides the SMPS switching frequency.
- **COG1**: Mode – Half-Bridge; Clock source – F_{OSC}; COGA PIN Steering – waveform; COGB PIN Steering – waveform; Rising event PWM3 – level trigger; Falling event PWM3 – level trigger; PWM3 low-to-high transition triggers the rising event of the COG and the high-to-low transition triggers the falling event, the dead-band delay set in the demo is 812.5 ns - this is the value that is used to control the high threshold and the low threshold, so the value must be adjusted according to the user's needs.
- **FVR**: FVR_buffer1 and FVR_buffer2 – 4x; 4.096V is used as the PRG source.
- **PRG**: Ramp generating mode – alternating ramp generator; Voltage input source – FVR_buffer1; Slope rate – 2.5V/us; Ramp rising timing source – PWM3_output/level sensitive/active_high, Ramp falling timing source – PWM3_output/Level sensitive/active_low, PRG is configured as alternating ramp generator; Slope rate: 2.5V/us.
- **PWM3**: Select timer – Timer2, duty cycle 50%, used as start ramp rising, start ramp falling for PRG, and as a signal source for the COG.
- **CMP1**: Positive input – PRG1; Negative input – CIN4, the negative input is connected to the equivalent of the input voltage or the measured signal, and the positive input is connected the PRG output. The output of the comparator will represent a PWM signal with the duty cycle equivalent and proportional to the measured voltage level.
- **CLC1**: Mode – AND–OR; AND1 Input is C1_OUT negated and COG1A; AND2 input is C1_OUT and COG1B. The output of the CLC can be connected directly to the auto-shutdown of the COG used for the SMPS loop (it is advised that you check the COG auto-shutdown tab in MCC to see which CLC is accepted as input). To stop the device when there is irregular input, an interrupt routine can be implemented to deal with the system during protection. The output expression in a Boolean notation is:

$$CLC1\_OUT = \overline{C1OUT}.COG1A + COG1B.C1OUT$$

- **OPA1**: Channel select: positive channel – PRG1_OUT and negative channel – 'anything' because is disabled; Set as 'Unity gain', this is used to monitor the internal PRG signal with the oscilloscope.

For more information on the CIPs see the PIC16F176X/7X product's data sheet.

The following figure depicts the MCC peripherals used, while the last figure shows the CLC connections made in MCC.

The lines of code added allow the PRG time to initialize and start when it is ready. The project example can be found in MPLAB® Xpress here.

```
while (!PRG1_IsReady());
PRG1_StartRampGeneration();
```

Figure 2-2. Code and PIN Configurations

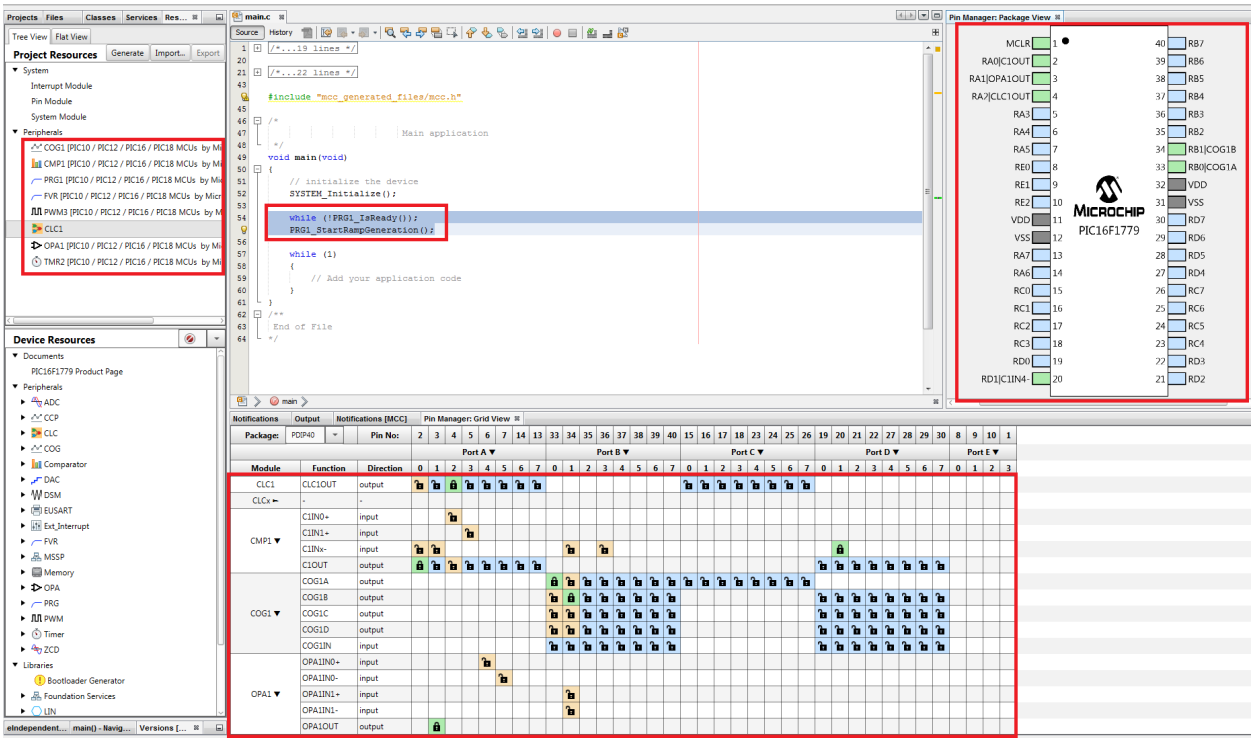
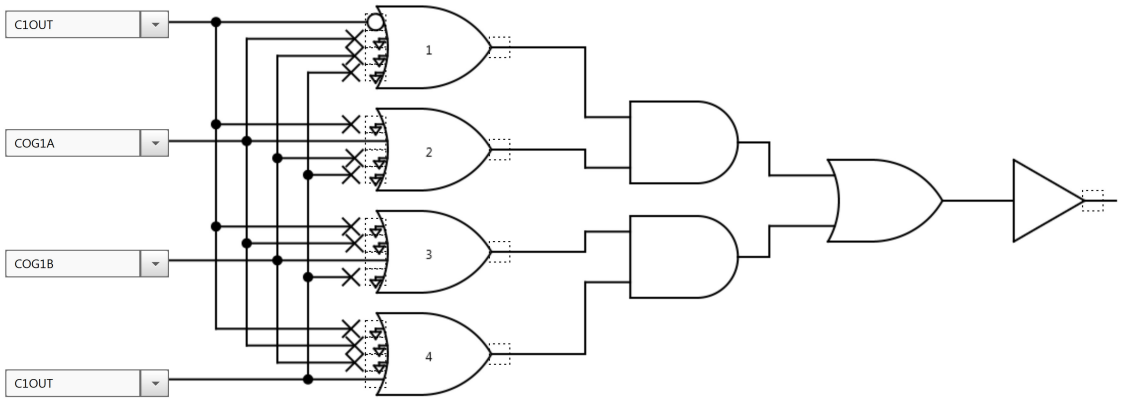


Figure 2-3. CLC Configuration



How to Set the Value of UV and OV

A number of variables must be taken in consideration to set the actual OV and UV level. First, the user must decide the input voltage divider, so the measured voltage is compatible with the sampling ramp maximum voltage. To calculate the PRG maximum reached voltage, use the equation below:

$$VPRG_{\max} = PRG_{slope} \times (T2Period \div 2)$$

This equation is valid only when the PWM that starts and stops the ramp is set to 50% duty-cycle and is powered from Timer2. PRG must be configured as alternate ramp generator. With the $VPRG_{max}$ known, the user can select the voltage divider which is used in equations as a subunit constant 'k'.

Next, the user must calculate the value of duty cycle present on the output of the comparator when the desired limits are reached. To do so, use the equation below:

$$C1OUT\_DC = \left(V_{IN} \times k\right) \div \left(VPRG_{\max}\right) \times 100\,\%$$

The value of the C1OUT_DC in UV condition (further used as DC_UV) and C1OUT_DC in OV condition (further used as DC_OV) will help calculate the dead-band delay necessary in COG1. The Dead-Band Rising (DBR) represents the OV limit and Dead-Band Falling (DBF), the UV limit. the desired values can be calculated using the equations below:

$$DBF = (T2Period \div 2) \times (1 - DC\_UV \div 100)$$

$$DBR = (T2Period \div 2) \times (DC\_OV \div 100)$$

Example

Vin: 7-20VDC

T2 period: 2us

PRG_{slope}: 2.5V/us

Using the first equation, the $VPRG_{max}$ = 2.5V. This means that the measured input voltage must not exceed 2.5V. With V_{IN} from 7-20V let's set OV:21V and UV:6V, a voltage divider of at least 1:10 (k = 0.1) must be placed before the input pin, which means the UV level is at 0.6V and the OV level at 2.1V. Using the second equation, the DC_UV = 24% and DC_OV = 84%.

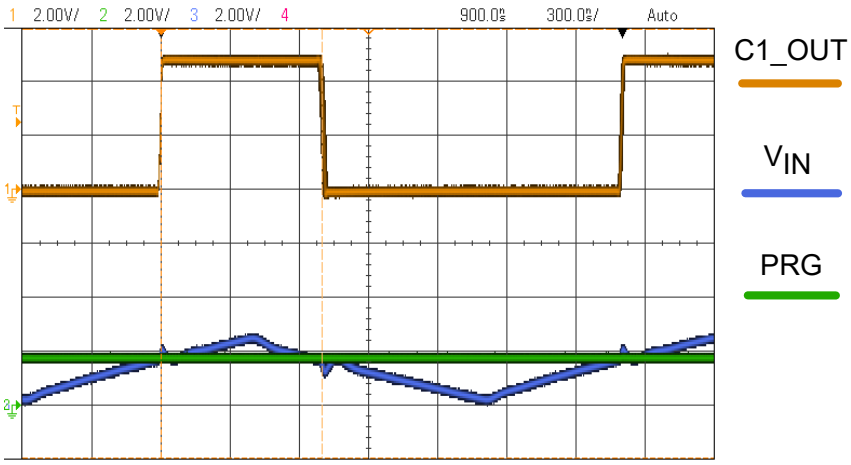
Finally, the dead-band delay values can be obtained using the last two equations, DBR = 840ns and DBF = 760ns.

3. Results

The following results were obtained using an oscilloscope to measure the required signals found at the pins depicted in Figure 2.1 and Figure 2.2. The results prove the correct functionality of the solution. Timer2 is the frequency source of the PWM3 and PWM3 is the rising and falling source for COG1 and PRG1. This provides synchronization between all the comparing signals.

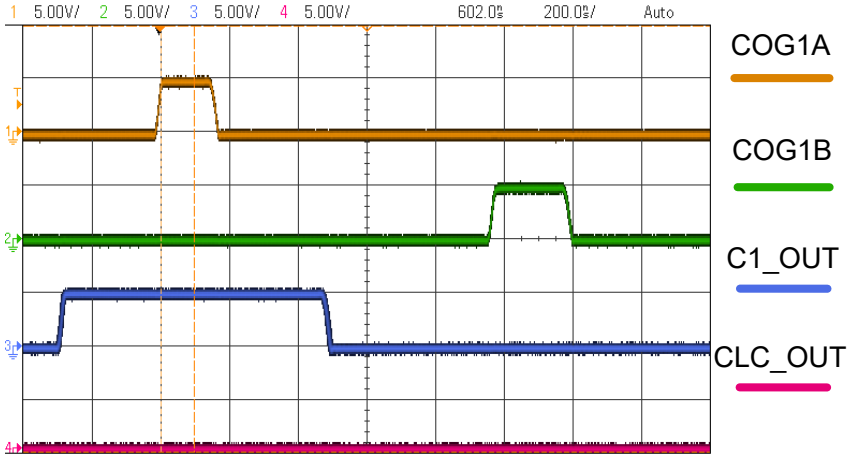
The following figure depicts the comparator output resulting from the comparison between the input voltage (sampled voltage) and the PRG ramp (sampling signal).

Figure 3-1. Comparator Output Based on VIN



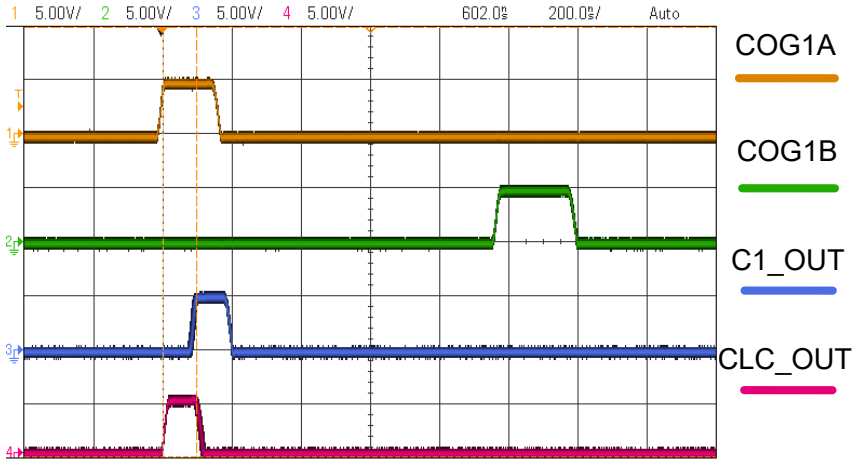
The following figure depicts the CLC1 output, when the measured input voltage is in the desired voltage window. For the SMPS application, this is equivalent with a safe input voltage operation.

Figure 3-2. Inside Voltage Window Operation



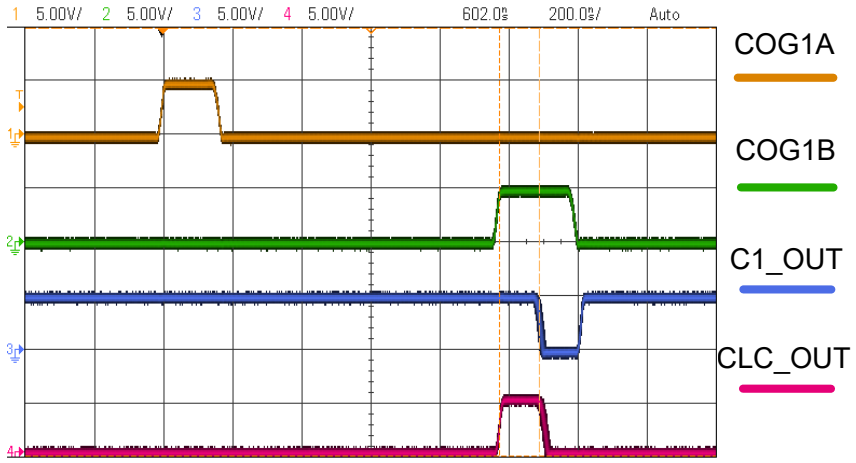
The following figure depicts the CLC1 output, when the measured input voltage is above the desired voltage window. For the SMPS application, this is equivalent with an input overvoltage detection.

Figure 3-3. Outside Voltage Window Operation OVP



The following figure depicts the CLC1 output, when the measured input voltage is below the desired voltage window. For the SMPS application, this is equivalent with an input undervoltage detection.

Figure 3-4. Outside Voltage Window Operation UVP



4. Conclusion

The solution presented in this technical brief solves the problem of voltage window detection by using a single comparator. The measured signal is converted into a PWM signal, where the duty cycle is equivalent to the voltage level and the threshold detection is implemented by the PWM signal comparison with logic cells.

The resulting function is faster than the ADC approach and does not need core supervision during the operation. It offers threshold configuration, change, and sampling speed selection.

The practical demonstration envisages a UVP and OVP example. This approach proves that the UV and OV protection function that usually needs two comparators and two voltage references can be implemented using a single comparator, if the designer transitions the comparison between four voltage signals into a comparison between four PWM signals.

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