

Advantages of NVSRAM Over FRAM

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INTRODUCTION

This technical brief describes the main advantages of NVSRAM over FRAM memory technology. Microchip's battery-backed SRAM devices have true unlimited read and write cycles, lower standby current, a wider voltage range and can be accessed via an SPI or SDI serial bus for fast data transfers. By simply adding a battery (as in [Figure 1](#)), the NVSRAM can retain data even after power loss. While the FRAM is a memory for long-term data storage, the NVSRAM is great for moving data in and out for applications, without worrying about read-write cycles, wear and power consumption. [Table 1](#) summarizes the main differences between FRAM and NVSRAM.

TABLE 1: KEY DIFFERENCES

	NVSRAM (SPI interface)	FRAM (SPI interface)
Supply voltage	2.5-5.5V	2-3.6V
Standby current	4 μ A	90 μ A
Max. data speed	20 MHz	40 MHz
Serial dual interface	Yes	No
Unlimited read/write cycles	Yes	No
Data retention	Until battery depletes	10 years
Temperature range	Industrial: -40°C to +85°C Storage: -65°C to +150°C	Industrial: -40°C to +85°C Storage: -55°C to 125°C
Packages	8-Lead SOIC 8-Lead PDIP 8-Lead TSSOP	8-Pin SOIC
Price per bit	Low	High

ADVANTAGES OF NVSRAM

There are several key features that make the NVSRAM a better solution than FRAM technology.

- **Unlimited write cycles:** the NVSRAM has true unlimited write cycles whereas the FRAM memory cell wears with every write.
- **Non-destructive reads:** the way the FRAM memory works is that for every read, the data is destroyed and it must be written back to the cell. This actually counts against the number of write cycles of the memory. But the way NVSRAM cell works means there is no destructive reading and the number of write cycles is truly infinite.
- **Data retention:** FRAM can store data for ten years. The NVSRAM data retention is limited only by the chosen battery.
- **Mode register:** the NVSRAM uses the mode register to select the mode of operation: Byte, Page or Sequential. The default state is sequential in which the internal address counter is automatically incremented and page boundaries are ignored. In Page mode, the reads and writes are limited to one page. When the last address of the page is reached, the internal address counter will roll over to the start of the page. In Byte mode, only one byte can be read or written to the device.

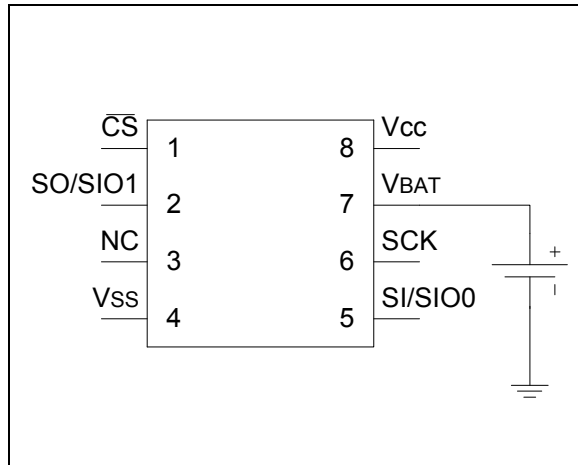
PIN DESCRIPTION

Both memories have the same communication interface, so they share some of the pin layout. The pins on the 23LCV512/23LCV1024 NVSRAM (see [Figure 1](#)) are explained below:

- $\overline{CS}$: Chip Select pin for SPI protocol. When $\overline{CS}$ is in pulled low, the chip is ready to accept commands. A high level deselects the device, allowing multiple devices to share the same data lines.
- SO/SIO1: data output pin. The device writes data to a master device through this pin on the falling edge of the serial clock.
- NC: not connected.
- Vss: ground pin
- SI/SIO0: data input pin. The device receives data from a master device on this pin and samples the bits on the rising edge of the serial clock, thus the memory may work only in (0,0) or (1,1) SPI modes.

- SCK: signal clock pin used to synchronize the communication between a master device and 23LCV512/23LCV1024. Data on the SI pin is latched on the rising edge and data on the SO pin is updated on the falling edge of SCK.
- VBAT: external backup supply input. It powers the device if VCC is below VTRIP point. It is recommended to connect VBAT to VSS, if it is not used.
- VCC: power supply pin.

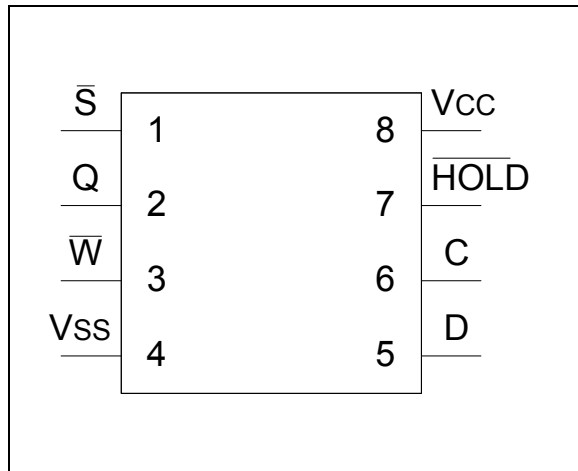
FIGURE 1: 23LCV512/23LCV1024 NVSRAM PIN LAYOUT



For FM25V10 (see [Figure 2](#)) the pins are:

- $\bar{S}$: chip select pin
- Q: data output pin
- $\bar{W}$: write protect
- VSS: ground pin
- D: data input pin
- C: signal clock pin
- $\overline{HOLD}$: hold pin
- VCC: power supply pin

FIGURE 2: FM25V10 FRAM PIN LAYOUT



Although they have different names, the data communication pins have the same position and function, so when migrating from the FM25V10 to the 23LCV512/23LCV1024, the only changes in pinout are the WP pin becomes a no-connect and the HOLD pin becomes VBAT. Additionally, the 23LCV512/23LCV1024 can work in SDI mode for faster data transfers. Thus, they use the SI and SO pins together for transferring two bits on a single clock pulse.

VOLTAGES

When moving from FRAM technology to SRAM, one must ensure the voltage applied to VCC pin is in the range specified in the data sheet. The 23LCV512/23LCV1024 have a wider voltage range (2.5-5.5V) and also have a significantly lower standby current (4 μ A) than the FRAM chips, making them usable across different types of circuits and power requirements.

For 23LCV512/23LCV1024 devices the VTRIP value is typically 1.8V (see data sheet). When VCC decreases below VTRIP, the memory cannot be accessed anymore, but its contents will be preserved if a battery is connected on the VBAT pin. In order to access the data, one must ensure the device is powered from VCC pin ($VCC > VTRIP$). The NVSRAM will retain data as long as the battery holds, unlike the FRAM, which will retain data for a limited time.

ENDURANCE

The 23LCV512/23LCV1024 uses volatile cell technology that provides a truly infinite number of writes. Accessing the array for reading does not destroy the data stored. In contrast, the FRAM technology uses ferroelectric cells that wear with every write. More so, when reading from a cell, the data is destroyed and has to be rewritten. This counts against the lifespan of the memory so the user has to estimate the number of reads and writes before implementing the application.

OPERATION MODES

SPI Mode

Just like the FRAM, the SRAM devices have an SPI interface in Slave mode for data transfer. To access the memory, a master device must first pull low the CS before generating clock pulses on the SCK pin. Only then, the memory can accept commands. For every byte received on the SI/SIO0 pin, the memory generates a byte on the SO/SIO1. For 23LCV1024 and 23LCV512 the maximum operating frequency is 20 MHz.

SDI Mode

In addition to SPI mode, the 23LCV512/23LCV1024 supports Serial Dual Interface, which means that for every clock pulse two bits are exchanged through the data lines, so both SI/SIO0 and SO/SIO1 are used. Thus, the data rate doubles for the same frequency (Figure 3 and Figure 4) allowing a maximum speed of

40 Mbps data rate to be achieved. To enter SDI mode, the EDIO command must be sent in SPI mode as in Figure 5. However, if the master resets before the SRAM, the user is required to verify the serial mode and reset it accordingly. To exit from SDI mode, the RSTIO command must be issued in the SDI format (Figure 6).

FIGURE 3: BYTE READ MODE SDI

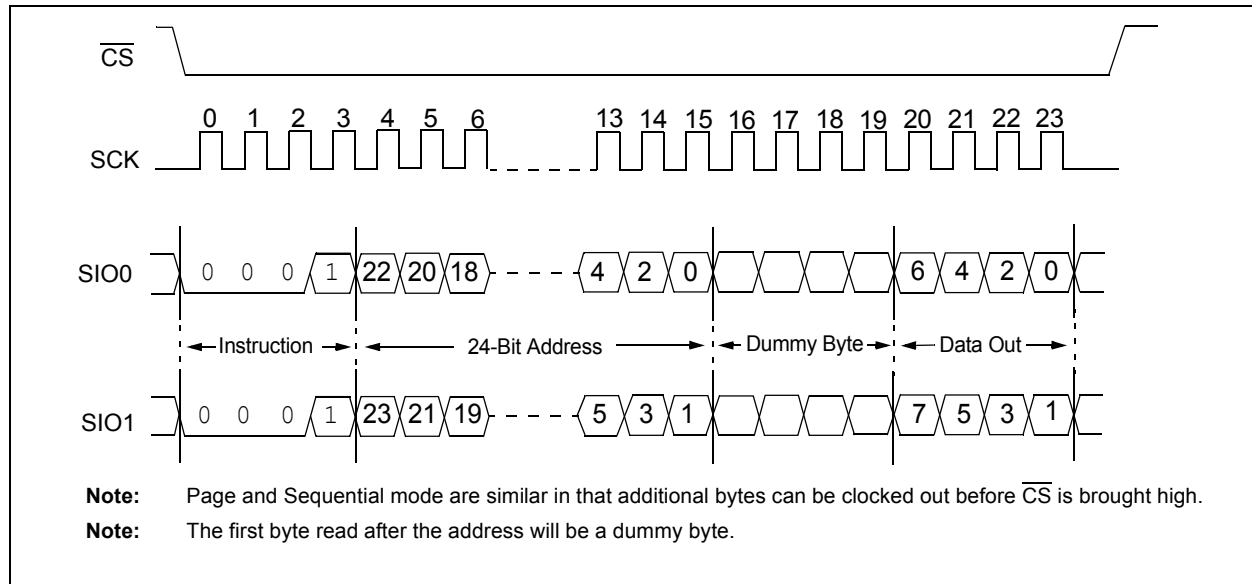


FIGURE 4: BYTE WRITE MODE SDI

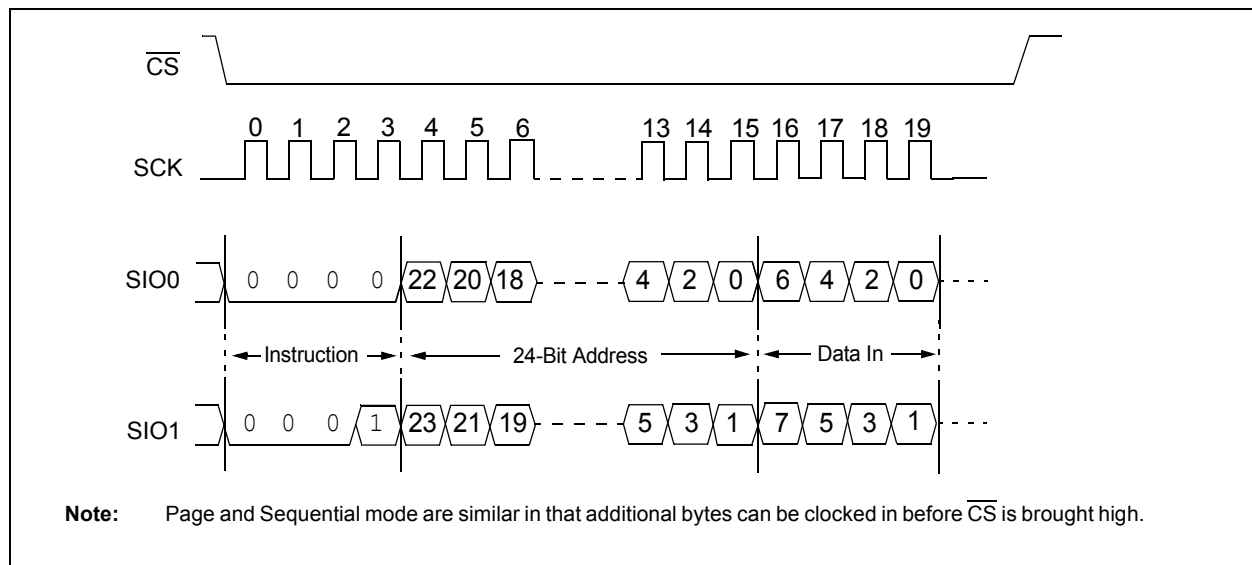


FIGURE 5: ENTER SDI MODE FROM SPI MODE

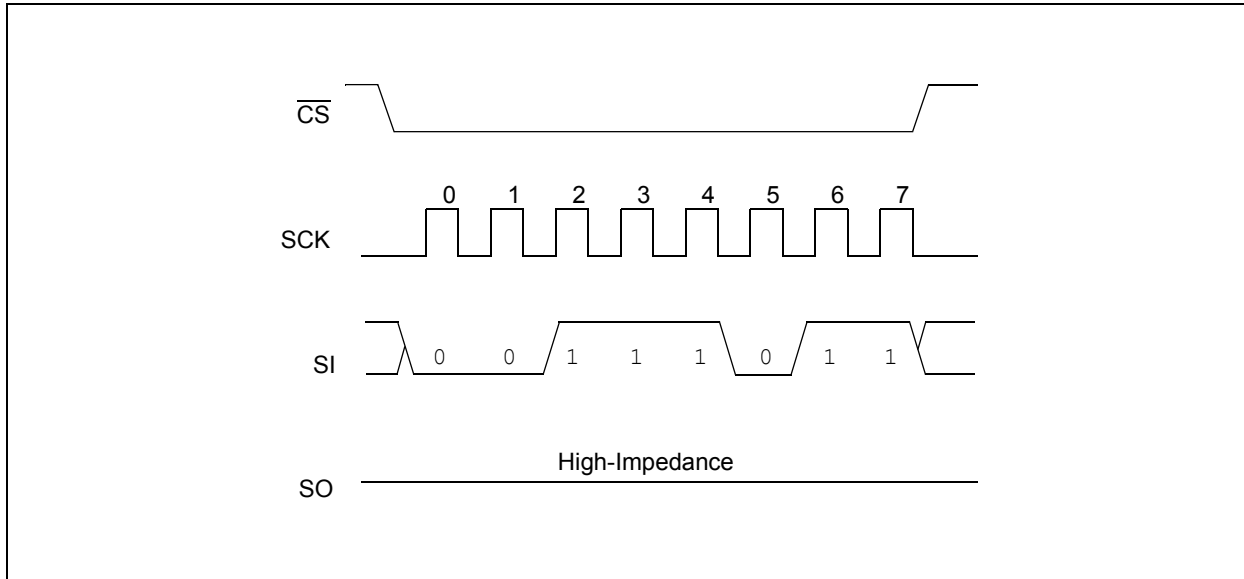
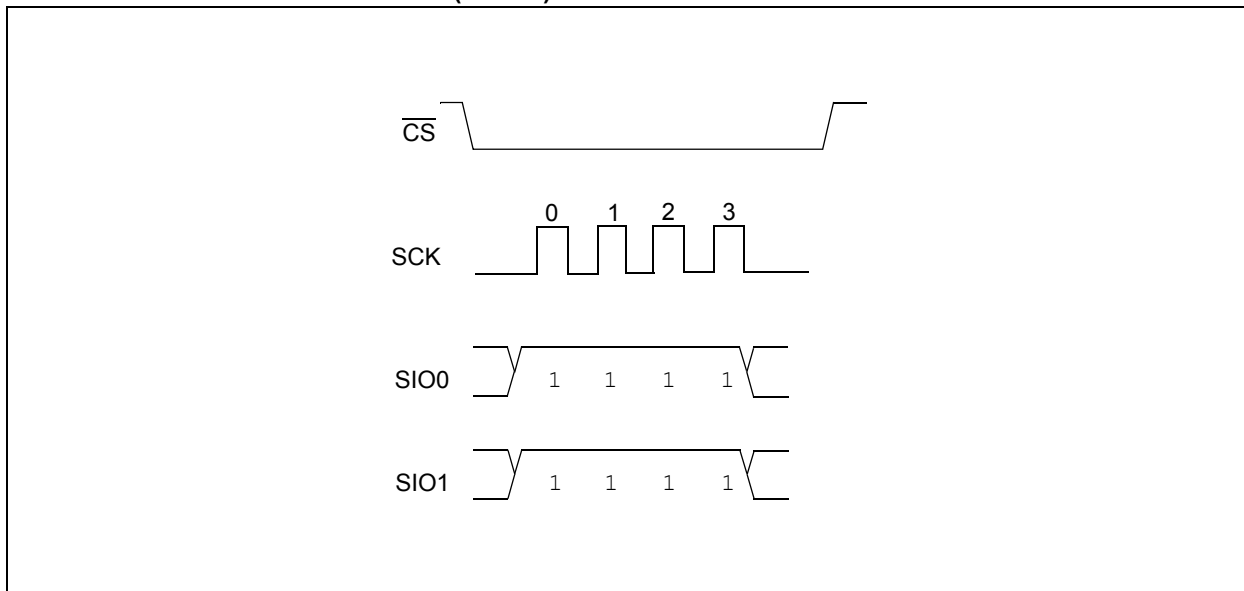


FIGURE 6: RESET SDI MODE (RSTIO) FROM SDI MODE



APPENDIX A: REVISION HISTORY

Revision A (06/2014)

Original release of this document.

NOTES:

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