MIC4604

85V Half-Bridge MOSFET Driver with up to 16V Programmable Gate Drive

Features

- AEC-Q100 Automotive Qualified, See Product Identification System (SOIC package only)
- 5.5V to 16V Gate Drive Supply Voltage Range
- Drives High-Side and Low-Side N-Channel MOSFETs with Independent Inputs
- TTL Input Thresholds
- On-Chip Bootstrap Diode
- Fast 39 ns Propagation Times
- Drives 1000 pF Load with 20 ns Rise and Fall Times
- Low Power Consumption
- Supplies Undervoltage Protection
- -40°C to +125°C Junction Temperature Range

Applications

- Power Inverters
- High Voltage Step-Down Regulators
- Half, Full, and 3-Phase Bridge Motor Drives
- Distributed Power Systems
- Computing Peripherals

General Description

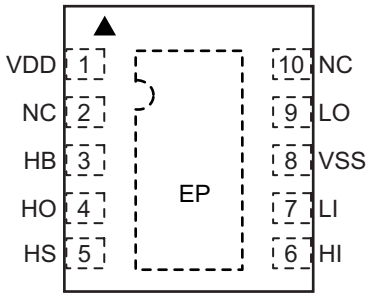
The MIC4604 is an 85V Half-Bridge MOSFET driver. The MIC4604 features fast 39 ns propagation delay times and 20 ns driver rise/fall times for a 1 nF capacitive load. The low-side and high-side gate drivers are independently controlled. The MIC4604 has TTL input thresholds. It includes a high-voltage internal diode that helps charge the high-side gate drive bootstrap capacitor.

A robust, high-speed, and low-power level shifter provides clean level transitions to the high-side output. The robust operation of the MIC4604 ensures that the outputs are not affected by supply glitches, HS ringing below ground, or HS slewing with high-speed voltage transitions. Undervoltage protection is provided on both the low-side and high-side drivers.

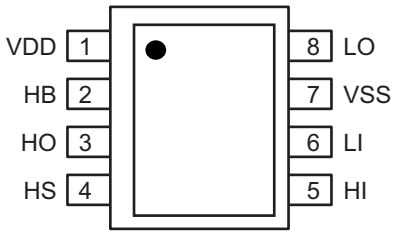
The MIC4604 is available in an 8-pin SOIC package and a tiny 10-pin 2.5 mm x 2.5 mm UDFN package. Both packages have an operating junction temperature range of -40°C to +125°C.

Package Types

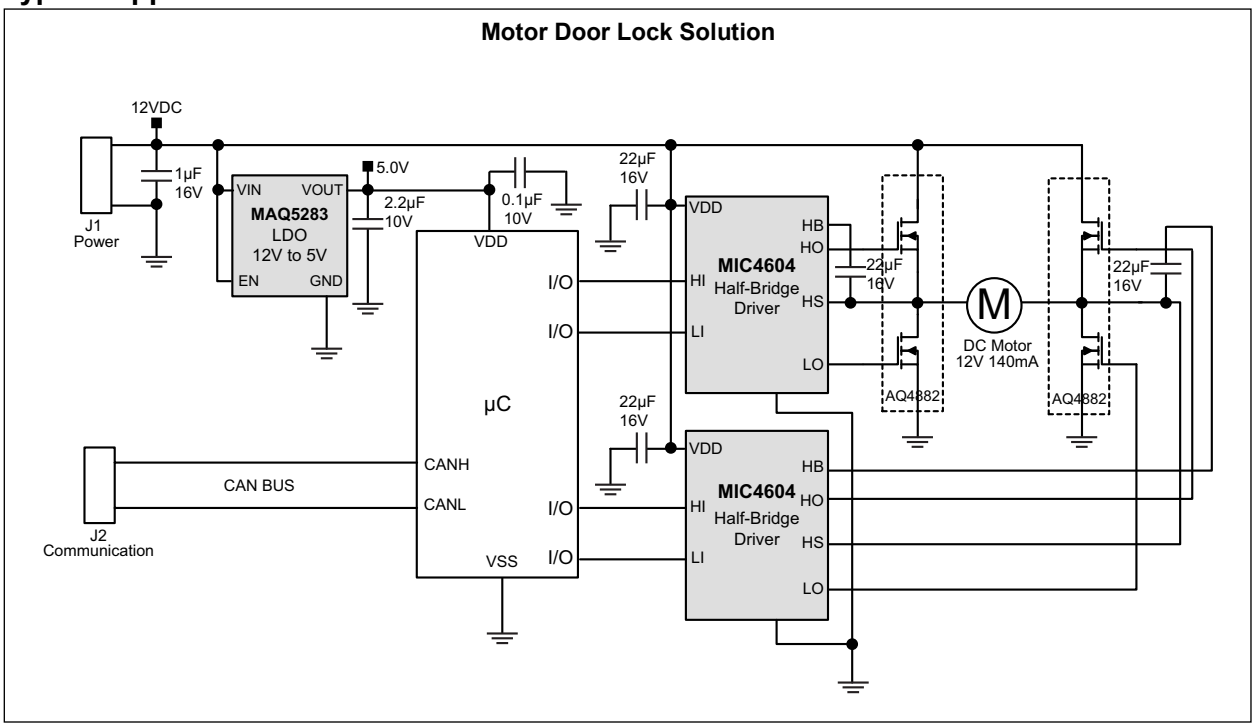
MIC4604YMT
10-Pin UDFN (MT)
(Top View)



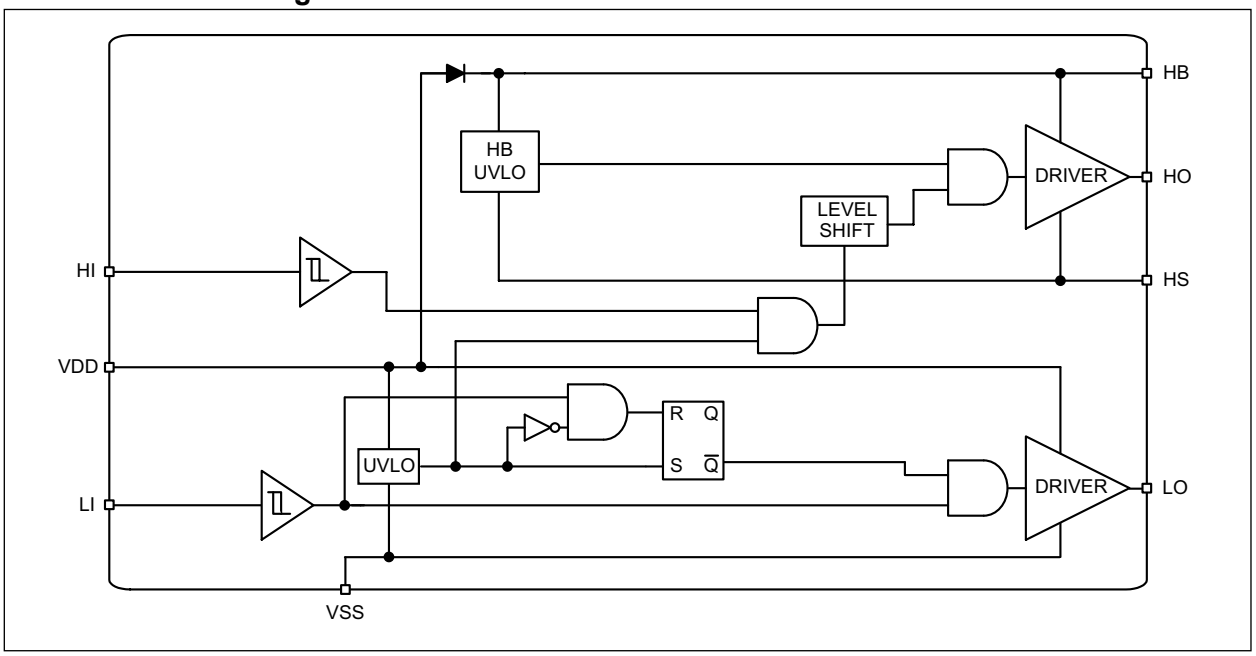
MIC4604YM
SOIC-8 (M)
(Top View)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage (V_{DD}, $V_{HB} – V_{HS}$) ..... -0.3V to +18V
Input Voltages (V_{LI}, V_{HI}, V_{EN}) ..... -0.3V to V_{DD} + 0.3V
Voltage on LO (V_{LO}) ..... -0.3V to V_{DD} + 0.3V
Voltage on HO (V_{HO}) ..... V_{HS} – 0.3V to V_{HB} + 0.3V
Voltage on HS (Continuous) ..... -0.3V to +90V
Voltage on HB ..... +108V
Average Current in V_{DD} to HB Diode ..... 100 mA
ESD Rating (Note 1) ..... HBM: 1.5 kV; MM: 200V

Operating Ratings‡

Supply Voltage (V_{DD}) [Decreasing V_{DD}] ..... +5.25V to +16V
Supply Voltage (V_{DD}) [Increasing V_{DD}] ..... +5.5V to +16V
Voltage on HS ..... -0.3V to +85V
Voltage on HS (Repetitive Transient) ..... -0.7V to +90V
HS Slew Rate ..... 50 V/ns
Voltage on HB ..... V_{HS} + 4.5V to V_{HS} + 16V
and/or ..... V_{DD} – 1V to V_{DD} + 85V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = V_{HB} = 12V; V_{SS} = V_{HS} = 0V; No load on LO or HO; T_A = +25°C; unless otherwise noted. **Bold** values indicate -40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current						
V_{DD} Quiescent Current	I_{DD}	—	48	**200**	µA	LI = HI = 0V
V_{DD} Operating Current	I_{DDO}	—	136	**300**	µA	f = 20 kHz
Total HB Quiescent Current	I_{HB}	—	20	**75**	µA	LI = HI = 0V or LI = 0V and HI = 5V
Total HB Operating Current	I_{HBO}	—	29	**200**	µA	f = 20 kHz
HB to V_{SS} Quiescent Current	I_{HBS}	—	0.5	5	µA	V_{HS} = V_{HB} = 90V
Input (LI, HI)						
Low-Level Input Voltage	V_{IL}	—	—	**0.8**	V	—
High-Level Input Voltage	V_{IH}	**2.2**	—	—	V	—
Input Voltage Hysteresis	V_{HYS}	—	0.05	—	V	—
Input Pull-Down Resistance	R_I	**100**	240	**500**	kΩ	—
Undervoltage Protection						
V_{DD} Falling Threshold	V_{DDF}	**4.0**	4.4	**4.9**	V	—
V_{DD} Threshold Hysteresis	V_{DDH}	—	0.21	—	V	Rising V_{DD} Threshold; V_{DDR} = V_{DDF} + V_{DDH}
HB Falling Threshold	V_{HBF}	**4.0**	4.4	**4.9**	V	—
HB Threshold Hysteresis	V_{HBH}	—	0.23	—	V	Rising V_{HB} Threshold; V_{HBR} = V_{HBF} + V_{HBH}
Bootstrap Diode						
Low-Current Forward Voltage	V_{DL}	—	0.42	**0.70**	V	I_{VDD-HB} = 100 µA
High-Current Forward Voltage	V_{DH}	—	0.75	**1.0**	V	I_{VDD-HB} = 50 mA
Dynamic Resistance	R_D	—	2.8	**5.0**	Ω	I_{VDD-HB} = 50 mA
LO Gate Driver						
Low-Level Output Voltage	V_{OLL}	—	0.17	**0.4**	V	I_{LO} = 50 mA
High-Level Output Voltage	V_{OHL}	—	0.25	**1.0**	V	I_{LO} = -50 mA, V_{OHL} = V_{DD} – V_{LO}
Peak Sink Current	I_{OHL}	—	1	—	A	V_{LO} = 5V
Peak Source Current	I_{OLL}	—	1	—	A	V_{LO} = 5V
HO Gate Driver						
Low-Level Output Voltage	V_{OLH}	—	0.2	**0.6**	V	I_{HO} = 50 mA
High-Level Output Voltage	V_{OHH}	—	0.22	**1.0**	V	I_{HO} = -50 mA, V_{OHH} = V_{HB} – V_{HO}
Peak Sink Current	I_{OHH}	—	1.5	—	A	V_{HO} = 5V
Peak Source Current	I_{OLH}	—	1	—	A	V_{HO} = 5V
Switching Specifications (Note 2)						
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}	—	37	**75**	ns	—
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}	—	34	**75**	ns	—
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}	—	39	**75**	ns	—
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}	—	33	**75**	ns	—

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DD} = V_{HB} = 12V; V_{SS} = V_{HS} = 0V; No load on LO or HO; T_A = +25°C; unless otherwise noted. **Bold** values indicate -40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Rise/Fall Time	$t_{RC/FC}$	—	20	—	ns	C_L = 1000 pF
Output Rise/Fall Time (3V to 9V)	$t_{R/F}$	—	0.8	—	µs	C_L = 0.1 µF
Minimum Input Pulse Width that Changes the Output	t_{PW}	—	50	—	ns	Note 3
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}	—	10	—	ns	—

Note 1: Specifications are for packaged product only.

2: Guaranteed by design. Not production tested.

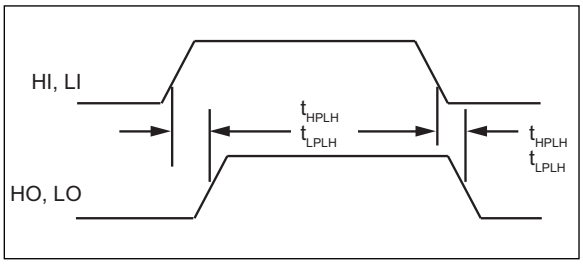
3: Minimum Input Pulse Width shorter than 200 ns should be avoided to prevent unpredicted behavior.

TEMPERATURE SPECIFICATIONS (Note 1)

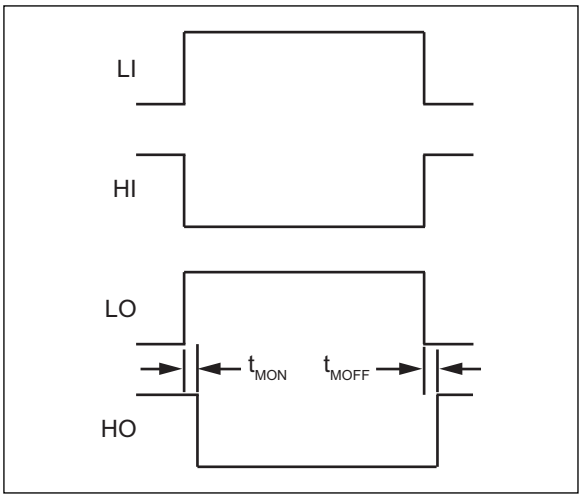
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature Range	T_J	-40	—	+125	°C	—
Storage Temperature Range	T_S	-60	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance UDFN-10Ld	θ_{JA}	—	53	—	°C/W	—
Thermal Resistance SOIC-8	θ_{JA}	—	145	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

Timing Diagrams



Note 1: All propagation delays are measured from the 50% voltage level.



2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

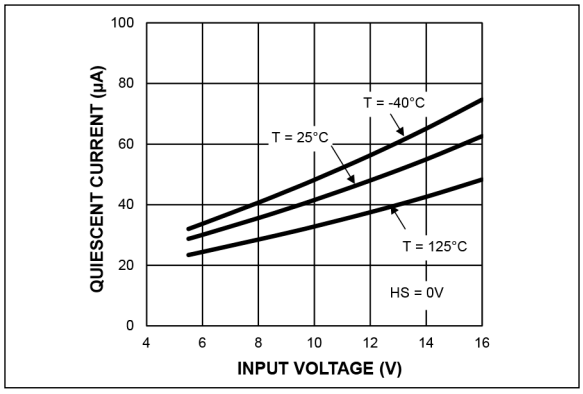


FIGURE 2-1: *Quiescent Current vs. Input Voltage.*

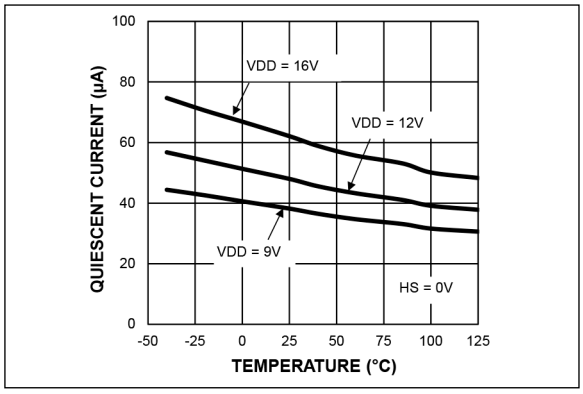


FIGURE 2-4: *Quiescent Current vs. Input Temperature.*

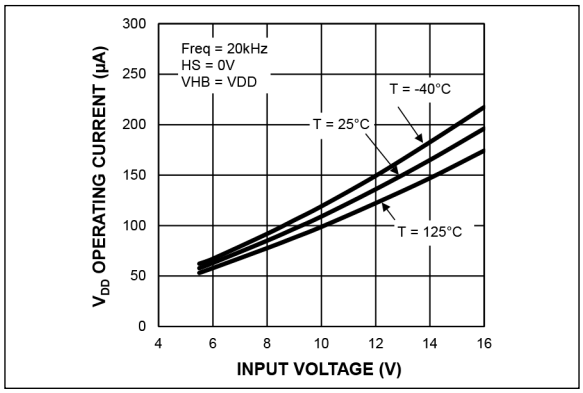


FIGURE 2-2: *V_{DD} Operating Current vs. Input Voltage.*

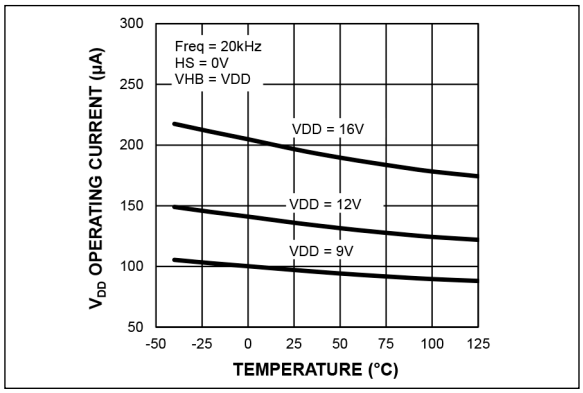


FIGURE 2-5: *V_{DD} Operating Current vs. Temperature.*

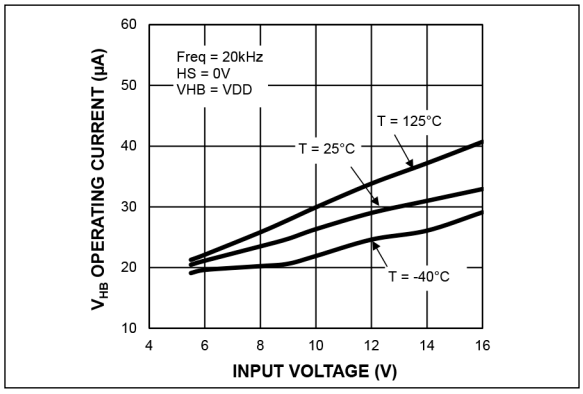


FIGURE 2-3: *V_{HB} Operating Current vs. Input Voltage.*

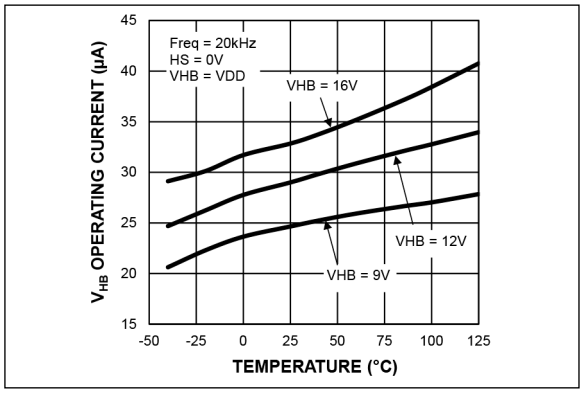


FIGURE 2-6: *V_{HB} Operating Current vs. Temperature.*

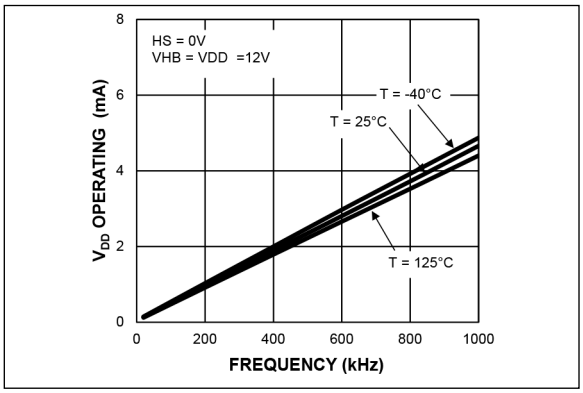


FIGURE 2-7: *V_{DD} Operating Current vs. Frequency.*

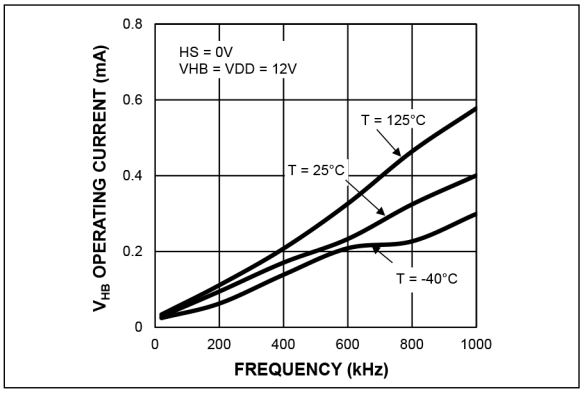


FIGURE 2-8: *V_{HB} Operating Current vs. Frequency.*

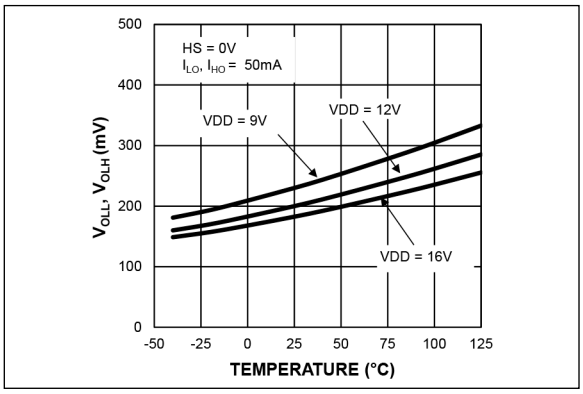


FIGURE 2-9: *Low Level Output Voltage vs. Temperature.*

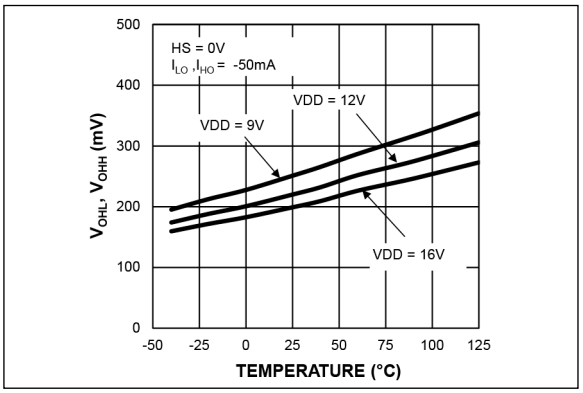


FIGURE 2-10: *High Level Output Voltage vs. Temperature.*

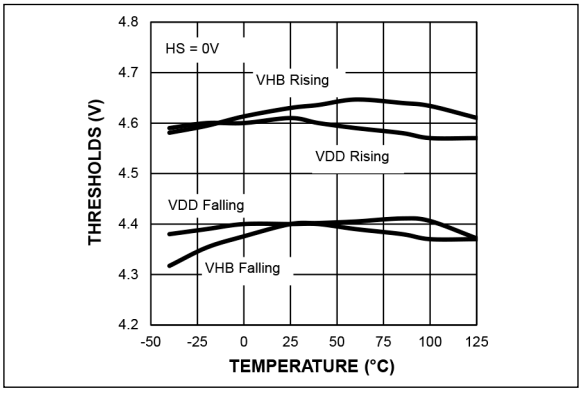


FIGURE 2-11: *UVLO Thresholds vs. Temperature.*

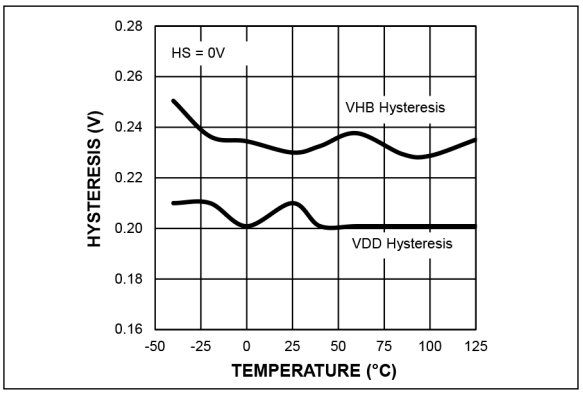


FIGURE 2-12: *UVLO Hysteresis vs. Temperature.*

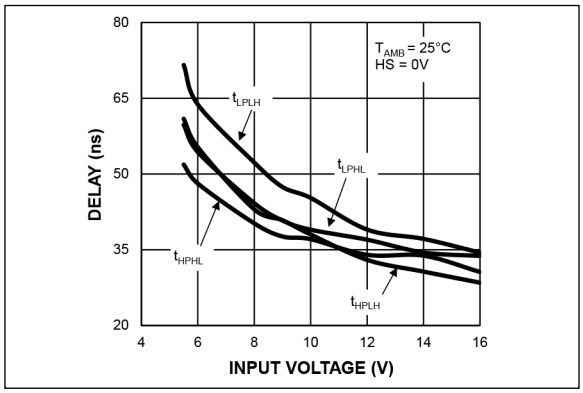


FIGURE 2-13: *Propagation Delay vs. Input Voltage.*

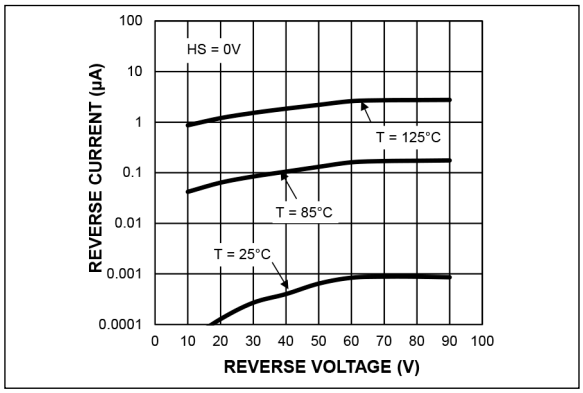


FIGURE 2-16: *Bootstrap Diode Reverse Current.*

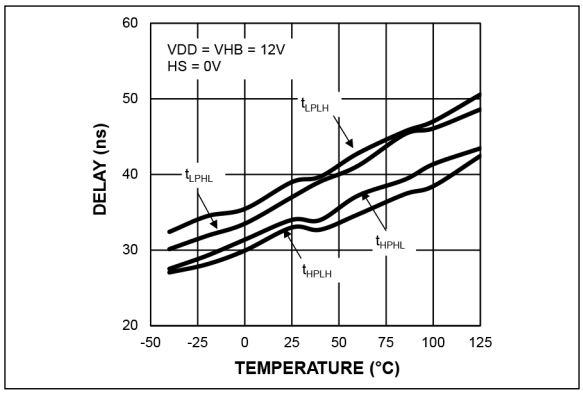


FIGURE 2-14: *Propagation Delay vs. Temperature.*

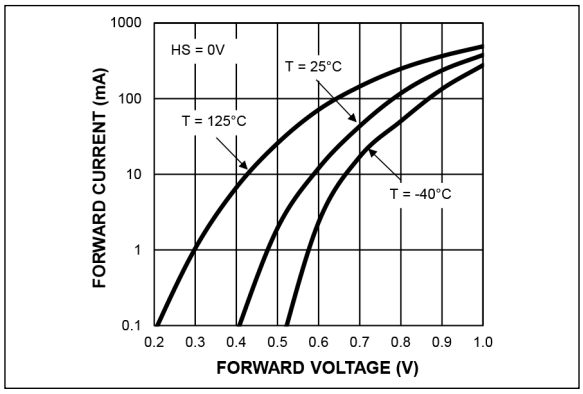


FIGURE 2-15: *Bootstrap Diode I-V Characteristics.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number UDFN	Pin Number SOIC	Pin Name	Description
1	1	VDD	Input supply for gate drivers. Decouple this pin to V_{SS} with a >2.2 µF capacitor. Anode connection to internal bootstrap diode.
2, 10	—	NC	No connect.
3	2	HB	High-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and HS. Cathode connection to internal bootstrap diode.
4	3	HO	High-side drive output. Connect to gate of the external high-side power MOSFET.
5	4	HS	High-side drive reference connection. Connect to source of the external high-side power MOSFET. Connect this pin to the bootstrap capacitor.
6	5	HI	High-side drive input.
7	6	LI	Low-side drive input.
8	7	VSS	Driver reference supply input. Connected to power ground of external circuitry and to source of low-side power MOSFET.
9	8	LO	Low-side drive output. Connect to gate of the external low-side power MOSFET.
EP	—	ePAD	Exposed pad. Connect to V_{SS}.

4.0 FUNCTIONAL DESCRIPTION

The MIC4604 is a high-voltage, noninverting, dual MOSFET driver that is designed to independently drive both high-side and low-side N-Channel MOSFETs (see the Functional Block Diagram).

Both drivers contain an input buffer with hysteresis, a UVLO circuit, and an output buffer. The high-side output buffer includes a high-speed level-shifting circuit that is referenced to the HS pin. An internal diode is used as part of a bootstrap circuit to provide the drive voltage for the high-side output.

4.1 Startup and UVLO

The UVLO circuit forces the driver output low until the supply voltage exceeds the UVLO threshold. The low-side UVLO circuit monitors the voltage between the VDD and VSS pins. The high-side UVLO circuit monitors the voltage between the HB and HS pins. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on.

4.2 Input Stage

Both the HI and LI pins of the MIC4604 are referenced to the V_{SS} pin. The voltage state of the input signal does not change the quiescent current draw of the driver.

The MIC4604 has a TTL-compatible input range and can be used with input signals with amplitude less than the supply voltage. The threshold level is independent of the V_{DD} supply voltage and there is no dependence between I_{VDD} and the input signal amplitude with the MIC4604. This feature makes the MIC4604 an excellent level translator that will drive high-threshold MOSFETs from a low-voltage PWM IC.

4.3 Low-Side Driver

A block diagram of the low-side driver is shown in Figure 4-1. The low-side driver is designed to drive a ground (V_{SS} pin) referenced N-channel MOSFET. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low $R_{DS(ON)}$ from the external MOSFET.

A high level applied to LI pin causes the upper driver MOSFET to turn on and V_{DD} voltage is applied to the gate of the external MOSFET. A low level on the LI pin turns off the upper driver and turns on the low side driver to ground the gate of the external MOSFET.

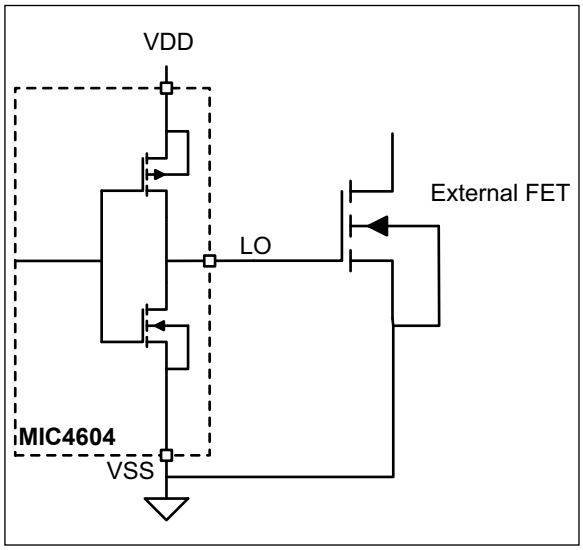


FIGURE 4-1: *Low-Side Driver Block Diagram.*

4.4 High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in Figure 4-2. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the HS pin.

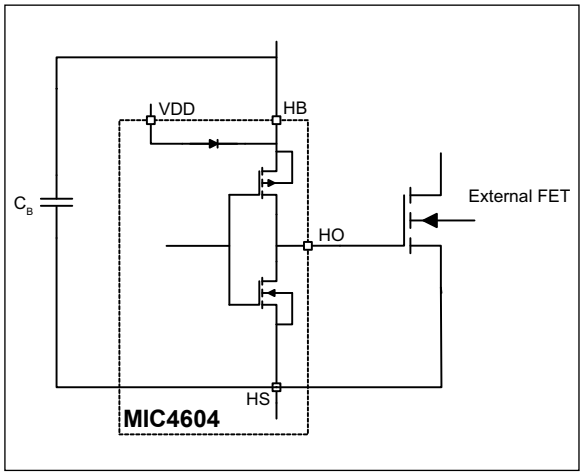


FIGURE 4-2: *High-Side Driver and Bootstrap Circuit Block Diagram.*

A low-power, high-speed, level-shifting circuit isolates the low-side (V_{SS} pin) referenced circuitry from the high-side (HS pin) referenced driver. Power to the high-side driver and UVLO circuit is supplied by the bootstrap circuit while the voltage level of the HS pin is shifted high.

The bootstrap circuit consists of an internal diode and external capacitor, C_B. In a typical application, such as the synchronous buck converter shown in Figure 4-3, the HS pin is at ground potential while the low-side

MOSFET is on. The internal diode allows capacitor C_B to charge up to $V_{DD} – V_F$ during this time (where V_F is the forward voltage drop of the internal diode). After the low-side MOSFET is turned off and the HO pin turns on, the voltage across capacitor C_B is applied to the gate of the upper external MOSFET. As the upper MOSFET turns on, voltage on the HS pin rises with the source of the high-side MOSFET until it reaches V_{IN}. As the HS and HB pin rise, the internal diode is reverse biased preventing capacitor C_B from discharging.

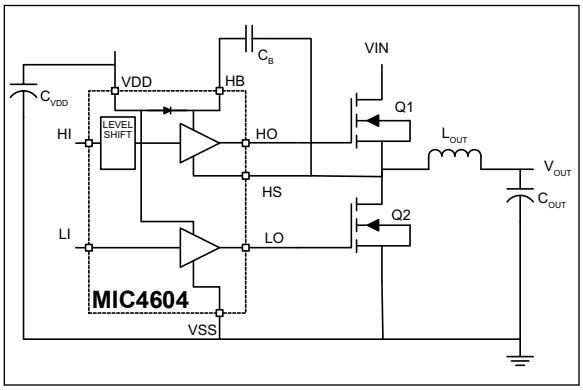


FIGURE 4-3: *High-Side Driver and Bootstrap Circuit Block Diagram.*

4.5 Programmable Gate Drive

The MIC4604 offers programmable gate drive, which means the MOSFET gate drive (gate-to-source voltage) equals the V_{DD} voltage. This feature offers designers flexibility in driving the MOSFETs. Different MOSFETs require different V_{GS} characteristics for optimum $R_{DS(ON)}$ performance. Typically, the higher the gate voltage (up to 16V), the lower the $R_{DS(ON)}$ achieved. For example, a 4899 MOSFET can be driven to the ON state at 4.5V gate voltage but $R_{DS(ON)}$ is 7.5 mΩ. If driven to 10V gate voltage, $R_{DS(ON)}$ is 4.5 mΩ. In low-current applications, the losses due to $R_{DS(ON)}$ are minimal, but in high-current applications such as power hand tools, the difference in $R_{DS(ON)}$ can cut into the efficiency budget.

In portable hand tools and other battery-powered applications, the MIC4604 offers the ability to drive motors at a lower voltage compared to the traditional MOSFET drivers because of the wide V_{DD} range (5.5V to 16V). Traditional MOSFET drivers typically require a V_{DD} greater than 9V. The MIC4604 drives a motor using only two Li-ion batteries (total 7.2V) compared to traditional MOSFET drivers which will require at least three cells (total of 10.8V) to exceed the minimal V_{DD} range. As an additional benefit, the low 5.5V gate drive capability allows a longer run time. This is because the Li-ion battery can run down to 5.5V, which is just above its 4.8V minimum recommended discharge voltage. This is also a benefit in higher current power tools that use five or six cells. The driver can be operated up to 16V to minimize the $R_{DS(ON)}$ of the MOSFETs and use as much of the discharge battery pack as possible for a longer run time. For example, an 18V battery pack can be used to the lowest operating discharge voltage of 13.5V.

5.0 APPLICATION INFORMATION

5.1 HS Pin Clamp

A resistor/diode clamp between the switch node and the HS pin is necessary to clamp large negative glitches or pulses on the HS pin.

Figure 5-1 shows the Phase A section high-side and low-side MOSFETs connected to one phase of the three phase motor. There is a brief period of time (dead time) between switching to prevent both MOSFETs from being on at the same time. When the high-side MOSFET is conducting during the on-time state, current flows into the motor. After the high-side MOSFET turns off—but before the low-side MOSFET turns on—current from the motor flows through the body diode in parallel with the low-side MOSFET. Depending upon the turn-on time of the body diode, the motor current, and circuit parasitics, the initial negative voltage on the switch node can be several volts or more. The forward voltage drop of the body diode can be several volts, depending on the body diode characteristics and motor current.

Even though the HS pin is rated for negative voltage, it is good practice to clamp the negative voltage on the HS pin with a resistor and possibly a diode to prevent excessive negative voltage from damaging the driver. Depending upon the application and amount of negative voltage on the switch node, a 3Ω resistor is recommended. If the HS pin voltage exceeds 0.7V, a diode between the HS pin and ground is recommended. The diode reverse voltage rating must be greater than the high voltage input supply (V_{IN}). Larger values of resistance can be used if necessary.

Adding a series resistor in the switch node limits the peak high-side driver current during turn-off, which affects the switching speed of the high-side driver. The resistor in series with the HO pin may be reduced to help compensate for the extra HS pin resistance.

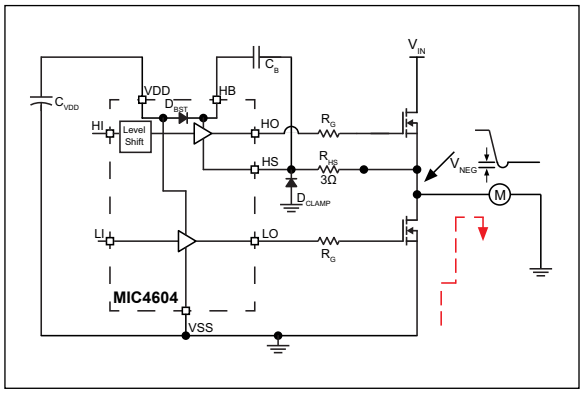


FIGURE 5-1: *Negative HS Pin Voltage.*

5.2 Power Dissipation Considerations

Power dissipation in the driver can be separated into three areas:

- Internal diode dissipation in the bootstrap circuit
- Internal driver dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

5.3 Bootstrap Circuit Power Dissipation

Power dissipation of the internal bootstrap diode primarily comes from the average charging current of the C_B capacitor multiplied by the forward voltage drop of the diode. Secondary sources of diode power dissipation are the reverse leakage current and reverse recovery effects of the diode.

The average current drawn by repeated charging of the high-side MOSFET is calculated by:

EQUATION 5-1:

$$I_{F(AVE)} = Q_{GATE} \times f_S$$

Where:

Q_{GATE}	Total gate charge at V_{HB}
f_S	Gate drive switching frequency

The average power dissipated by the forward voltage drop of the diode equals:

EQUATION 5-2:

$$P_{DIODEfwd} = I_{F(AVE)} \times V_F$$

Where:

V_F	Diode forward voltage drop

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The reverse leakage current of the internal bootstrap diode is typically 2 µA at a reverse voltage of 85V at 125°C. Power dissipation due to reverse leakage is typically much less than 1 mW and can be ignored.

Reverse recovery time is the time required for the injected minority carriers to be swept away from the depletion region during turn-off of the diode. Power dissipation due to reverse recovery can be calculated by computing the average reverse current due to reverse recovery charge times the reverse voltage across the diode. The average reverse current and power dissipation due to reverse recovery can be estimated by:

EQUATION 5-3:

$$I_{RR(AVE)} = 0.5 \times I_{RRM} \times t_{RR} \times f_S$$

Where:

I_{RRM}	Peak reverse recovery current
t_{RR}	Reverse recovery time

EQUATION 5-4:

$$P_{DIODErr} = I_{RR(AVE)} \times V_{REV}$$

The total diode power dissipation is:

EQUATION 5-5:

$$P_{DIODEtotal} = P_{DIODEfwd} + P_{DIODErr}$$

An optional external bootstrap diode may be used instead of the internal diode (Figure 5-2). An external diode may be useful if high gate charge MOSFETs are being driven and the power dissipation of the internal diode is contributing to excessive die temperatures. The voltage drop of the external diode must be less than the internal diode for this option to work. The reverse voltage across the diode will be equal to the input voltage minus the V_{DD} supply voltage. The above equations can be used to calculate power dissipation in the external diode; however, if the external diode has significant reverse leakage current, the power dissipated in that diode due to reverse leakage can be calculated as:

EQUATION 5-6:

$$P_{DIODErev} = I_R \times V_{REV} \times (1 - D)$$

Where:

I_R	Reverse current flow at V_{REV} and T_J
V_{REV}	Diode reverse voltage
D	Duty cycle. ($t_{ON} \times f_S$)

The on-time is the time the high-side switch is conducting. In most topologies, the diode is reverse biased during the switching cycle off-time.

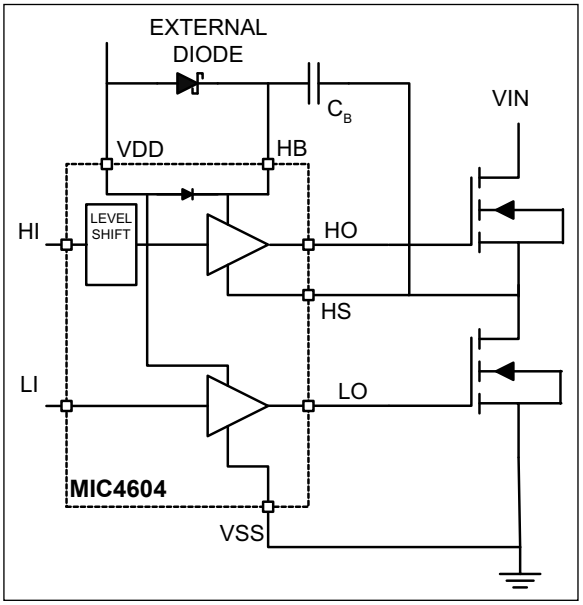


FIGURE 5-2: *Optional Bootstrap Diode.*

5.4 Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 5-3 shows a simplified equivalent circuit of the MIC4604 driving an external MOSFET.

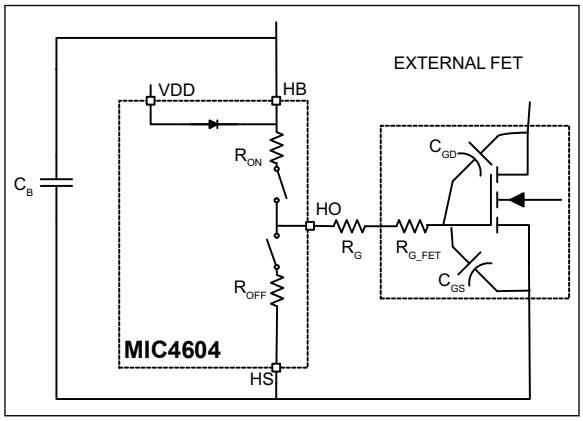


FIGURE 5-3: *MIC4604 Driving an External MOSFET.*

5.4.1 DISSIPATION DURING THE EXTERNAL MOSFET TURN-ON

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G, and R_{G_FET}. R_{ON} is the on resistance of the upper driver MOSFET in the MIC4604. R_G is the series resistor (if any) between the driver IC and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET. R_{G_FET} is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored because they are much less than R_{ON} and R_{G_FET}.

The effective capacitances of C_{GD} and C_{GS} are difficult to calculate because they vary nonlinearly with I_D, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge versus V_{GS}. Figure 5-4 shows a typical gate charge curve for an arbitrary power MOSFET. This chart shows that for a gate voltage of 10V, the MOSFET requires about 23.5 nC of charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

EQUATION 5-7:

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^{2}$$

but

$$Q = C \times V$$

so

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$

Where:

C_{ISS}	Total gate capacitance of the MOSFET

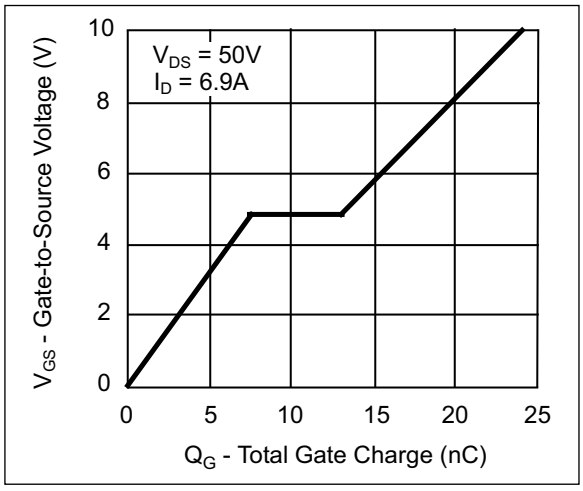


FIGURE 5-4: *Typical Gate Charge vs. V_{GS}.*

The same energy is dissipated by R_{OFF}, R_G, and R_{G_FET} when the driver IC turns the MOSFET off. Assuming R_{ON} is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is:

EQUATION 5-8:

$$E_{DRIVER} = Q_G \times V_{GS}$$

and

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where:

E_{DRIVER}	Energy dissipated per switching cycle
P_{DRIVER}	Power dissipated per switching cycle
Q_G	Total gate charge at V_{GS}
V_{GS}	Gate-to-source voltage on the MOSFET
f_S	Switching frequency of the gate drive circuit

The power dissipated inside the MIC4604 is equal to the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting R_{ON} = R_{OFF}, the power dissipated in the MIC4604 due to driving the external MOSFET is:

EQUATION 5-9:

$$P_{DISSdriver} = P_{DRIVER} \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}}$$

5.5 Supply Current Power Dissipation

Power is dissipated in the MIC4604 even if nothing is being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry, and shoot-through current in the output drivers. The supply current is proportional to operating frequency and the V_{DD} and V_{HB} voltages. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC4604 due to supply current is:

EQUATION 5-10:

$$P_{DISSsupply} = V_{DD} \times I_{DD} + V_{HB} \times I_{HB}$$

5.6 Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4604 is equal to the power dissipation caused by driving the external MOSFETs, the supply current and the internal bootstrap diode.

EQUATION 5-11:

$$P_{DISStotal} = P_{DISSsupply} + P_{DISSdrive} + P_{DIODEtotal}$$

The die temperature can be calculated after the total power dissipation is known.

EQUATION 5-12:

$$T_J = T_A + P_{DISStotal} \times \theta_{JA}$$

Where:

T_J	Junction temperature (°C)
T_A	Maximum ambient temperature
$P_{DISStotal}$	Power dissipation of the MIC4604
θ_{JA}	Thermal resistance from junction to ambient air

5.7 Propagation Delay and Other Timing Considerations

Propagation delay and signal timing are important considerations. Many power supply topologies use two switching MOSFETs operating 180° out of phase from each other. These MOSFETs must not be on at the same time or a short circuit will occur, causing high peak currents and higher power dissipation in the MOSFETs. The MIC4604 output gate drivers are not designed with anti-shoot-through protection circuitry. The output drive signals simply follow the inputs. The power supply design must include timing delays (dead-time) between the input signals to prevent shoot-through.

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high side on-time to switching period) is controlled by the minimum pulse width of the low side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

5.8 Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low-side (V_{DD}) and high-side (HB) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from HB to HS has two functions: it provides decoupling for the high-side circuitry and also provides current to the high-side circuit while the high-side external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended because of the large change in capacitance over temperature and voltage. A minimum value of 0.1 µF is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends on the supply voltage, ambient temperature and the voltage derating used for reliability. 25V rated X5R or X7R ceramic capacitors are recommended for most applications. The minimum capacitance value should be increased if low voltage capacitors are used because even good quality dielectric capacitors, such as X5R, will lose 40% to 70% of their capacitance value at the rated voltage.

Placement of the decoupling capacitors is critical. The bypass capacitor for V_{DD} should be placed as close as possible between the V_{DD} and V_{SS} pins. The bypass capacitor (C_B) for the HB supply pin must be located as

close as possible between the HB and HS pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the section on Grounding, Component Placement, and Circuit Layout for more information.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus V_{GS} voltage. Based on this information and a recommended ΔV_{HB} of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

EQUATION 5-13:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{HB}}$$

Where:

Q_{GATE}	Total gate charge at V_{HB}
ΔV_{HB}	Voltage drop at the HB pin

The decoupling capacitor for the V_{DD} input may be calculated in with the same formula; however, the two capacitors are usually equal in value.

5.9 Grounding, Component Placement, and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4604 drivers require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

Figure 5-5 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the HB pin and out the HO pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor C_B. The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor C_B must be placed close to the HB and HS pins. This capacitor not only provides all the energy for turn-on but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.

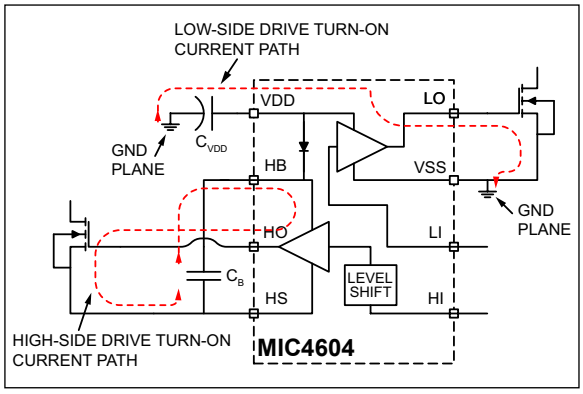


FIGURE 5-5: *Turn-On Current Paths.*

Figure 5-6 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_B.

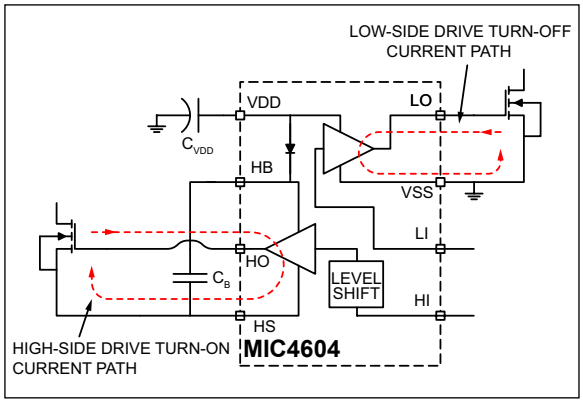


FIGURE 5-6: *Turn-Off Current Paths.*

5.10 DC Motor Applications

MIC4604 MOSFET drivers are widely used in DC motor applications. They address brushed motors in both half-bridge and full-bridge motor topologies as well as 3-phase brushless motors. As shown in Figure 5-7, Figure 5-8, and Figure 5-9, the drivers

switch the MOSFETs at variable duty cycles that modulate the voltage to control motor speed. In the half-bridge topology, the motor turns in one direction only. The full-bridge topology allows for bidirectional control. 3-Phase motors are more efficient compared to the brushed motors but require three half-bridge switches and additional circuitry to sense the position of the rotor.

The MIC4604 85V operating voltage offers the engineer margin to protect against Back Electromotive Force (EMF) which is a voltage spike caused by the rotation of the rotor. The Back EMF voltage amplitude depends on the speed of the rotation. It is good practice to have at least twice the HV voltage of the motor supply. 85V is plenty of margin for 12V, 24V, and 40V motors.

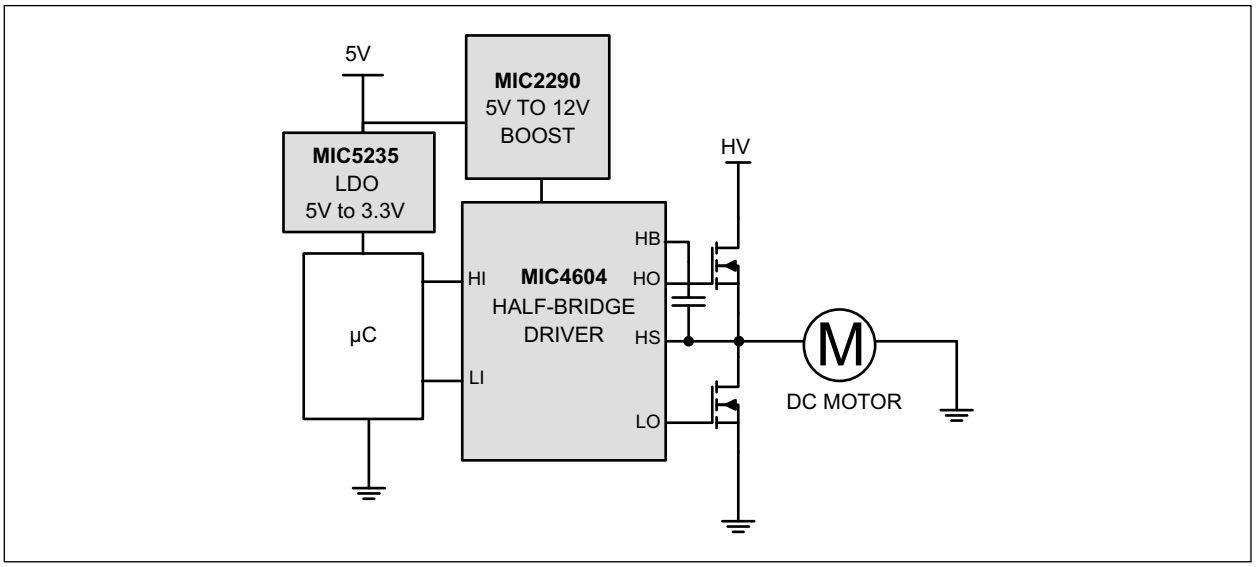


FIGURE 5-7: *Half-Bridge DC Motor.*

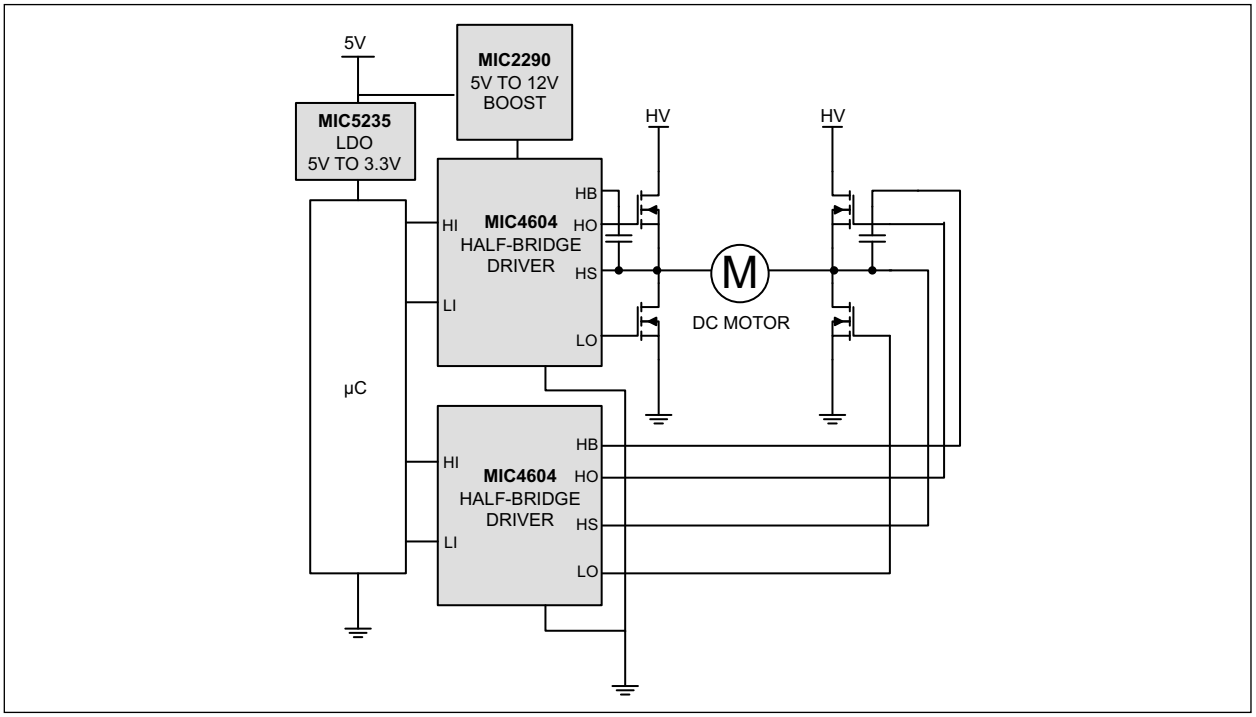


FIGURE 5-8: *Full-Bridge DC Motor.*

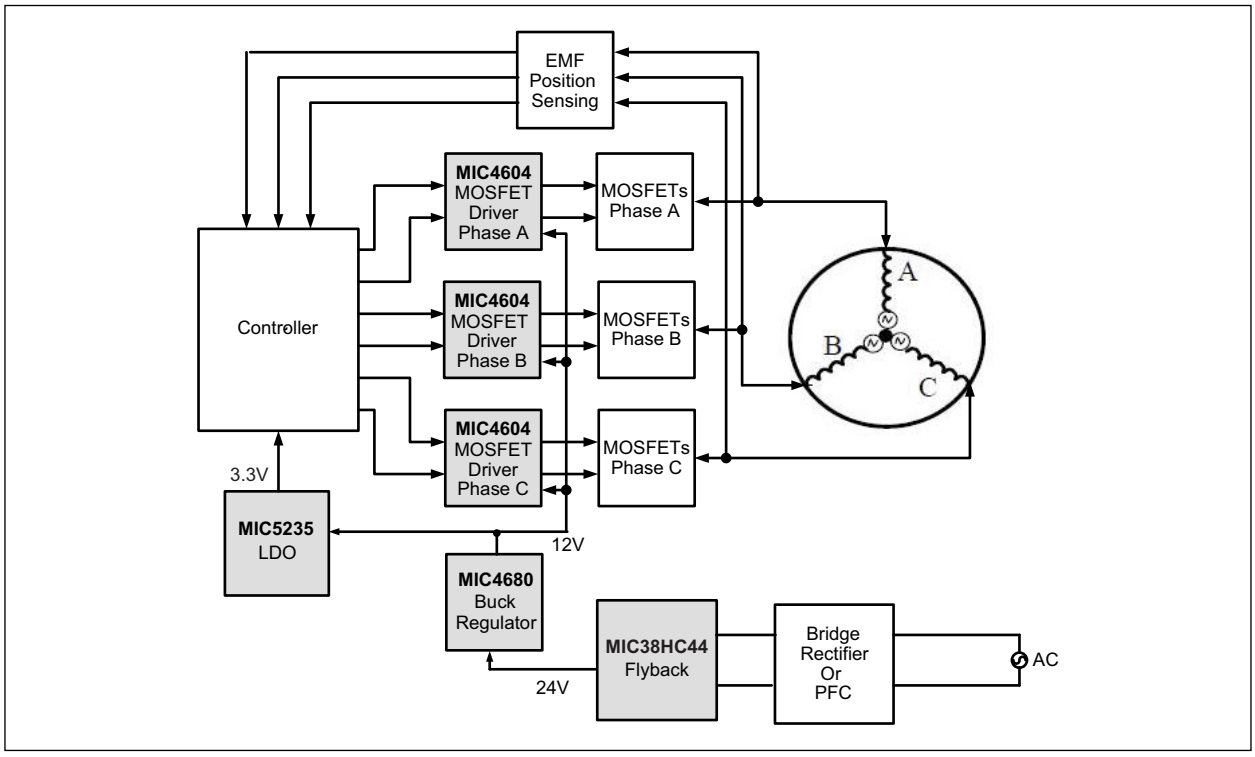


FIGURE 5-9: *3-Phase Brushless DC Motor Driver – 24V Block Diagram.*

The MIC4604 is offered in a small 2.5 mm x 2.5 mm UDFN package for applications that are space constrained and an SOIC-8 package for ease of manufacturing. The motor trend is to put the motor control circuit inside the motor casing, which requires small packaging because of the size of the motor.

The MIC4604 offers low UVLO threshold and programmable gate drive, which allows for longer operation time in battery operated motors such as power hand tools.

Cross conduction across the half bridge can cause catastrophic failure in a motor application. Engineers typically add dead time between states that switch between high input and low input to ensure that the low-side MOSFET completely turns off before the high-side MOSFET turns on and vice versa. The dead time depends on the MOSFET used in the application, but 200 ns is typical for most motor applications.

5.11 Power Inverter

Power inverters are used to supply AC loads from a DC operated battery system, mainly during power failure. The battery voltage can be 12 VDC, 24 VDC, or up to 36 VDC, depending on the power requirements. There two popular conversion methods, Type I and Type II, that convert the battery energy to AC line voltage (110 VAC or 230 VAC).

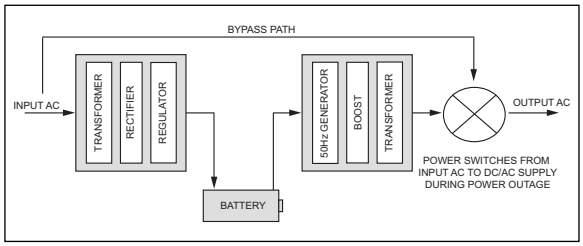


FIGURE 5-10: *Type I Inverter Topology.*

As shown in Figure 5-10, Type I is a dual-stage topology where line voltage is converted to DC through a transformer to charge the storage batteries. When a power failure is detected, the stored DC energy is converted to AC through another transformer to drive the AC loads connected to the inverter output. This method is simplest to design, but tends to be bulky and expensive because it uses two transformers.

Type II is a single-stage topology that uses only one transformer to charge the bank of batteries to store the energy. During a power outage, the same transformer is used to power the line voltage. The Type II switches at a higher frequency compared to the Type I topology to maintain a small transformer size.

Both types require a half bridge or full bridge topology to boost the DC to AC. This application can use two MIC4604s. The 85V operating voltage offers enough margin to address all of the available banks of batteries commonly used in inverter applications. The 85V operating voltage allows designers to increase the bank of batteries up to 72V, if desired. The MIC4604

can sink as much as 1A, which is enough current to overcome the MOSFET's input capacitance and switch the MOSFET up to 50 kHz. This makes the MIC4604 an ideal solution for inverter applications.

As with all half-bridge and full-bridge topologies, cross conduction is a concern to inverter manufactures because it can cause catastrophic failure. This can be remedied by adding the appropriate dead time between transitioning from the high-side MOSFET to the low-side MOSFET and vice versa.

5.12 Layout Guidelines

Use the following layout guidelines for optimum circuit performance:

- Place the V_{DD} and HB bypass capacitors close to the supply and ground pins. It is critical that the etch length between the high side decoupling capacitor (C_B) and the HB and HS pins be minimized to reduce lead inductance.
- Use a ground plane to minimize parasitic inductance and impedance of the return paths. The MIC4604 is capable of greater than 1A peak currents and any impedance between the MIC4604, the decoupling capacitors, and the external MOSFET will degrade the performance of the driver.
- Trace out the high d_i/d_t and d_v/d_t paths, as shown in Figure 5-11 and Figure 5-12, and minimize etch length and loop area for these connections. Minimizing these parameters decreases the parasitic inductance and the radiated EMI generated by fast rise and fall times.

A typical layout of a synchronous buck converter power stage (Figure 5-11) is shown in Figure 5-12.

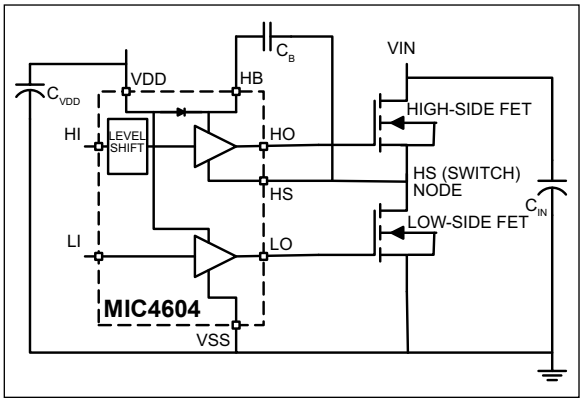


FIGURE 5-11: *Synchronous Buck Converter Power Stage.*

The high-side MOSFET drain connects to the input supply voltage (drain) and the source connects to the switching node. The low-side MOSFET drain connects to the switching node and its source is connected to ground. The buck converter output inductor (not shown) connects to the switching node. The high-side drive trace, HO, is routed on top of its return trace, HS, to minimize loop area and parasitic inductance. The low-side drive trace LO is routed over the ground plane to minimize the impedance of that current path. The decoupling capacitors, C_B and C_{VDD}, are placed to minimize etch length between the capacitors and their respective pins. This close placement is necessary to efficiently charge capacitor C_B when the HS node is low. All traces are 0.025 in. wide or greater to reduce impedance. C_{IN} is used to decouple the high current path through the MOSFETs.

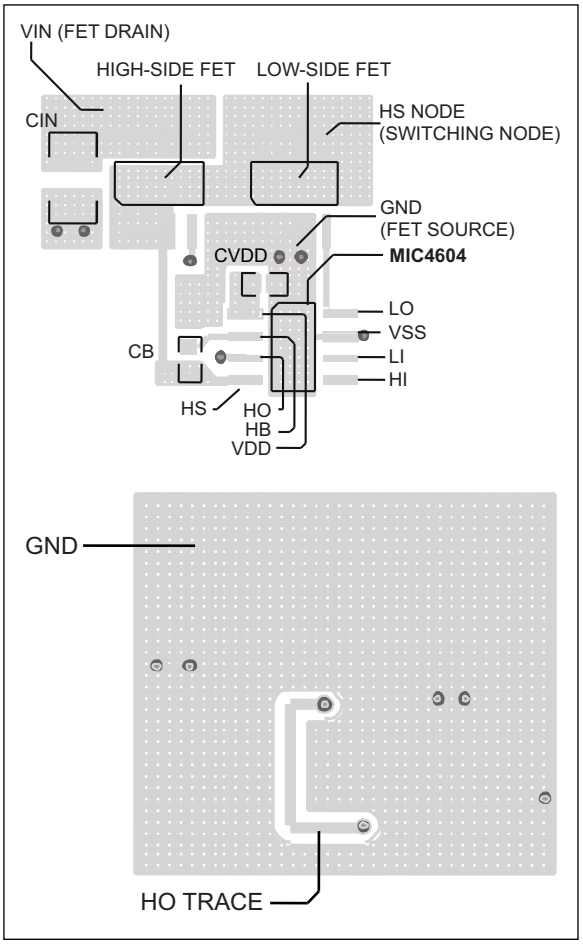
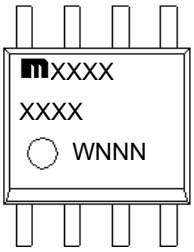


FIGURE 5-12: *Typical Layout of a Synchronous Buck Converter Power Stage.*

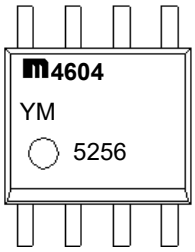
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

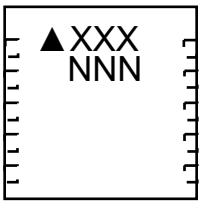
8-Pin SOIC



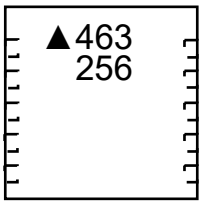
Example:



8-Pin UDFN



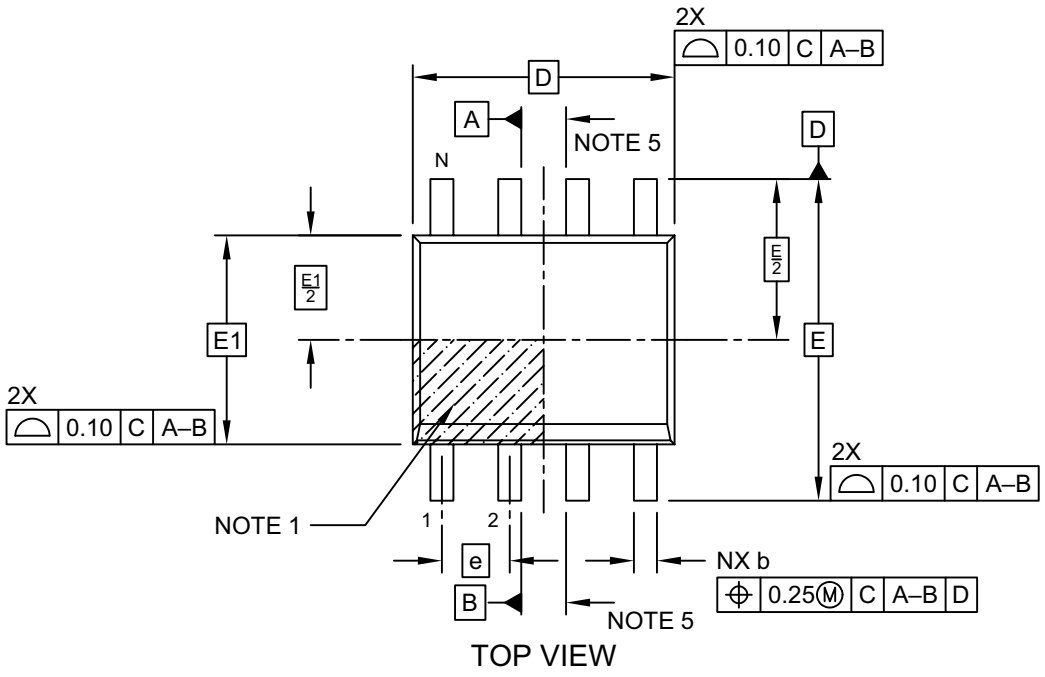
Example:

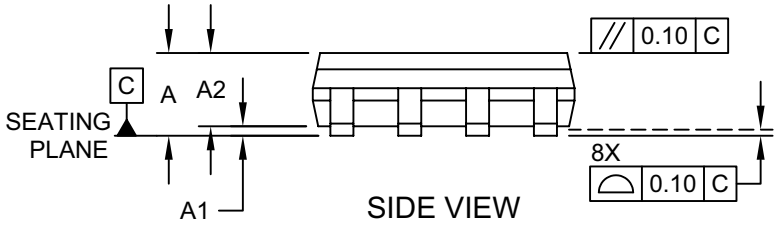


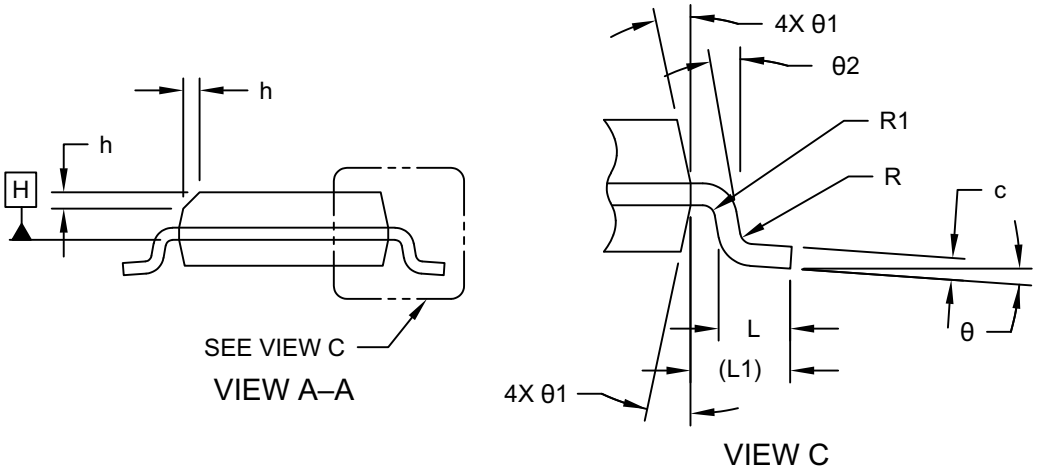
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (¯) symbol may not be to scale.

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



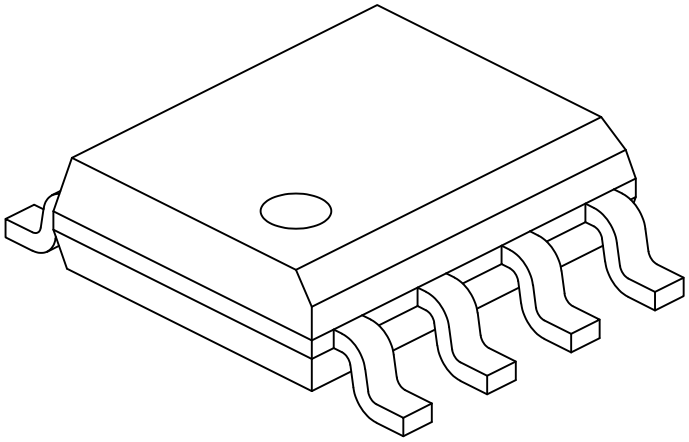




Microchip Technology Drawing No. C04-057-3BX Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

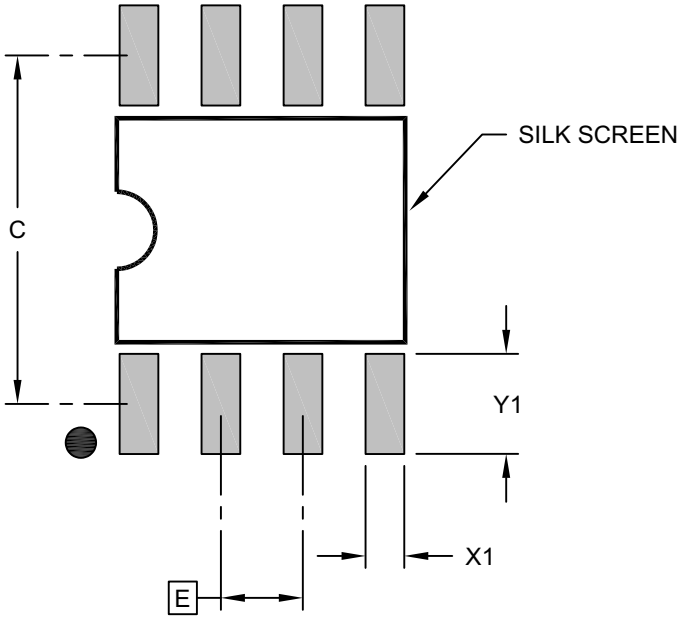
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-3BX Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

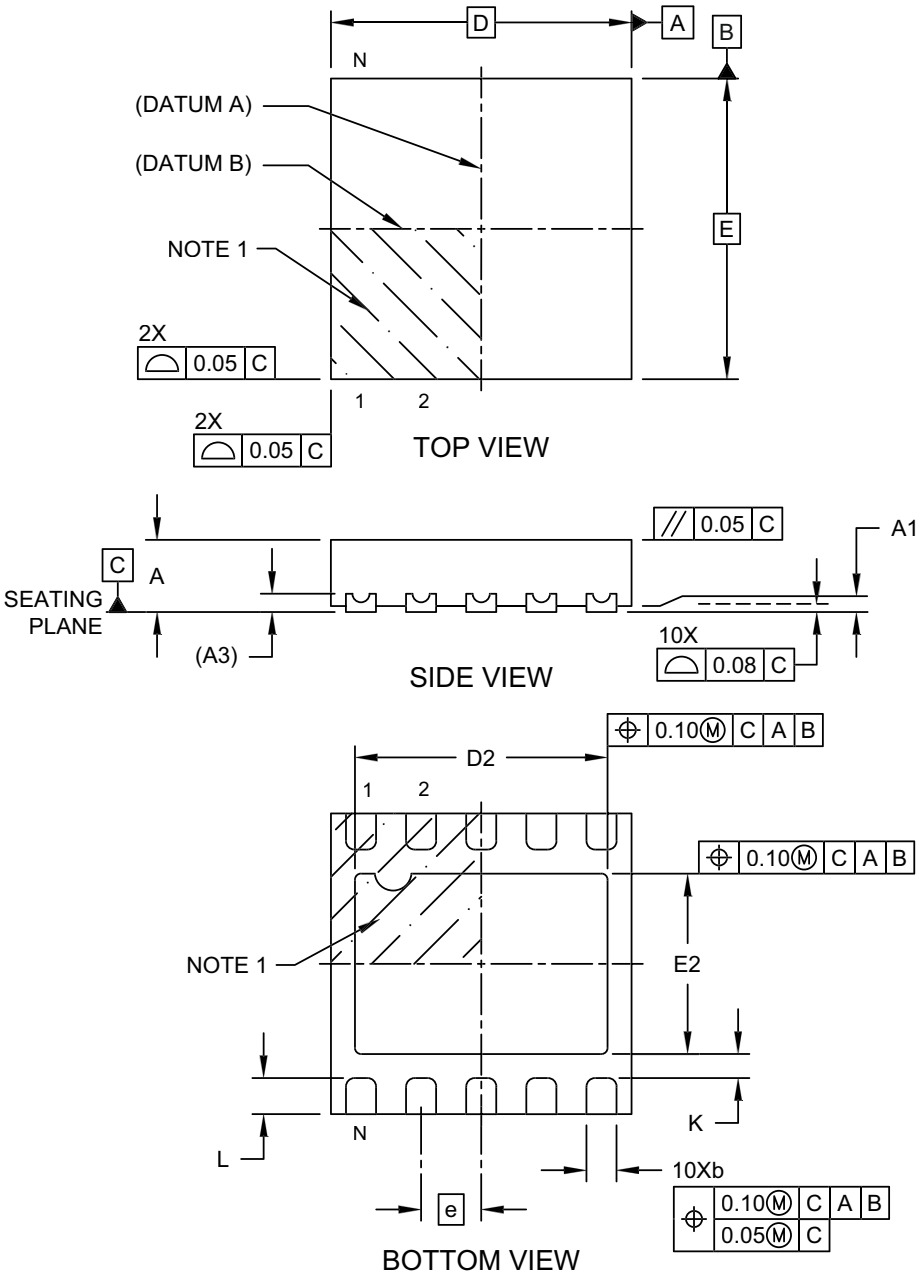
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-3BX Rev K

10-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HNA) - 2.5x2.5x0.6 mm Body [UDFN] With 2.10x1.50 mm Exposed Pad

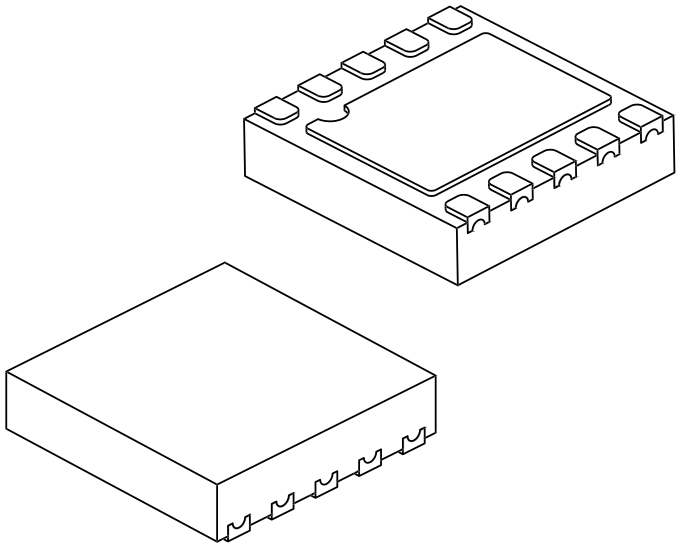
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-01161-HNA Rev B Sheet 1 of 2

10-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HNA) - 2.5x2.5x0.6 mm Body [UDFN] With 2.10x1.50 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.50 BSC	
Exposed Pad Length	D2	2.05	2.10	2.15
Overall Width	E		2.50 BSC	
Exposed Pad Width	E2	1.45	1.50	1.55
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.30	0.35
Terminal-to-Exposed-Pad	K	0.20	–	–

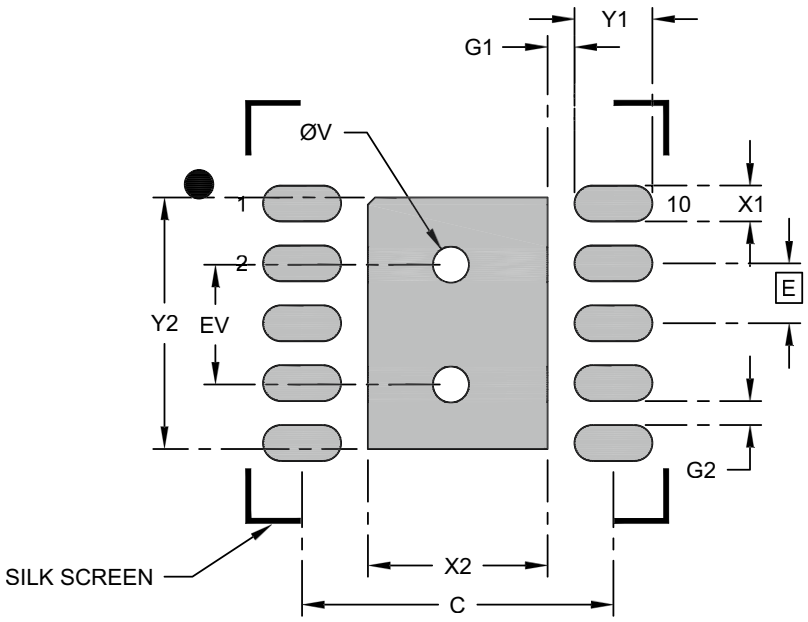
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerances, for information purposes only.

Microchip Technology Drawing C04-01161-HNA Rev B Sheet 2 of 2

10-Lead Ultra Thin Plastic Dual Flat, No Lead Package (HNA) - 2.5x2.5x0.6 mm Body [UDFN] With 2.10x1.50 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.50
Center Pad Length	Y2			2.10
Contact Pad Spacing	C1		2.60	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.65
Contact Pad to Center Pad (X10)	G1	0.23		
Contact Pad to Contact Pad (X8)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during the reflow process.

Microchip Technology Drawing C04-03161-HNA Rev B

NOTES:

APPENDIX A: REVISION HISTORY

Revision C (March 2025)

- Updated Figure 4-2, Figure 4-3, Figure 5-1, Figure 5-2, Figure 5-3, Figure 5-5, Figure 5-6 and Figure 5-11.
- Updated Package Marking Information
- Updated the package outline drawings for the 10-Lead UDFN (HNA).
- Changed TDFN to UDFN when referring to package type.

Revision B (December 2023)

- Added information about the Automotive Qualification status of the device in Section Features.
- Updated Package Drawings in Section 6.0 Packaging Information
- Updated Section Product Identification System, with Automotive Qualified devices.
- Added Note 3 in Table 1-1.

Revision A (January 2018)

- Converted Micrel document MIC4604 to Microchip data sheet DS20005852A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	XX	–XX	VAO
Device	Temperature	Package	Media Type	Qualification

Device:	MIC4604:	85V Half-Bridge MOSFET Driver with up to 16V Programmable Gate Drive
Temperature:	Y	= -40°C to +125°C
Package:	M MT	= 8-Lead SOIC = 10-Lead 2.5 mm x 2.5 mm UDFN
Media Type:	Blank TR	= 95/Tube = SOIC: 2,500/Reel; UDFN: 5000/Reel
Qualification*:	Blank VAO	= Standard Part = AEC-Q100 Automotive Qualified (SOIC only)

*Contact your local Microchip sales office to request automotive qualified variants for other package types.

Examples:

b) MIC4604YM-TR: 85V Half-Bridge MOSFET Driver with up to 16V Programmable Gate Drive, -40°C to +125°C, 8-Lead SOIC 2,500/Reel

d) MIC4604YMT-TR: 85V Half-Bridge MOSFET Driver with up to 16V Programmable Gate Drive, -40°C to +125°C, 10-Lead 2.5 mm x 2.5 mm UDFN, 5000/Reel

e) MIC4604YM-TRVAO: 85V Half-Bridge MOSFET Driver with up to 16V Programmable Gate Drive, -40°C to +125°C, 10-Lead 2.5 mm x 2.5 mm UDFN, 2,500/Reel, AEC-Q100 Automotive Qualified

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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