AN1994

SCH322x PCB Schematic Review Checklist

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INTRODUCTION

This application note is a schematic review checklist for SCH322x family devices that are comprised of sub-checklists. Use the checklists to verify that concepts, tasks, or options for SCH322x family devices have been considered or handled. This checklist is not meant to be a substitute for a proper study of available data sheet, design guides or reference schematics. For a list of these documents, see References.

This document includes the following sub-checklists:

Audience

This document is written for a reader that is familiar with hardware design. The goal of this application note is to provide checklists for available schematics to ensure the key signals are handled appropriately.

References

The following documents should be referenced when using this application note:

- SCH322x Family Devices Data Sheet
- SCH322x Evaluation Board Reference Schematic
- PCI Local Bus Specification (see www.pcisig.com)
- Intel Low Pin Count (LPC) Interface Specification, Revision 1.1, August 2002

Package Information

The SCH322x devices are available in the following packages:

- SCH3227 144-pin WFBGA RoHS compliant package
- SCH3226 100-pin WFBGA RoHS compliant package
- SCH3224 100-pin WFBGA RoHS compliant package
- SCH3223 64-pin WFBGA RoHS compliant package
- SCH3222 84-pin WFBGA RoHS compliant package

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SCH322X CHECKLIST

The characteristics of the I/O buffer implemented in the SCH322x are defined in their respective data sheet. Care should be taken to ensure that external devices maintain acceptable voltage levels on all inputs and open drain outputs. It is not advisable to allow input buffers to float or remain in an indeterminate state.

General Rules

TABLE 1: GENERAL RULES CHECKLIST

General Rules	Check
VTR powered inputs should not be floating when VCC is off, or this can result in extra current drain.	
Do not cross power domains when attaching pull-ups to pins. • Pins that are located on the VCC power well must be pulled either to ground or to VCC. • GPIO pins with wakeup capability that are located on the VCC power well may be pulled to VCC, VTR, or ground, depending on the design. • Pins that are located on the VTR power well must be pulled either to ground or to VTR.	
Input buffers must be at a logic high or a logic low state when power is applied to the buffer. If the external device controlling the input pin tri-states while power is applied to the buffer, an external pull-up/pull-down resistor should be added to prevent the pin from floating.	
All output pins that are implemented as open drain outputs must be pulled-up with an external resistor to the proper VCC or VTR power well.	
Most GPIOs default as Input on the VTR POR. Following a power failure (loss of VTR power), these pins will be GPIO inputs. It is suggested that these pins be pulled to their inactive state depending on the function being used.	
Bi-directional buffers require either pull-ups or pull-downs to prevent the input buffer from floating when the bus is tri-stated.	

Power, Ground, and Clock

TABLE 2: POWER, GROUND, AND CLOCK CHECKLIST

Power, Ground and Clock	Check
One decoupling capacitor (0.1uF) should be placed as close as possible to each of the power pins (VCC, VTR, VBAT, HVTR) of the SCH322x.	
HVTR must be powered by VTR.	
Place the connection between the AVSS/HVSS and VSS ground planes in a noise free area of the board, or use a single GND plane.	
CLOCKI must be connected to an external 14.318Mhz clock input. If using an external clock source, it requires 50% duty cycle +/- 10%, +/- 100ppm, and jitter < 100ps RMS.	
CLKI32 is a 32.768KHz clock single-ended input from the system core logic (ex: SUSCLK) whenever RSMRST# is de-asserted. If this clock is not used, the pin should be grounded.	

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Strap Options

TABLE 3: STRAP OPTIONS CHECKLIST

Strap Options	Check
For SCH3227 & SCH3226, a STRAPOPT pin has a strap option to select between UART or Glue Logic functions on corresponding 8 pins (please see data sheet for more information). • A “0” sets the corresponding 8 pins to Glue Logic Functions, and Device ID to 0x7D. • A “1” sets the corresponding 8 pins to UART Functions, and Device ID to 0x7F.	
RTS2# pin has a strap option for reset generator pulse width selection. • A “0” sets the RESGEN delay for 500 msec. • A “1” sets the RESGEN delay for 200 msec.	
RTS1# pin has a strap option for SYSOPT0 (Configuration Port Base Address Control), and DTR1# pin has a strap option for SYSOPT1. Footprints for a pull-up and pull-down resistor should be placed near the RTS1# and DTR1# pins to strap the SYSOPT function. • SYSOPT1 / SYSOPT0 = 1 / 0 set the configuration base address to 002Eh. • SYSOPT1 / SYSOPT0 = 1 / 1 set the configuration base address to 004Eh. • SYSOPT1 / SYSOPT0 = 0 / 0 set the configuration base address to 162Eh. • SYSOPT1 / SYSOPT0 = 0 / 1 set the configuration base address to 164Eh.	
When choosing the values for pull-ups/pull-downs on the strap option pins (RTS2#, RTS1#, DTR1#), the internal pull-ups/pull-downs in the attached RS-232 transceiver need to be taken into account so that a valid logic level is seen when the straps are sampled.	

Host Interface

TABLE 4: HOST INTERFACE CHECKLIST

Host Interface	Check
LAD[3:0] are bi-directional signals. They can be floated and needs to be maintained high by weak pull-up resistors (100k ohm) during the turnaround (TAR) periods of a cycle.	
LDRQ# needs a weak pull-up resistor (100k ohm) or direct connect to VCC on each unconnected LDRQ# signal at the chipset to make sure it does not accidentally go low when floating.	
LFRAME# needs a connection from the host. Add a 10k ohm pull-up to VCC to avoid floating when host is tri-stated.	
PCI_RESET# is required from the system PCI reset circuit. Add a 10k ohm pull-up to VCC to avoid floating when host is tri-stated.	
PCI_CLK is required to connect from the 33MHz, same as the PCI clock on the host.	
Serial IRQ needs to connect to the host. Add a 10k ohm pull-up to VCC to avoid floating.	
IO_PME# can be used as a power management event output to wake-up from S3 and below. This signal should be pulled-up to VTR through a 10k ohm resistor.	
IO_SMI# can be used as system management interrupt to the host. The function must set the pin as output open-drain, and use a 10k ohm pull-up resistor to VCC.	

Hardware Monitoring

TABLE 5: HARDWARE MONITORING CHECKLIST

Hardware Monitoring	Check
HWM_INT# interrupt output is an open-drain signal. Add a 10k ohm pull-up to VTR is required.	
THERMTRIP# output is an open-drain signal. Add a 10k ohm pull-up to VTR is required.	
Voltage Monitoring Inputs (+5V_IN, +2.5V_IN, VCCP_IN, +12V_IN) are on the HVTR power supply, which are back-drive protected.	
The remote diode + and - tracks should be kept close together, in parallel with grounded guard tracks on each side. A 10 mil track minimum width and spacing is recommended.	
Place a cap between the two leads, as close as possible to the SCH322x chip. 330pF (beta enabled) is used for the processor diode. 2200pF (beta disabled) is used for the 3904 diode.	
The remote diode + and - tracks should be kept to a maximum length of eight inches. If a longer length is needed, use a twisted wire pair or coaxial cable.	
Both remote temperature sensor channel inputs should be terminated with a thermal diode, a transistor or a resistor, even they are not used in the design. Transistors that are suitable for use are MMBT3904 or equivalents. Termination resistor values for use can be from 510 ohm to 1K ohm.	

Glue Logic

TABLE 6: GLUE LOGIC CHECKLIST

Glue Logic Interface	Check
PB_IN# input signal is used to detect a power button event. Add a 10k ohm pull-up to VTR is required.	
SLP_Sx# input signal is used to detect the System Sx Sleep State. Add a 10k ohm pull-up to VTR is required.	
PB_OUT# is a pull-push output signal that is used as power button output to the chipset.	
PS_ON# output signal is the inverse of the SLP_Sx# input signal. This signal goes directly to the Power Supply to turn the supply on or off.	
IDE_RSTDRV# is an open drain buffered copy of PCI_RESET# (see TABLE 4:) signal. Add a 1K ohm pull-up to VCC or 5V is required.	
PICRESET1#, PICRESET2#, and PICRESET3# outputs are 3.3V balance buffer push-pull buffered copies of PIC_RESET# input.	
PWRGD_PS is a power good input from power supply. This signal has hysteresis and are internally pulled to VTR through a 30uA resistor.	
PWRGD_OUT is a power good output open drain signal. Add a 10k ohm pull-up to VTR is required.	
RSMRST# is a resume reset output open drain signal for the chipset resume well. This signal is used as a power on reset signal for the chipset. Add a 10k ohm pull-up to VTR is required.	

Keyboard/Mouse

TABLE 7: KEYBOARD/MOUSE INTERFACE CHECKLIST

Keyboard/Mouse Interface	Check
All PS/2 clock and data pins (KDAT, KCLK, MDAT, MCLK) must be pulled-up to the PS/2 power supply pin on the connector (to support wake-up functionality) through a 10k ohm resistor, even if the PS/2 channels are not used. The PS/2 power supply may or may not be VTR; it should be a 5v_Stdby if the keyboard is set to wake the system, or 5V or not.	
KBDRST# (keyboard reset) is an open drain output, a pull-up to VCC through a 10k ohm resistor is required.	
A20M (Gate A20) is an open drain output, a pull-up to VCC through a 10k ohm resistor is required.	

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Miscellaneous

TABLE 8: MISCELLANEOUS CHECKLIST

Miscellaneous	Check
For unused serial ports, all the input pins (RXD, DSR#, CTS#, RI#, DCD#) should be pulled-up to VCC through a 10k ohm resistor.	
For unused parallel port, all the input and bi-directional pins (PD[7:0], SLCT, PE, BUSY, ACK#, ERROR#) should be pulled-up to VCC through a 10k ohm resistor.	
For PWM and FAN TACH implementation, please refer to SCH322x EVB reference schematic regarding typical 4-wire fan reference circuitries.	
LED functionality is implemented on 2 GPIOs: GP60, and GP61. These LEDs can be configured as either open drain or push-pull. In the case of open-drain, the pin is capable of sinking current and a pull-up to VTR is required, the pull-up value is depended on the external LED recommended. In the case of push-pull, the part will source current.	
WDT is a watch dog output signal that must be configured as an open-drain output, a pull-up to VTR through a 10k ohm resistor is required.	
FPRST# is a front panel reset input signal. This signal has hysteresis and are internally pulled to VTR through a 30uA resistor, also is debounced internally.	
CLKO is a programmable clock output signal. This signal will output a programmable frequency between 0.5Hz to 16Hz. This pin can be configured as push-pull (default) or open-drain. If configure as open-drain, a pull-up to VTR through a 10k ohm resistor is required.	

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001994A (09-02-15)	Document Release	

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