3.3V/5V 155Mbps PECL LOW-POWER LIMITING POST AMPLIFIER W/PECL SIGNAL DETECT

SY88813V EVALUATION BOARD

FUNCTIONAL FEATURES

The SY88813V features:

- **Single 3.3V or 5V power supply**
- **Up to 155Mbps operation**
- **Low noise PECL data outputs**
- **Chatter-free PECL Signal Detect (SD) output**
- **TTL /EN input**
- **Programmable SD level set (SD_{LVL})**
- **Available in a tiny 10-pin MSOP (3mm × 3mm) package**

The SY88813V evaluation board features:

- **AC-coupled I/O with SMA connectors**
- **Single potentiometer to set SD_{LVL}**
- **50Ω input network termination**

AVAILABLE MEASUREMENTS

The SY88813V evaluation board allows the following measurements:

- **Frequency performance**
- **Output eye pattern generation**
- **Mask testing**
- **Jitter**
- **Output rise/fall time**
- **BER testing**
- **Hysteresis measurement**

EVALUATION BOARD

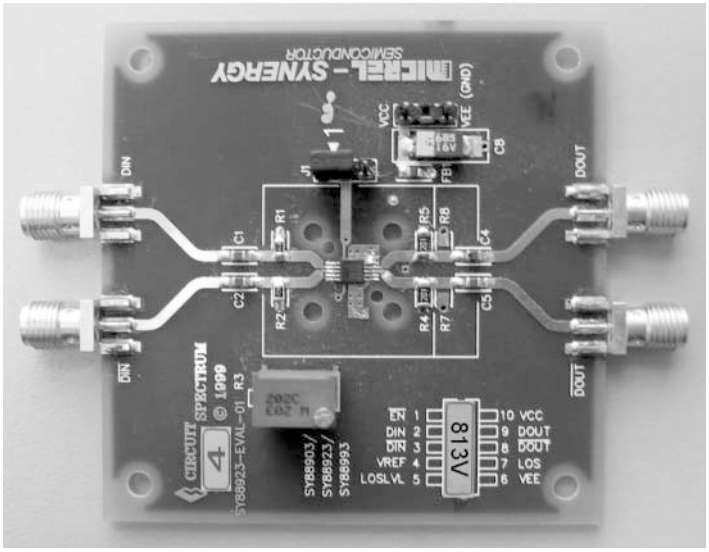

Figure 1. SY88813V Evaluation Board

DESCRIPTION

The SY88813V low-power limiting post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88813V quantizes these signals and outputs PECL level waveforms.

The SY88813V operates from a single +3.3V ±10% or +5V ±10% power supply, over temperatures ranging from –40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 155Mbps and as small as $5mV_{pp}$ can be amplified to drive devices with PECL inputs.

The SY88813V generates a PECL signal-detect output. A programmable signal-detect level set pin (SD_{LVL}) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and deasserts low otherwise. /EN deasserts the true output signal without removing the input signal. Typically 4.6dB SD hysteresis is provided to prevent chattering.

This manual provides information on the SY88813V evaluation board. It should be used in conjunction with the SY88813V datasheet, which contains full specifications of the SY88813V.

The SY88813V evaluation board enables fast and thorough evaluation of the SY88813V 155Mbps PECL low-power limiting post amplifier. The board is an easy-to-use, single-layer high-speed microstrip design. It is designed to be driven by a high-speed 155Mbps pattern generator and provides on-board 50Ω terminations for the generator's outputs. The input termination network also provides the required input bias of V_{CC}–1.3V for the SY88813V.

The SY88813V evaluation board is intended to be terminated to a 50Ω scope and provides for simple user adjustability of the SD threshold through the adjustment of an on-board potentiometer. This allows the user to evaluate various parameters of the SY88813V, as listed in the "Available Measurements" section of this document.

All data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

MEASUREMENT SETUP

Equipment used for measurements:

1. Agilent 83752A Synthesized Sweeper
2. Agilent 70004A Display
3. Agilent 70843B Error Performance Analyzer
4. Agilent 86100A Wide-Bandwidth Oscilloscope
5. Two (2) MCL BW S15W2 40dB attenuators
6. Agilent E3620A DC Power Supply
7. Tektronix DMM157 Multimeter
8. Matched High-Speed Cables w/SMA Connectors

Note:

Items 1 through 3 constitute the BERT stack.

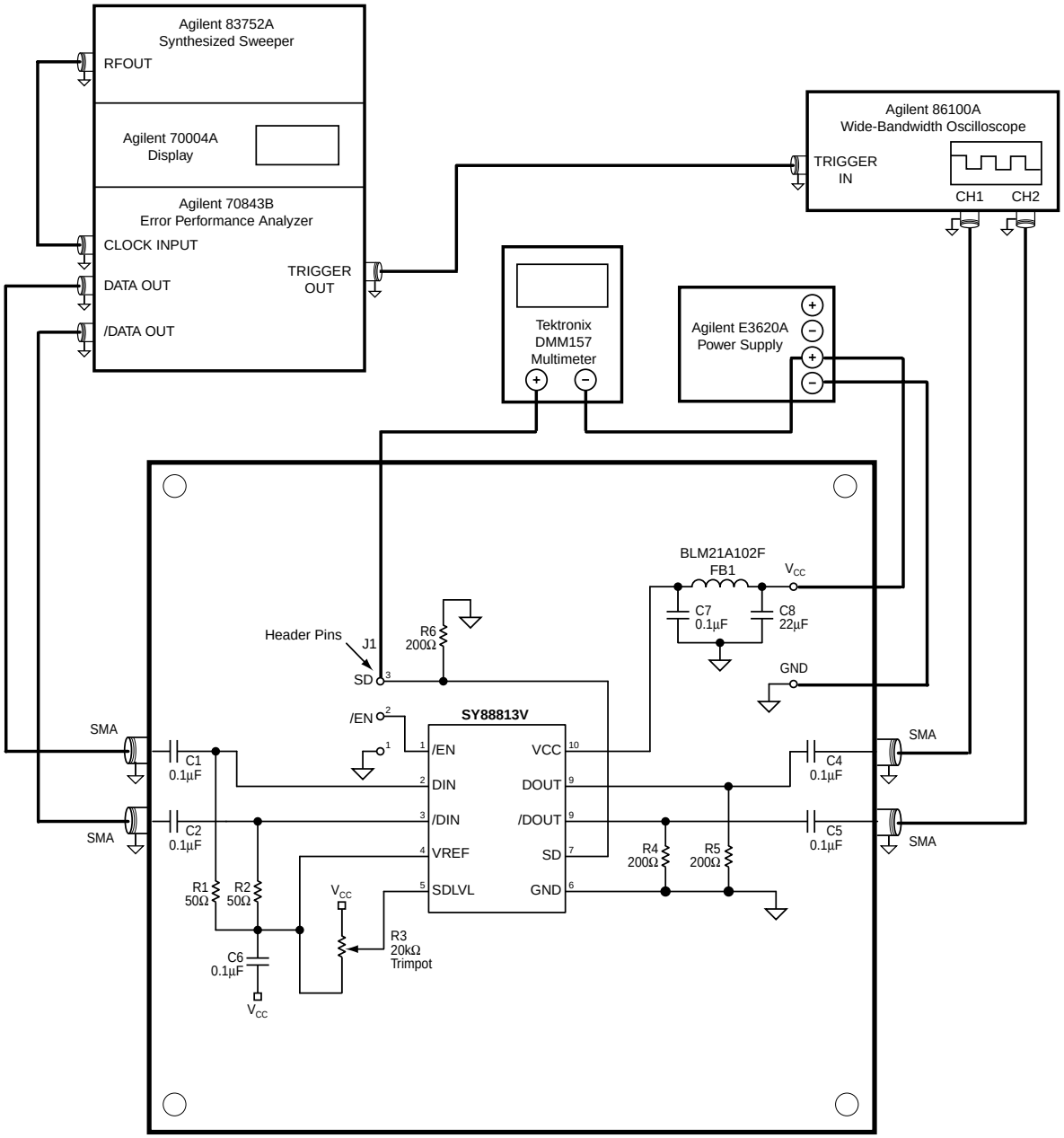

Figure 2. Setup for Measurements

SETUP FOR MEASUREMENTS

This section explains how to connect and setup the SY88813V evaluation board per Figure 2. Ensure proper ESD precautionary measures are taken before handling sensitive electronic equipment, including the SY88813V evaluation board.

1. Set E3620A to output 3.3V and then turn off E3620A. Connect E3620A's positive lead to V_{CC} post, negative lead to GND post.
2. Configure Agilent BERT stack:
   a) Set the 83752A Synthesized Sweeper to 155MHz.
   b) From the 70004A's Pattern menu, choose the PRBS 2^{31}–1 pattern.
   c) From the 70004A's Trigger menu:
      i. Choose clock as trigger output
      ii. Choose CLK/8 for divider
   d) From the 70004A's Data menu:
      i. External termination = DC termination 0V
      ii. Attenuation = 40dB
      iii. Amplitude = 5mV ($10mV_{pp}$)
      iv. Hi-Level = 0V
      v. Tracking = ON
      vi. Polarity = NORMAL
      vii. Data Output = ON
      viii. Crossing = 0
3. Connect 70843V's trigger output to 86100A's trigger input.
4. Use J1 to short /EN to GND on SY88803V evaluation board.
5. Connect DIN and /DIN on SY88813V evaluation board to 70843V's data outputs through 40dB attenuators.
   a) Connect 40dB attenuators directly to the board rather than the 70843V's data outputs to allow a larger and cleaner signal to pass through the connecting SMA cables.
6. Connect DOUT and /DOUT on SY88813V evaluation board to 86100A's inputs.
7. Set DMM157 to display voltage. Connect positive lead to SD header on J1 and connect negative lead to V_{CC}.
8. Turn on E3620A. Typical power supply current should be ~45mA, including the SY88813V's current and current through the on-board 200Ω output pulldown resistors at 3.3V supply voltage. Excessive current usually means the power supply leads have been connected backwards. Be careful of this!
9. Configure 86100A oscilloscope.
   a) Verify a trigger signal is present by checking that the Trigger Source button is lit.
      i. Depress this button to choose external source if necessary.
      ii. Adjust trigger level if necessary.
   b) Press Eye/Mask Mode on front panel.
   c) Choose NRZ Eye Measurements from on-screen display.
   d) Choose RMS Jitter, Rise Time, Fall Time and Eye Amplitude measurements from on-screen selection list.

MEASUREMENTS

The SY88813V evaluation board assumes the use of a 50Ω scope to terminate the SY88813V. The following sections detail various measurements that the SY88813V evaluation board allows.

1. Eye pattern generation including jitter and rise/fall times:
   a) Set 70004's Data amplitude to 5mV ($10mV_{pp}$).
   b) Press Autoscale on oscilloscope. The eye pattern should automatically display on the scope. If not, verify the steps listed in the "Setup for Measurements" section are completed. Sometimes the waveform needs to be manually adjusted to fit the display. Use the Time Scale and Voltage Scale knobs on the front panel of the scope to adjust this.
   c) Observe measurements on scope's display. The rise and fall times should be less than 1000ps, amplitude around 800mV ($1600mV_{pp}$) and jitter around $10ps_{rms}$.
      i. Note that the output amplitude varies with the input amplitude until the SY88813V enters limiting mode at around $20mV_{pp}$ input. The SY88813V has a typical gain of 38dB. Hence, $10mV_{pp}$ input will give only $800mV_{pp}$ output, whereas $40mV_{pp}$ input will give $1600mV_{pp}$ output.
   d) Set 70004's Data amplitude to 20mV ($40mV_{pp}$) and repeat above.

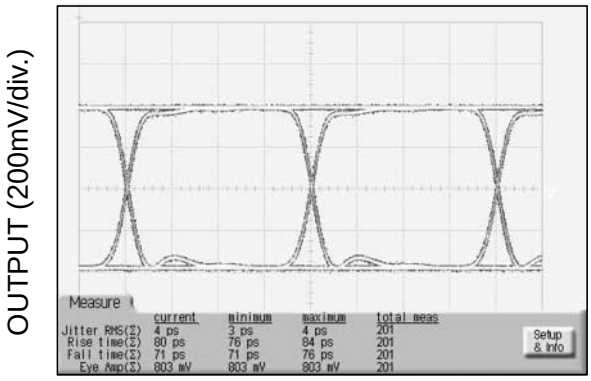

Figure 3. Typical SY88813V Eye Diagram

2. Mask testing:
   a) Press Eye/Mask Mode on front panel of scope.
   b) Choose Mask Testing from on-screen display.
   c) Choose Open Mask from on-screen selection list.
      i. Select and open the OC-3 mask
   d) Choose Start Mask Testing from on-screen selection list. Waveform should automatically display with appropriate mask regions and testing will start. If not, verify the steps listed in the "Setup for Measurements" section are completed.
3. BER testing:
   a) Feedback the SY88813V evaluation board's DOUT output to the 70843V's BERT Data input.
   b) Feedback the 70843V's Clock output to the 70843V's BERT Clock input.
   c) Set 70004's Data amplitude to 20mV ($40mV_{pp}$).
   d) From the 70004A's Gating menu:
      i. Choose a gate condition. The options are: gate by time, errors or bits. Choose bits, but this is of no relevance because there should be no errors, and the test will run forever until manually interrupted if gate by errors is chosen.
      ii. Choose single gating period.
      iii. Choose run gating.
      iv. 70004A will reset error count and synchronize SY88813V's transmitted bitstream to 70843V's generated bitstream. If synchronization does not occur, it is sometimes due to cable length. Try using different length cables to achieve synchronization. If this is unavailable, another trick is to adjust the 83752A's frequency to a slightly higher or lower value.
      v. At end of gating period, there should be no errors.

4) SD hysteresis:
   a) The SY88813V evaluation board provides a potentiometer to allow for easy adjustment of SD_{LVL} without the need for an extra power supply. SD_{LVL} taps off the potentiometer whose ends are connected from V_{CC} to V_{REF}. V_{REF} is a reference voltage of approximately V_{CC}–1.3V. Hence, SD_{LVL} can be set to any voltage from V_{CC} to V_{CC}–1.2V, as specified in the SY88813V datasheet. The potentiometer creates a voltage divider. Thus,

      $$SD_{LVL} = V_{CC}(V) - 1.3V \times R(k\Omega)/ 20k\Omega,$$

      where R is the measured resistance of the potentiometer from V_{CC} to the tap at SDlvl. The proceeding steps show how to find the SD hysteresis for a $10mV_{pp}$ SD deassert voltage without measuring R.
   b) Set 70004's Data amplitude to 5mV ($10mV_{pp}$).
   c) Verify DMM157 displays that SD is HIGH (~-0.9V). If not, turn R3 until SD is HIGH.
   d) Turn R3 just until SD is LOW (~-1.7V).
   e) Slowly increase 70004A's Data amplitude until SD becomes HIGH. Note the voltage at which SD becomes HIGH. This is the SD assert voltage.
   f) Now slowly lower the 70004A's Data amplitude until SD becomes LOW again. This should be the starting voltage of 5mV ($10mV_{pp}$). This is the SD deassert voltage.
   g) Hysteresis(dB) = 20log(SD assert voltage/SD deassert voltage). This should be ≥ 2dB.

FREQUENTLY ASKED QUESTIONS

I just got my SY88813V evaluation board and I cannot get anything to work! Where should I start?

First, check the power supplies. Typical power supply current should be ~45mA, including the SY88813V's current and current through the on-board 200Ω output pulldown resistors at 3.3V supply voltage. Excessive current usually means the power supply leads have been connected backwards. Be careful of this!

Next, ensure the SY88813V is enabled by shorting /EN to GND via J1. If this looks okay, then verify the 70004A's Data outputs are enabled and there's sufficient amplitude (at least $5mV_{pp}$) to drive the SY88813V.

If the above are okay and there's still nothing displaying on the scope, then there's most likely a trigger setup issue with the scope. Look on the scope's front panel and verify that the instrument is triggered. The Trigger Source button should be lit if a trigger signal is present. If not, press the button until the external trigger is selected. Also, try adjusting the level until a signal is found. If this does not work, verify the 70004A is set to output a CLK/8 trigger signal as described in the "Setup for Measurements" section of this document.

Can you suggest a bypass/decoupling scheme?

Figure 2 shows the power supply decoupling scheme used for the SY88813V evaluation board. The "Bill of Materials" at the end of this document lists the supplier and component values. We have found this arrangement to be an excellent starting point.

What layout tips do you have?

1. Establish controlled impedance stripline, microstrip or coplanar construction techniques for high-speed signal paths.

2. All differential paths are critical timing paths and skew should be matched to within ±10ps.

3. Signal trace impedance should not vary more thn ±5%. If in doubt, perform Time Domain Reflectometry (TDR) analysis of signal traces.

4. Place power supply decoupling capacitors as close as possible to the device's power pins.

What is Time Domain Reflectometry (TDR)?

TDR is used to verify impedance continuity along a signal path. Many interconnects, such as SMA, if not launched correctly onto the PCB, will exhibit inductive-like resonance with an abrupt capacitive discontinuity. This discontinuity will subtract signal from the inputs and outputs, effectively closing the resulting data eye. The 86100A allows TDR testing and is a useful tool to help evaluate your PCB.

I still have questions. Who should I contact?

Micrel's HBW Applications helpline is available to assist you. Please call (408) 955-1690 or e-mail hbwhelp@micrel.com for assistance.

BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty
C1, C2, C3, C4, C5, C6, C7	PCC1762CT-ND	Panasonic(1)	0.1µF surface mount capacitor, size 0603	6
C8	P11317CT-ND	Panasonic(1)	22µF surface mount capacitor, size C	1
FB1	BLM21A102F	Murata(2)	ferrite bead, size 0603	1
J1, V_{CC}	TSW–103–07–S–S	Samtec(3)	0.1mil center through hole terminal strip	2
R1, R2	P49.9LCT-ND	Panasonic(1)	49.9Ω surface mount resistor, size 0603	2
R3	3269W-1-203G	Bourns(4)	20kΩ trimmer	1
R4, R5, R6	P200GCT-ND	Panasonic(1)	200Ω surface mount resistor, size 0603	3
S1, S2, S3, S4	142-0701-851	Johnson(5)	end launch SMA	4
U1	SY88813V	**Micrel, Inc.**(6)	155Mbps PECL post amplifier	1

Notes:

1. Panasonic tel: 800-344-2112
2. Murata tel: 770-436-1300
3. Samtec tel: 800-726-8329
4. Bourns tel: 877-426-8767
5. Johnson tel: 800-247-8256
6. Micrel, Inc. tel: 408-944-0800

MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com