Atmel MCU Wireless

AT02601: Migration from AT86RF230 to AT86RF233

APPLICATION NOTE

Description

This application note is a guide to assist users of Atmel® AT86RF230 GHz transceiver in converting designs to Atmel AT86RF233. For complete transceiver details, always refer to the most recent version of the AT86RF233 datasheet.

Errata differences between AT86RF230 and AT86RF233 are not listed in this document, refer individual datasheet for more details.

AT86RF233 transceiver support is available in Atmel Software Framework version 3.7.3 or later.

In addition to the migration details, this document also highlights the enhanced features of AT86RF233 transceiver.

Features

- Hardware consideration while migrating to Atmel AT86RF233
- Firmware consideration while migrating to AT86RF233
- Enhanced features of AT86RF233
  - Security module (AES)
  - Random number generator
  - High Data Rate modes
  - Antenna diversity
  - RX/TX indicator
  - RX and TX frame time stamping
  - Frame buffer empty indicator
  - Dynamic frame buffer protection
  - Alternate Start-Of-Delimiter
  - Reduced power consumption mode
  - Time-Of-Flight module
  - Phase difference measurement

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1. Migration from Atmel AT86RF230 to AT86RF233

This chapter summarizes the modifications that might be required while migrating from AT86RF230 to AT86RF233 transceiver.

1.1. Hardware Considerations

This chapter summarizes the hardware modifications that might be considered while migrating from AT86RF230 to AT86RF233 transceiver.

1.1.1. TST Pin Changed to DVSS

The AT86RF230 and AT86RF233 vary in pin functionality for pin 7 as mentioned in table Pin Functional Deviation. In AT86RF230, pin 7 acts as TST pin which controls Continuous Transmission Test Mode, whereas in AT86RF233 pin 7 is changed to DVSS.

Design change is required only if AT86RF230 based design connects TST pin to a GPIO. During migration pin 7 of AT86RF233 requires a pull down resistor to avoid floating conditions. Best case would be to ground Pin 7 of AT86RF233 directly to DVSS. For more details, refer to section Pin Descriptions in individual datasheets.

1.1.2. XTAL Circuit

AT86RF230 and AT86RF233 vary in pin functionality for pins 25 and 26 as mentioned in below table. If external reference clock used, then it requires a design change as XTAL1 and XTAL2 pins are swapped in AT86RF233 compared to AT86RF230.

If external 16MHz crystal is used then there shall not be any design change required.

For more details, refer to section External Reference Frequency Setup in individual datasheets.

Table 1-1. Pin Functional Deviation

Pin No	AT86RF230	AT86RF233
Pin 7	TST	DVSS
Pin 25	XTAL1	XTAL2
Pin 26	XTAL2	XTAL1

1.1.3. Balun Selection

As per the datasheets of AT86RF230 and AT86RF233, we have a change in the recommended Johanson Technology Balun part Number as captured in below table.

This Balun part number change is not mandatory during migration from AT86RF230 to AT86RF233. But if 2450BM15A0015 Balun/Filter is used then the BOM cost is reduced as DC capacitor is not required on pin 2.

Table 1-2. Balun Part Number

SMD balun / filter	AT86RF230	AT86RF233
Part number	2450FB15L0001	2450BM15A0015

1.1.4. Bypass Capacitor

Below table captures the recommended bypass capacitor (CB1/CB3) value changes for AT86RF230 and AT86RF233 transceivers. The capacitor value depends on the custom board design. So, change may not

be required during migration. For more details, refer to section Basic Application Schematic in individual datasheets.

Note:
It is recommended to use capacitor values as given in Table 1-3 for Atmel AT86RF233 for faster state transition timings (Section Faster State Transition Timing)

Table 1-3. Bypass Capacitor CB1/CB3

Capacitor	AT86RF230	AT86RF233
CB1	1µF	100nF
CB3		

1.1.5. PAD_IO and PAD_IO_CLKM

Atmel AT86RF230 controls the drive current of digital output pads and CLKM through register configuration (PAD_IO and PAD_IO_CLKM respectively).

But Atmel AT86RF233 does not support configuration of drive current for digital output pads (MISO and IRQ) and CLKM pin.

For more details, refer to Section Drive Strength of Digital Pins.

1.2. Software Considerations

This chapter summarizes the software modifications that might be required while migrating from AT86RF230 to AT86RF233 transceiver.

1.2.1. Basic Operating Modes

AT86RF230 and AT86RF233 vary in few transceiver states while operating in basic operating mode. Below table captures the states configurable through register TRX_STATE [4:0] (TRX_CMD)

- Figure Basic Operating Mode State Machine for AT86RF230 depicts the transceiver state which is removed in AT86RF233
- Figure Basic Operating Mode State Machine for AT86RF233 depicts newly added transceiver states in AT86RF233

Table 1-4. Available State through Register Configuration (TRX_CMD)

TRX_CMD	AT86RF230	AT86RF233
0x00	NOP	NOP
0x02	TX_START	TX_START
0x03	FORCE_TRX_OFF	FORCE_TRX_OFF
0x04	-	FORCE_PLL_ON
0x06	RX_ON	RX_ON
0x08	TRX_OFF	TRX_OFF
0x09	PLL_ON	PLL_ON
0x10	-	PREP_DEEP_SLEEP

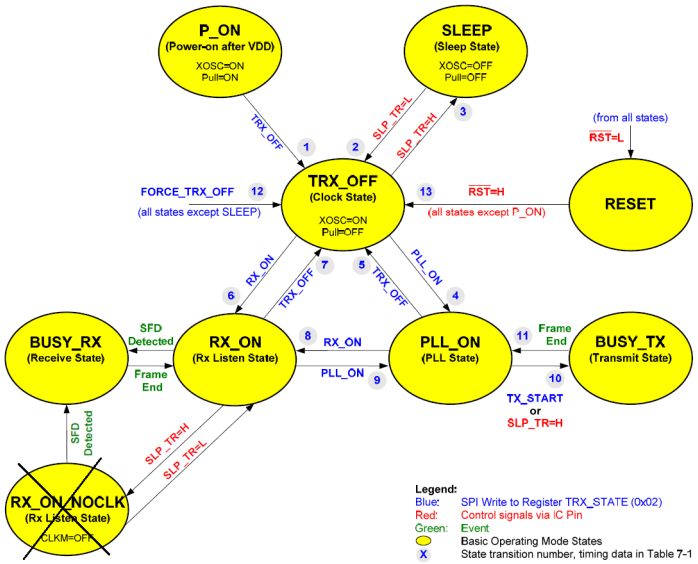
TRX_CMD	AT86RF230	AT86RF233
0x16	RX_AACK_ON	RX_AACK_ON
0x19	TX_ARET_ON	TX_ARET_ON

1.2.1.1. Migrating RX_ON_NOCLK to RX_ON State

In basic operation mode, RX_ON_NOCLK state shown in the figure Basic Operating Mode State Machine for AT86RF230 is not supported by the Atmel AT86RF233. RX_ON_NOCLK state should be migrated to RX_ON state in AT86RF233. For more details, refer to section Basic Operating Mode in individual datasheets.

If application requires switching off CLKM in RX_ON state, then it has to be done manually to disable CLKM using register TRX_CTRL [2:0].

Figure 1-1. Basic Operating Mode State Machine for AT86RF230



1.2.1.2. Migrating SLEEP to DEEP_SLEEP State

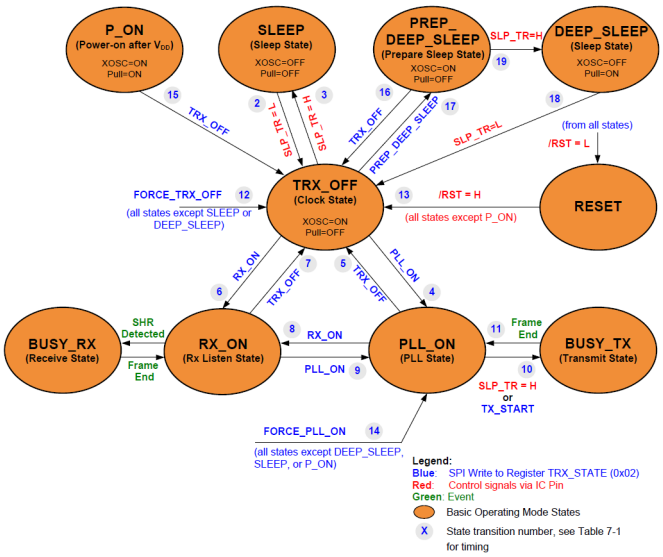
Atmel AT86RF230 and AT86RF233 vary in sleep state functionality. In AT86RF230, SLEEP state shown in the figure Basic Operating Mode State Machine for AT86RF230 is equivalent to DEEP_SLEEP state shown in the below figure for AT86RF233. Before entering into the DEEP_SLEEP state application should first enter into PREP_DEEP_SLEEP. Below table captures the electrical characteristics of SLEEP and DEEP_SLEEP states. For more details, refer to section Basic Operating Mode individual datasheets.

Note:
DEEP_SLEEP state can only be entered from PREP_DEEP_SLEEP state

Table 1-5. Current Consumption Specification

Transceiver	Supply current SLEEP state [µA]	Supply current DEEP_SLEEP state [µA]
AT86RF230	0.02	-
AT86RF233	0.2	0.02

Figure 1-2. Basic Operating Mode State Machine for AT86RF233



1.3. Extended Operating Mode

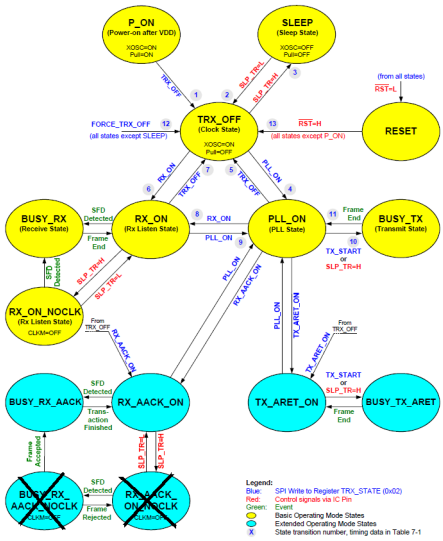
Atmel AT86RF230 and AT86RF233 vary in few transceiver states while operating in extended operating mode. Table Available State through Register Configuration (TRX_CMD) captures the states configurable through register TRX_STATE [4:0] (TRX_CMD). Figure Extended Operating Mode State Machine in AT86RF230 depicts the transceiver state removed in AT86RF230.

1.3.1. Migration of RX_ AACK_ON_NOCLK State to RX_AACK_ON

In extended operating mode RX_AACK_ON_NOCLK and BUSY_RX_AACK_NOCLK are not supported by AT86RF233 as shown in the below figure. Hence during migration RX_ AACK_ON_NOCLK state should be replaced by RX_AACK_ON state in AT86RF233. For more details, refer to section Extended Operating Mode in individual datasheets.

If application requires switching off CLKM in RX_AACK_ON state, then it has to be done manually to disable CLKM using register TRX_CTRL_0 [2:0].

Figure 1-3. Extended Operating Mode State Machine in AT86RF230

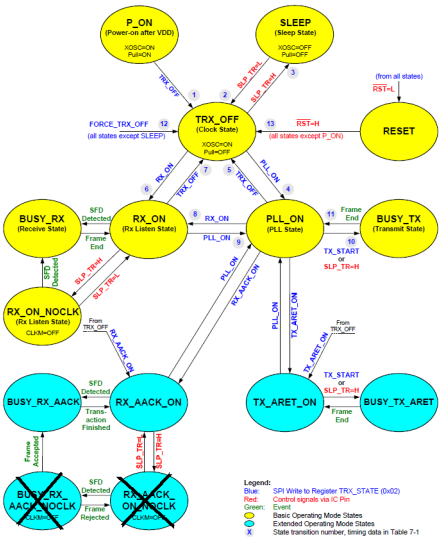


1.3.2. Migration of RX_ AACK_ON_NOCLK State to RX_AACK_ON

In extended operating mode RX_AACK_ON_NOCLK and BUSY_RX_AACK_NOCLK are not supported by AT86RF233 as shown in the below figure. Hence during migration RX_ AACK_ON_NOCLK state should be replaced by RX_AACK_ON state in AT86RF233. For more details, refer to section Extended Operating Mode in individual datasheets.

If application requires switching off CLKM in RX_AACK_ON state, then it has to be done manually to disable CLKM using register TRX_CTRL_0 [2:0].

Figure 1-4. Extended Operating Mode State Machine in AT86RF230



1.4. Faster State Transition Timing

Atmel AT86RF233 has improved in timing for few state transitions compared with Atmel AT86RF230. Below table captures the state transition timing differences for AT86RF230 and AT86RF233.

Table 1-6. State Transition Timings

State Transition	AT86RF230 [µs]	AT86RF233 [µs]
P_ON => TRX_OFF/CLKM	880	330
SLEEP => TRX_OFF	880	210
TRX_OFF => PLL_ON	180	80
TRX_OFF => RX_ON	180	80
RESET => TRX_OFF	120	26

Note:
Above State transition timings for AT86RF233 are only valid when capacitor (CB1/CB3) values are 100nF.

1.5. Part Number and Version Number

Atmel AT86RF230 and AT86RF233 vary in part number and version number. If the application firmware checks the transceiver's PART_NUM (0x1C) and VERSION_NUM (0x1D) registers, then it has to be changed according to below given tables.

Table 1-7. PART_NUM Register

Register name	AT86RF230	AT86RF233
PART_NUM (0x1C)	0x02	0x0B

Table 1-8. VERSION_NUM Register

Register name	AT86RF230	AT86RF233
VERSION_NUM (0x1D)	0x02 (Revision B)	0x01 (Revision A)

1.6. Drive Strength of Digital Pins

Atmel AT86RF230 controls the drive current of digital output pads and CLKM through register configuration (PAD_IO and PAD_IO_CLKM respectively). PAD_IO and PAD_IO_CLKM features were removed in Atmel AT86RF233. Hence output driver current of digital output pads and CLKM cannot be controlled through register configuration. Register bit field modifications with respect to AT86RF233 are captured in the below table. For more details, refer to section Register Reference in individual datasheets.

Table 1-9. TRX_CRTL_0

Register name	AT86RF230		AT86RF233	
	Register bits	Functionality	Register bits	Functionality
TRX_CRTL_0 (0x03)	[7:6]	PAD_IO	[7]	TOM_EN
			[6]	Reserved
	[5:4]	PAD_IO_CLKM	[5]	PMU_EN
			[4]	PMU_IF_INVERSE

Note:
AT86RF233 register reset values by default enable PMU_IF_INVERSE bit. Application should disable it during migration.

1.7. Automatic FCS Generation and Checking

AT86RF230 and AT86RF233 vary in register and bit field for configuring TX_AUTO_CRC_ON bit. Below table captures the register name and the bit for TX_AUTO_CRC_ON with respect to AT86RF233. For more details, refer to section Frame Check Sequence in individual datasheets

Table 1-10. TX_AUTO_CRC_ON Configuration

Feature	Register and bit field		Description
	AT86RF230	AT86RF233	
TX_AUTO_CRC_ON	PHY_TX_PWR[7]	TRX_CTRL_1[5]	Enabling this bit controls automatic FCS generation and validation during TX and RX respectively.

1.8. Renamed Registers and Bit Fields

AT86RF230 and AT86RF233 vary in the naming convention for the following mention in the below table.

Table 1-11. Renamed Registers and Bit Fields in AT86RF230 Compared to AT86RF233

Old name as per AT86RF230	New name as per AT86RF233	Description
XAH_CTRL	XAH_CTRL_0	Register has been renamed
BAT_LOW	IRQ_7_BAT_LOW	Register bit field has been renamed
TRX_UR	IRQ_6_TRX_UR	Register bit field has been renamed
TRX_END	IRQ_3_TRX_END	Register bit field has been renamed
RX_START	IRQ_2_RX_START	Register bit field has been renamed
PLL_UNLOCK	IRQ_1_PLL_UNLOCK	Register bit field has been renamed
PLL_LOCK	IRQ_0_PLL_LOCK	Register bit field has been renamed
I_AM_COORD	AACK_I_AM_COORD	Register bit field has been renamed

1.9. CSMA-CA Backoff Exponents

Atmel AT86RF230 and AT86RF233 vary in register and bit fields for configuring minimum backoff exponent (CSMA-CA algorithm). Below table captures the register name and the bit fields for configuring MIN_BE with respect to AT86RF233. For more details, refer to section Register Reference in individual datasheets.

Table 1-12. MIN_BE Configuration

Feature	Register and bit fields		Description
	AT86RF230	AT86RF233	
MIN_BE	CSMA_SEED_1 [7:6]	CSMA_BE[3:0]	Defines minimum backoff exponent for CSMA_CA algorithm

1.10. Digital Interface Timing Specifications

AT86RF230 and AT86RF233 vary in few digital interface timing specifications, as captured in below table.

Table 1-13. Digital Interface Timing Specification

Symbol	Parameter	Condition	AT86RF230		AT86RF233			Unit
			Min	Typ	Min	Typ	Max	
t_2	SCLK falling edge to MISO out	Data hold time	10	-	-	-	25	ns
t_7	SLP_TR pulse width	TX start trigger	65	-	62.5	-	-	ns
t_9	Last CLK rising edge to /SEL rising edge		250	-	-	250	-	ns

1.11. Active Bits Modified To Reserved Bits

Below table captures the bits modified to reserved bits in AT86RF233 compared to AT86RF230. In AT86RF233, it is recommended to write reset values to all reserved bits.

Table 1-14. Active bits modified to reserved bits in AT86RF233 compared to AT86RF230

Register name	Bit position	Reset value	Description
TRX_CTRL_0	[6]	0x0	In AT86RF230, this bit is LSB of PAD_IO (refer to Section Drive Strength of Digital Pins)
PHY_TX_PWR	[7]	0x0	In AT86RF230, this bit acts as TX_AUTO_CRC_ON bit. But in AT86RF233 TX_AUTO_CRC_ON bit is moved to TRX_CTRL_1 register (refer to Section Automatic FCS Generation and Checking)

1.12. Register Reset Values

AT86RF230 and AT86RF233 vary for few register reset values. AT86RF233 register reset values varied with AT86RF230's register reset values are captured in the below table.

Table 1-15. Register Summary – Reset Values

Address	Reset value		Description: Behavior of the migrated application with AT86RF233 reset value
	AT86RF230	AT86RF233	
0x03	0x19	0x09	-
0x04	0x00	0x22	TX_AUTO_CRC_ON (Section 1.3.5) and IRQ_MASK_MODE (Section 2.19) are enabled.
0x06	0x00	0x60	PHY_RSSI [6:5] denotes RND_VALUE, and is initialized to 0x03.
0x07	0x00	0xFF	ED_LEVEL holds 0xFF; this indicates no measurement has been started yet.
0x0A	0xBC	0x37	In AT86RF233, it is mandatory to keep the reset value 0x07 for PDT_THRES [2:0] if antenna diversity is disabled.
0x0C	0x04	0x20	OQPSK_SCRAM_EN [5] is enabled and OQPSK_DATA_RATE [2:0] is set to 250Kbps.
0x0E	0xFF	0x00	In AT86RF233, polling of interrupts is enabled by default (Section 2.18). Application should write the IRQ_MASK to the appropriate value to enable interrupt.
0x16	0x00	0xC1	No effect, RX_RPC_EN is disabled (Section 2.10)
0x19	0x55	0x00	ARET_FRAME_RETRIES and ARET_CSMA_RETRIES are set to zero.
0x1C	0x02	0x0B	If application checks for PART_NUM, check should be modified accordingly new reset value.
0x1D	0x02	0x01	If application checks for VERSION_NUM, check should be modified accordingly new reset value.
0x20	0x00	0xFF	SHORT_ADDR_0 is set to 0xFF
0x21	0x00	0xFF	SHORT_ADDR_1 is set to 0xFF
0x22	0x00	0xFF	PAN_ID_0 is set to 0xFF

Address	Reset value		Description: Behavior of the migrated application with AT86RF233 reset value
	AT86RF230	AT86RF233	
0x23	0x00	0xFF	PAN_ID_1 is set to 0xFF
0x2E	0xC2	0x42	Frame filter accepts frames with version number 0 and 1 (Section Frame Filter [2])
0x2F	0x00	0x53	MIN_BE is set to 0x03 similar to AT86RF230 and MAX_BE is set to 0x05 (Section 1.3.7 and Section 2.15).

1.13. Continuous Transmission Test Mode

Both Atmel AT86RF230 and AT86RF233 offer a Continuous Transmission Test Mode to support final application/production tests as well as certification tests.

Using this test mode the radio transceiver transmits continuously a previously downloaded frame data (PRBS mode) or a continuous wave signal.

But the software configuration procedure is changed for AT86RF233, refer Appendix A - Continuous Transmission Test Mode in AT86RF233 datasheet for more information.

2. Enhanced Features of AT86RF233

This chapter summarizes the enhancement and additional features of the AT86RF233 compared to the AT86RF230 transceiver.

2.1. Security Module (AES)

AT86RF233 has security module based on AES-128 core according to FIPS197 standard. Encryption and decryption can be performed in parallel with a frame transmission or reception. The security module (AES) features include:

- Hardware accelerated encryption and decryption
- Compatible with AES-128 standard (128-bit key and data block size)
- ECB (encryption/decryption) mode and CBC (encryption) mode support
- Stand-alone operation, independent of other blocks

The control of the security block is implemented as an SRAM access to address space 0x82 to 0x94. A Fast SRAM access mode allows for simultaneous new data writes and reads of processed data within the same SPI transfer. For more details, refer to section Security Module in AT86RF233 datasheet.

Note:
ECB decryption is not required by IEEE® 802.15.4 or ZigBee® security processing. The AT86RF233 provides this as an additional feature. And can be used as proprietary feature for IEEE 802.15.4 non-compliant application.

2.2. Random Number Generator

AT86RF233 incorporates a two bit truly random number generator by observation of noise. This random number can be used to:

- Generate random seeds for CSMA-CA algorithm
- Generate random values for AES key generation

Random numbers are stored in register bits RND_VALUE (register 0x06, PHY_RSSI). The random number is updated every tRND = 1µs in Basic Operation Mode receive states. The Random Number Generator does not work if the preamble detector is disabled (i.e. if RX_PDT_DIS = 1). For more details, refer to section Random Number Generator in AT86RF233 datasheet.

2.3. High Data Rate Modes

AT86RF233 also supports alternative data rates, higher than 250kb/s (up to 2000kbps) for applications beyond IEEE 802.15.4 compliant networks. The selection of a data rate does not affect the remaining functionality. Thus it is possible to run all features and operating modes of the radio transceiver in various combinations. The High Data Rate Modes occupy the same RF channel bandwidth as the IEEE 802.15.4 – 2.4GHz 250kb/s standard mode. For more details, refer to section High Data Rate Modes in AT86RF233 datasheet.

2.4. Antenna Diversity

To improve the reliability of an RF connection between network nodes Antenna Diversity can be applied to reduce effects of multipath propagation and fading. Antenna Diversity uses two antennas to select the

most reliable RF signal path. If a valid IEEE 802.15.4 frame is detected on one antenna, this antenna is selected for reception. Otherwise the search is continued on the other antenna and vice versa.

DIG1/DIG2 pins are enabled to drive the antenna switch control signals to the differential inputs of the RF Switch (SW1) to switch between ANT0 and ANT1. Antenna Diversity can be used in Basic and Extended Operating Modes and can also be combined with other features and operating modes like High Data Rate Mode and RX/TX Indication. For more details, refer to section Antenna Diversity in the Atmel AT86RF233 datasheet.

Note:
DIG2 pin is multifunctional pin. This pin can be either used for antenna diversity or for RX/TX frame time stamping. For more details on RX/TX frame time stamping refer to Section RX and TX Frame Time Stamping.

2.5. RX/TX Indicator

The control of an external RF front-end is done via two differential control pin pair DIG1/DIG3. The function of this pin pair is enabled with register bit PA_EXT_EN (register 0x04, TRX_CTRL_1). While the transmitter is turned off, pin 1 (DIG3) is set to low level and pin 2 (DIG4) to high level. If the radio transceiver starts to transmit, the two pins change the polarity. This differential pin pair can be used to control PA, LNA, and RF switches. The main features are:

- RX/TX indicator to control an external RF front-end
- Microcontroller independent RF front-end control
- Providing TX timing information

Note:
For more details, refer to section RX/TX Indicator in AT86RF233 datasheet.

2.6. RX and TX Frame Time Stamping

An exact timing of received and transmitted frames is signaled by AT86RF233 pin 10 (DIG2). A valid PHR reception or start of frame transmission is indicated by a DIG2 rising edge. The pin remains high during frame reception or transmission. TX Frame Time Stamping is limited to TX_ARET, whereas the RX Frame Time Stamping is available for all receive modes. For more details, refer to section RX and TX Frame Time Stamping in AT86RF233 datasheet.

Note:
DIG2 pin is multifunctional pin. This pin can be either used for antenna diversity or for RX/TX frame time stamping. For more details on antenna diversity refer to Section Antenna Diversity.

2.7. Frame Buffer Empty Indicator

For time critical applications that want to start reading the frame data as early as possible, the AT86RF233 Frame Buffer status can be indicated to the microcontroller through a dedicated pin. This pin indicates to the microcontroller if an access to the Frame Buffer is not possible since valid PSDU data are missing.

Pin 24 (IRQ) can be configured as a Frame Buffer Empty Indicator during a Frame Buffer read access. This mode is enabled by register bit RX_BL_CTRL (register 0x04, TRX_CTRL_1). The IRQ pin turns into Frame Buffer Empty Indicator after the Frame Buffer read access command and becomes valid after t12 = 750ns starting from the last SCLK rising edge while reading a Frame Buffer command byte. For more details, refer to section Frame Buffer Empty Indicator in AT86RF233 datasheet.

2.8. Dynamic Frame Buffer Protection

The AT86RF233 continues the reception of incoming frames as long as it is in any receive state. When a frame was successfully received and stored into the Frame Buffer, the following frame will overwrite the Frame Buffer content again. The Dynamic Frame Buffer Protection prevents that a new valid frame passes to the Frame Buffer until a Frame Buffer read access has ended. A received frame is automatically protected against overwriting:

- In Basic Operating Mode, if its FCS is valid
- In Extended Operating Mode, if an IRQ_3 (TRX_END) is generated

Note:
For more details, refer to section Dynamic Frame Buffer Protection in AT86RF233 datasheet.

2.9. Alternate Start-Of-Frame Delimiter

The value of the SFD can be changed if it is needed to operate in non-IEEE 802.15.4 compliant networks. A node with a non-standard SFD value cannot synchronize with any of the IEEE 802.15.4 network nodes. For more details, refer to section Alternate Start-Of-Frame Delimiter in the Atmel AT86RF233 datasheet.

2.10. Reduced Power Consumption Mode

AT86RF233 RPC offers a variety independent techniques and methods to significantly reduce the power consumption. RPC is applicable to several operating modes and transparent to other extended features. The Reduced Power Consumption mode is characterized by:

- Significant power reduction for several operating modes
- Self-contained, self-calibrating and adaptive power reduction schemes

Note:
For more details, refer to Reduced Power Consumption Mode in AT86RF233 datasheet.

2.11. Time-Of-Flight Module (TOM)

The AT86RF233 includes a set of means to trigger time measurements during message transfer. The time-of-flight measurement functions are characterized by:

- 24-bit Timer/Counter (T/C)
- Automated T/C start, capturing and reset
- Reference frequency error measurement
- Preamble synchronization monitoring

Note:
For more details, refer to section Time-Of-Flight Mode in AT86RF233 datasheet.

2.12. Phase Difference Measurement

The AT86RF233 performs a phase measurement of a received signal relative to an internal reference. The derived value represents the phase delay of the received signal referenced to an internal reference signal in the receiver low-IF domain. The Phase Difference Measurement Unit (PMU) is characterized by:

- Relative phase measurement of received signal

For more details, refer to section Phase Difference Measurement in AT86RF233 datasheet. Atmel AVR®2151: RTB Evaluation Application is available for range measurement application.

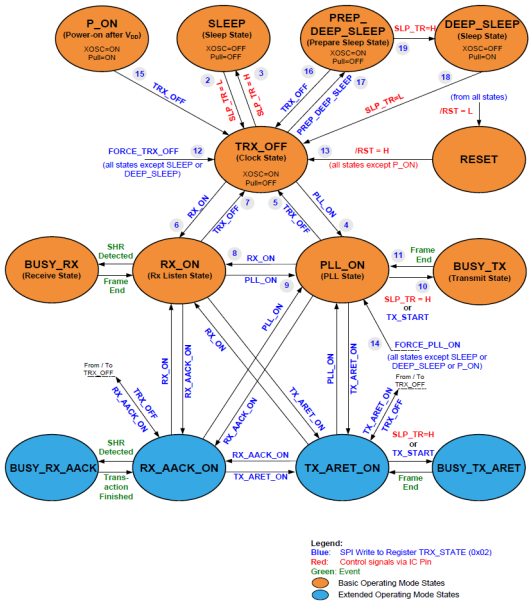
2.13. Extended Operating Mode State Transition

AT86RF233 supports additional TRX_STATE transitions in extended operating mode (as shown in the below figure) as follows:

- TX_ARET_ON <-> RX_AACK_ON
- TX_ARET_ON <-> TRX_OFF
- RX_AACK_ON <-> TRX_OFF
- FORCE_PLL_ON from all states except from SLEEP, DEEP_SLEEP and P_ON states
- FORCE_TRX_OFF from all states except from SLEEP and DEEP_SLEEP states

For more details, refer to section Extended Operating Mode in AT86RF233 datasheet.

Figure 2-1. Extended Operating Mode State Machine for Atmel AT86RF233



2.14. Data Retention after SLEEP State

In AT86RF233, after SLEEP state transceiver register contents and AES register contents remain valid while the contents of the Frame Buffer are lost. For more details, refer to Basic Operating Mode in AT86RF233 datasheet.

2.15. CSMA MAX Backoff Exponent

AT86RF230 supports only for configuring CSMA minimum backoff exponent. But AT86RF233 has dedicated register (CSMA_BE 0x2F) for setting CSMA MIN and MAX backoff exponents. For more details, refer to Register Reference in AT86RF233 datasheet.

2.16. Address Match Interrupt

Frame Filtering is a procedure that evaluates whether or not a received frame matches predefined criteria, like source or destination address or frame types. A filtering procedure as described in IEEE 802.15.4-2006 Section 7.5.6.2 (Third level of filtering) is applied to the frame to accept a received frame and to generate the address match interrupt IRQ_5 (AMI).

Frame filtering is available in Extended and Basic Operating Mode. A frame that passes the Frame Filter generates the interrupt IRQ_5 (AMI) if not masked. For more details, refer to section Frame Filter in the Atmel AT86RF233 datasheet.

2.17. AWAKE_END and CCA_ED_END Interrupts

In Atmel AT86RF233 IRQ_4 is a multi-functional interrupt, this particular interrupt is raised during the following scenarios:

1. IRQ_4 (AWAKE_END): entering the TRX_OFF state from P_ON, SLEEP, DEEP_SLEEP or RESET state.
2. IRQ_4 (CCA_ED_END): issued at the end of a manually initiated ED measurement.

For more details, refer to section Interrupt Logic in AT86RF233 datasheet.

2.18. Interrupt Mask Modes and Pin Polarity

AT86RF233 supports polling of interrupt events and IRQ pin polarity configuration.

- Interrupt polling is enabled by setting register bit IRQ_MASK_MODE in TRX_CTRL_1 register. When this bit is set to one, it allows masked off interrupt bits to reflect in the IRQ_STATUS
- The default polarity of the pin 24 (IRQ) is active high. The polarity can be configured to active low via register bit IRQ_POLARITY in TRX_CTRL_1 register

For more details, refer to section Interrupt Mask Modes and Pin Polarity in AT86RF233 datasheet.

Note:

1. If the “Frame Buffer Empty Indicator” is enabled during Frame Buffer read access, the IRQ pin has an alternative functionality.
2. This setting does not affect the polarity of the “Frame Buffer Empty Indicator”. The Frame Buffer Empty Indicator is always active high. Refer to section Frame Buffer Empty Indicator.

2.19. RF Channel Selection

The PLL is designed to support 16 channels in the 2.4GHz ISM band with channel spacing of 5MHz according to IEEE 802.15.4. Additionally, the PLL supports all frequencies from 2322MHz to 2527MHz with 500kHz frequency spacing. The frequency is selected by register bits CC_BAND (registers 0x14, CC_CTRL_1) and register bits CC_NUMBER (registers 0x13, CC_CTRL_0). For more details, refer to section RF Channel Selection in AT86RF233 datasheet.

2.20. Promiscuous Mode or Sniffer

The promiscuous mode is described in IEEE 802.15.4-2006, Section 7.5.6.5. If the AT86RF233 radio transceiver is in promiscuous mode, second level of filtering according to IEEE 802.15.4-2006, Section 7.5.6.2, is applied to a received frame. However, an IRQ_3 (TRX_END) is issued even if the FCS is invalid. Thus, it is necessary to read register bit RX_CRC_VALID (register 0x06, PHY_RSSI) after IRQ_3 (TRX_END) in order to verify the reception of a frame with a valid FCS.

In order to support sniffer application and promiscuous mode, only second level filter rules as defined by IEEE 802.15.4-2006, Section 7.5.6.2 are applied to the received frame. For more details, refer to section Frame Filter in AT86RF233 datasheet.

2.21. Reception of Reserved Frame Types

The reception of reserved frame types is an extension of the AT86RF233 Frame Filter. This might be required when implementing proprietary, non-standard compliant, protocols. Received frames are either handled like data frames, or may be allowed to completely bypass the Frame Filter. For more details, refer to section Reception of Reserved Frames in AT86RF233 datasheet.

2.22. Manual Filter Tuning (FTN)

Although receiver and transmitter are very robust against temperature and supply voltage variations, it is recommended to initiate the FTN manually if the radio transceiver does not use the SLEEP or DEEP_SLEEP states. If necessary, a calibration cycle is to be initiated in states TRX_OFF, PLL_ON or RX_ON.

Manual Filter tuning applies in particular for the High Data Rate Modes (see Section High Data Rate Modes) with a much higher sensitivity against Band Pass Filter transfer function variations. The recommended calibration interval is five minutes or less, if the AT86RF233 operates always in an active state (PLL_ON, TX_ARET_ON, RX_ON, and RX_AACK_ON). For more details, refer to section Automatic Filter Tuning AT86RF233 datasheet.

Note:
Full function devices will always operate in PLL_ON/ TX_ARET_ON/ RX_ON/ RX_AACK_ON and don't use SLEEP or DEEP_SLEEP states. In such cases it is recommended to use manual filter tuning.

2.23. Current Counter Values for Frame and CSMA Retries in Extended mode

In Atmel AT86RF233 provides new read-only register XAH_CTRL_2 to retrieve the current counter values for Extended Operating Mode like:

- ARET_FRAME_RETRIES: retrieves current frame retry counter value
- ARET_CSMA_RETRIES: retrieves current CSMA-CA retry counter value

For more details, refer to section Register Reference in AT86RF233 datasheet.

2.24. Slotted Operation

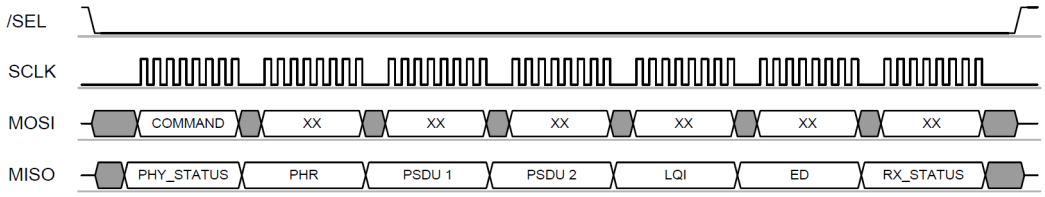
Using RX_AACK mode in networks operating in beacon or slotted mode, register bit SLOTTED_OPERATION indicates that acknowledgement frames are to be sent on backoff slot boundaries (slotted acknowledgement).

If register bit SLOTTED_OPERATION is set the acknowledgement frame transmission has to be initiated by the microcontroller using the rising edge of pin 11 (SLP_TR). This waiting state is signaled in register bits TRAC_STATUS (register 0x02, TRX_STATE) with value SUCCESS_WAIT_FOR_ACK. For more details, refer to section Register Reference in AT86RF233 datasheet.

2.25. Frame Buffer Read Access

In AT86RF233, during frame buffer read access two additional bytes ED and RX_STATUS values are appended at the end compared to AT86RF230 as shown in the following figure. Hence care should be taken while migrating from Atmel AT86RF230 to AT86RF233. For more details, refer to section Frame Buffer Access Mode in individual datasheet.

Figure 2-2. Frame Buffer Read Access Having Additional Information in AT86RF233



2.26. Radio Transceiver Status Information

In AT86RF233, each SPI access can return radio transceiver status information which is a first byte transmitted out of MISO output as the serial data is being shifted into MOSI input (as shown in figure Frame Buffer Read Access Having Additional Information in AT86RF233). Radio transceiver status information (PHY_STATUS) can be configured using register bits SPI_CMD_MODE (register 0x04, TRX_CTRL_1) to return TRX_STATUS, PHY_RSSI or IRQ_STATUS register. For more details, refer to section Radio Transceiver Status Information in AT86RF233 datasheet.

3. Typical and Electrical Characteristics

A Typical Characteristic section is added in the AT86RF233 datasheet, which is not available in AT86RF230.

Due to additional features of AT86RF233, electrical characteristics shall be different for both AT86RF230 and AT86RF233 transceivers. Check the latest datasheet for details.

4. Ordering Information

Table 4-1. Ordering Information

Ordering Code	Packaging	Package	Voltage Range	Temperature Range
AT86RF233-ZU	Tray	QN	1.8V – 3.6V	Industrial (-40°C to +85°C) Lead-free/ Halogen-free
AT86RF233-ZUR	Tape & Reel	QN	1.8V – 3.6V	Industrial (-40°C to +85°C) Lead-free/ Halogen-free

Note:
Tape & Reel quantity 5,000.

Contact your local Atmel sales office for more detailed ordering information and minimum quantities.

5. Contact

Atmel Technical Support - http://www.atmel.com/design-support/.

6. Revision History

Doc. Rev.	Date	Comments
42198B	10/2016	Non-technical updates
42198A	10/2013	Initial document release.

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Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**