
Introduction to HSIC

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INTRODUCTION

The High-Speed Inter-Chip (HSIC) interface is a two signal, source synchronous interface capable of providing USB High-Speed data at 480Mbps. The data transfers are 100% host driver compatible with traditional USB topologies. Full-Speed (FS) and Low-Speed (LS) are not supported by the format, however a hub with HSIC can provide FS and LS support. The most significant features of HSIC are:

- Different than USB in the physical layer only
- High-Speed data only, no chirp protocol
- Source-synchronous serial data transmission
- No hot removal/attach, interface is always connected
- 1.2V signal levels, designed for low-power applications at standard LVCMOS levels
- Maximum trace length of 10cm

This document includes the following topics:

- [HSIC Signaling on page 2](#)
- [HSIC Application Information on page 4](#)

Audience

This document is written for developers who are familiar with the USB protocol and specification but have limited knowledge regarding HSIC features. The goal of this application note is to familiarize the reader with HSIC and to address some common questions associated with implementing and testing HSIC applications.

References

The following documents should be referenced when using this application note. Refer to your Microchip representative for availability.

- High-Speed Inter-Chip USB Electrical Specification, Version 1.0
- Universal Serial Bus Specification, Revision 2.0

HSIC SIGNALING

Table 1 details all of the basic signaling protocols for HSIC. Many signals, such as CONNECT/RESUME and IDLE/SUSPEND are equivalent. Figure 1 illustrates a connect sequence (also see Connection Procedure), while Figure 2 illustrates a reset.

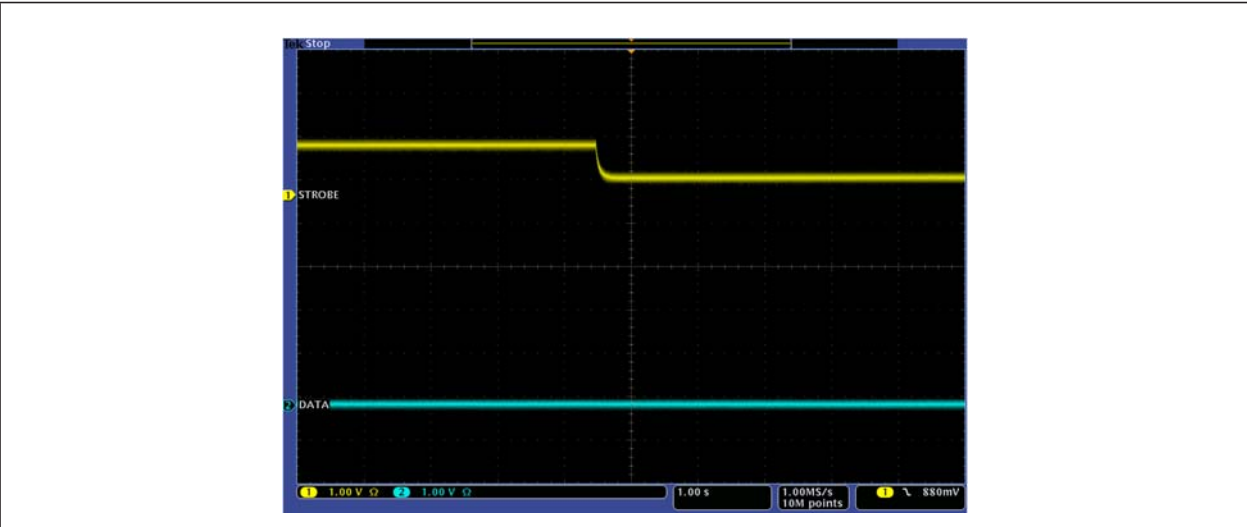
TABLE 1: HSIC SIGNALING SUMMARY

Signal	Strobe	Data	Description
IDLE	High	Low	1 or more strobe periods
CONNECT	Low	High	2 strobe periods
RESUME	Low	High	For time periods per USB 2.0 specification. RESUME can be signaled by either a host or a peripheral.
SUSPEND	High	Low	Identical to IDLE state
RESET	Low	Low	Per USB 2.0 specification

FIGURE 1: IDLE/SUSPEND TO CONNECT/RESUME SIGNALING

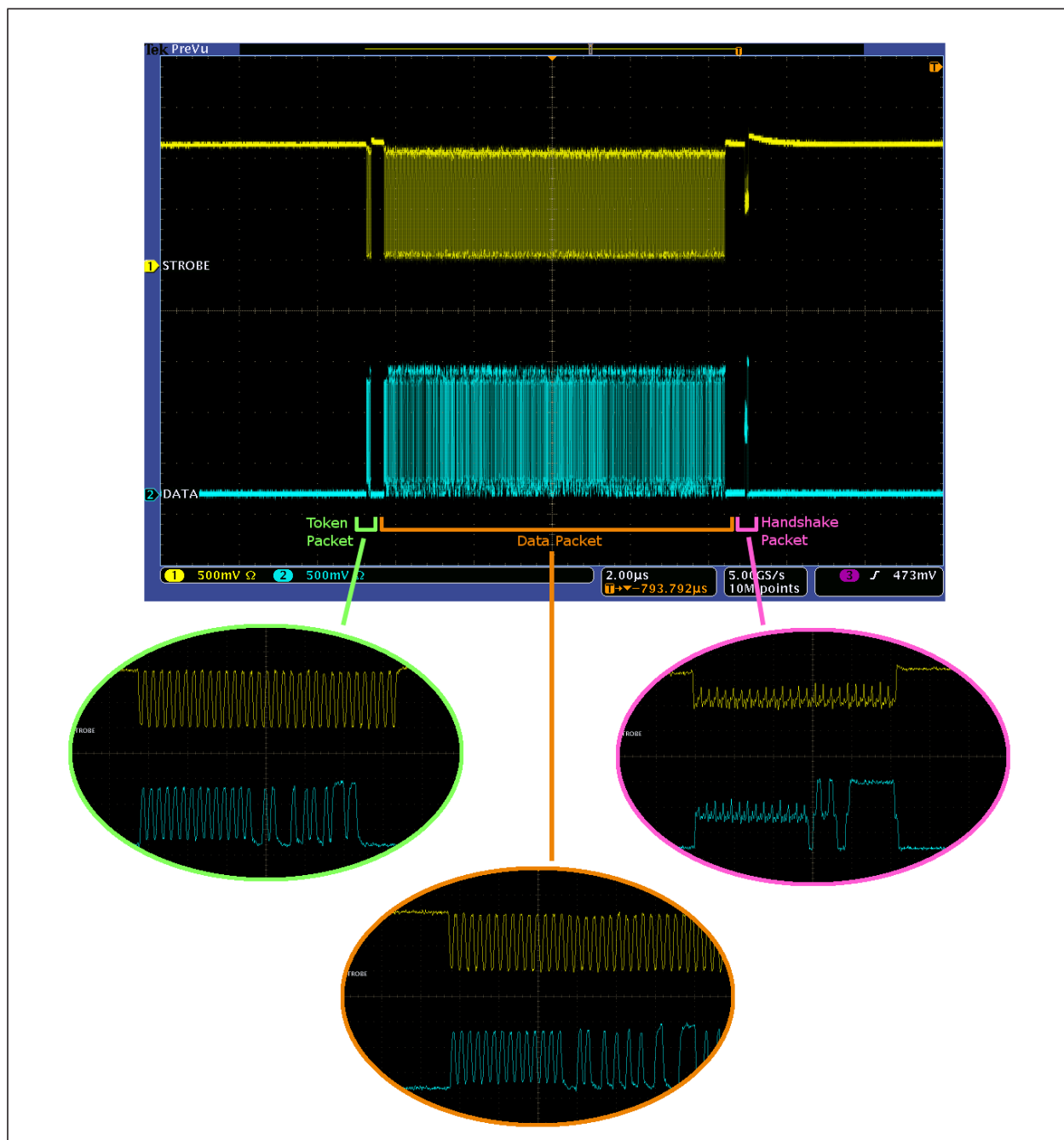


FIGURE 2: IDLE/SUSPEND TO RESET SIGNALING



Data signaling begins when STROBE and DATA lines transition from IDLE to END-OF-IDLE. END-OF-IDLE is defined as STROBE switching high to low while DATA is low. An example of a data transfer from a host to a device is shown in Figure 3.

FIGURE 3: DATA PACKET TRANSFERRED FROM HOST TO DEVICE



As seen in Figure 3, The protocol for data transactions between host and device via HSIC is the same as USB. The primary difference is that all information is transmitted via a single data line, and a strobe signal communicates when to sample the received data signal. HSIC uses double data rate (DDR) signaling; data is sampled at both the rising and falling edges of the strobe signal. The strobe signal oscillates at a frequency of 240Mhz, which provides a total data rate of 480Mbps.

Note: The distortion seen in the handshake packet is explained in the [Probing HSIC Signals](#) section.

HSIC APPLICATION INFORMATION

HSIC offers several notable advantages over USB for hard-wired inter-chip applications. HSIC is a fully digital standard and thus no analog front end is required. The lack of an analog front end allows for reduction in die sizes, and can therefore lead to reduced cost. Additional die reduction can be made due to the decreased amount of digital logic required by the simplified connection protocol.

The HSIC standard does not inherently reduce power consumption, but the removal of the analog front end can lead to lower power designs, especially since analog circuitry does not necessarily scale one-to-one with digital circuits for reductions in process feature size. HSIC is especially low power when placed into the suspended state. During suspend, there is no current draw on the STROBE or DATA lines. By comparison, standard USB draws a minimum of 200 μ A on D+ through a 1.5k Ω pull-up resistor when suspended.

Because HSIC is only different from USB at the physical layer, making the migration from USB to HSIC is not like changing to a completely new standard. This means that existing USB software stacks and USB protocol knowledge bases can be quickly transitioned to HSIC.

The remaining sections discuss some more in-depth topics aimed at easing troubleshooting and answering common HSIC application concerns.

HSIC Data Sampling

With standard USB, every data packet begins with a sync pattern to allow the receiver clock to synchronize with the phase of the incoming data. The differential sign of the D+/D- signal is then sampled according to the sync pattern. HSIC uses a separate STROBE line to tell the receiver when to sample the incoming data. The HSIC DATA signal is sampled at the rising and falling edges of the STROBE signal. If the STROBE and DATA signals become skewed for any reason, the sampled data may become corrupted. The HSIC Electrical Specification defines the maximum allowable skew as 15ps.

To ensure skew does not become an issue, the design must adhere to the following requirements:

- The HSIC traces must be kept as short as possible and must not exceed 10 cm in length.
- The DATA and STROBE traces must be equal in length.
- The DATA and STROBE traces should be routed to 50 Ω single-ended impedance.

To illustrate the amount of skew possible in the real world, [Figure 4](#) shows the beginning of a test packet transmitted from a host to a device through HSIC with equal lengths. [Figure 5](#) shows the same packet transmitted from the same host with a STROBE trace that is approximately 10cm longer than the DATA trace. The resulting skew is approximately half of a nanosecond. This is an extreme example, but the results suggest that even a small amount of length mismatch may result in an HSIC specification violation.

FIGURE 4: EQUAL HSIC TRACE LENGTHS

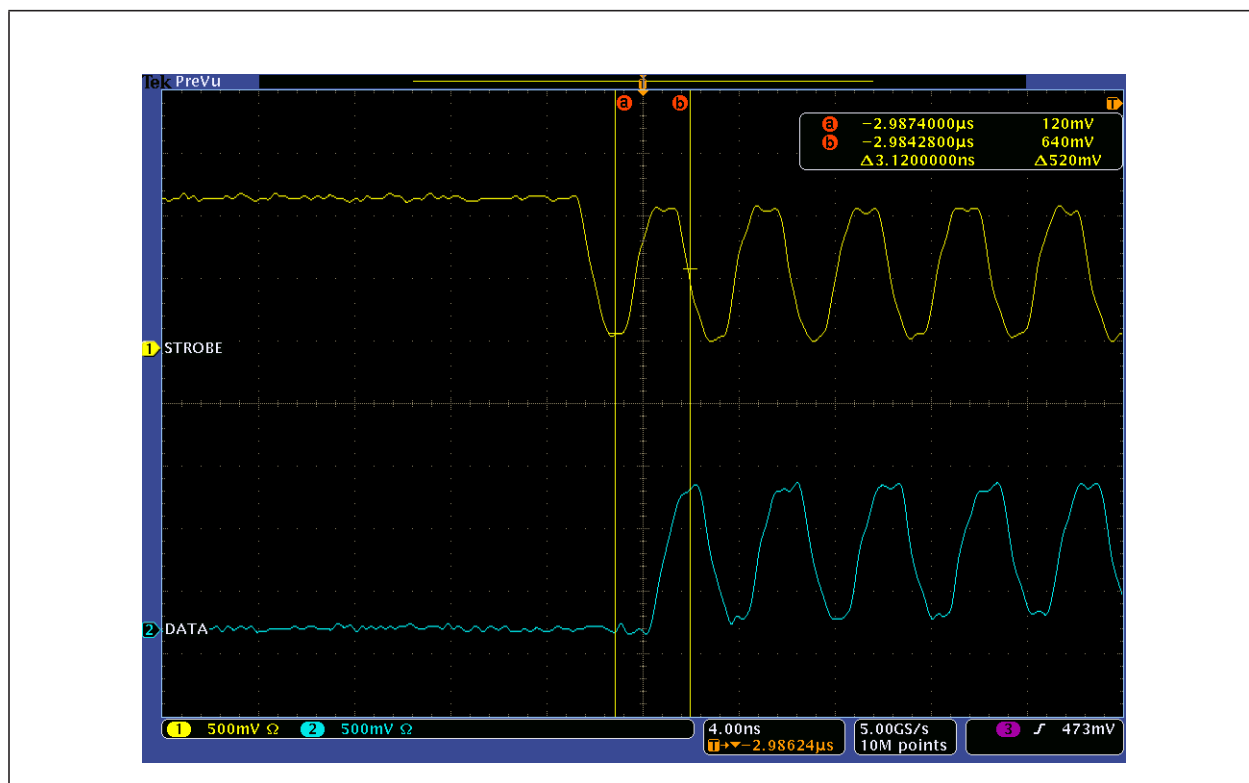
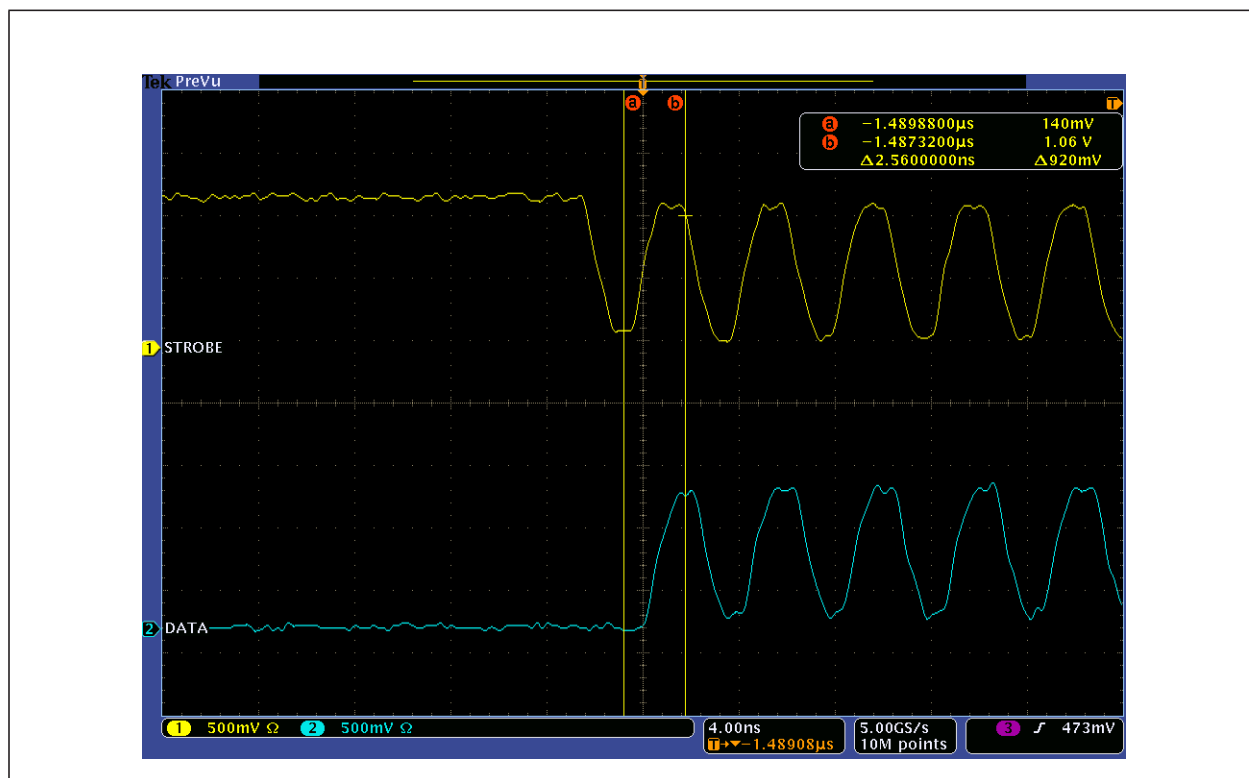


FIGURE 5: STROBE TRACE 10CM LONGER THAN DATA TRACE



Probing HSIC Signals

The single-ended nature and differences in signal termination present some challenges when attempting to probe HSIC lines. Standard USB signals can be easily monitored and deciphered by placing a differential probe connected to an oscilloscope at either the transmitter side or receiver side. HSIC signals are more sensitive and one must consider transmission line theory when attempting to probe them.

A good general guideline is to probe at the side opposite to the source of the signal that you would like to observe. For instance, if you wish to observe the signals originating from a device, place a probe at the host-side terminals. If you wish to observe the signals originating from a host, place the probes at the device-side terminals.

When attempting to probe signals originating from a device while probing at the device side, the signal becomes distorted. This is likely due to interference caused by the signal reflecting back on itself. One can also probe at the middle of the trace, but the results are typically not as clean as if probed properly from one side. An ideal solution is to probe simultaneously from both ends. A series protocol analyzer may be able to accurately sample the signals in both directions, but the 10 cm trace length restriction makes this option impractical.

To illustrate the effects of probing at various points, a test packet was generated at a host down to a hub connected through HSIC. [Figure 6](#) shows clean signals probed from the hub side. [Figure 7](#) shows distorted signals probed from the host side.

FIGURE 6: SIGNALS PROBED AT DEVICE/HUB SIDE TERMINALS

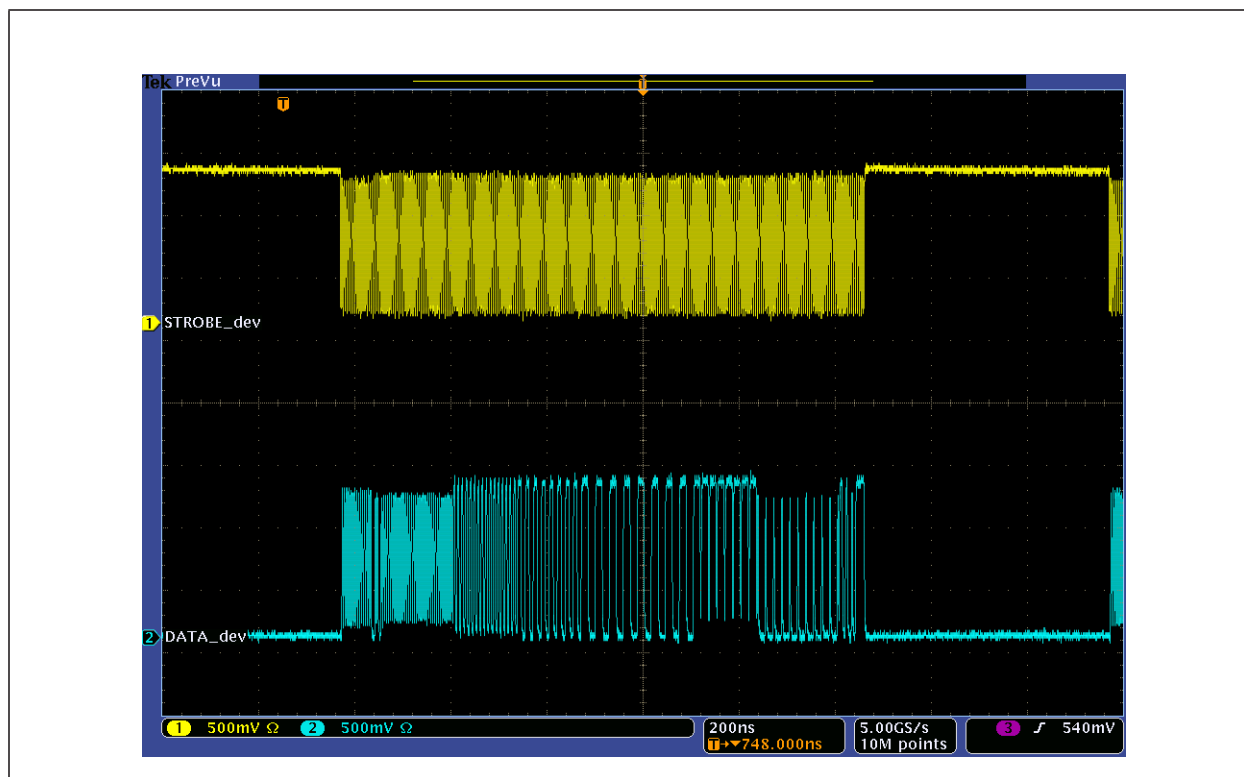
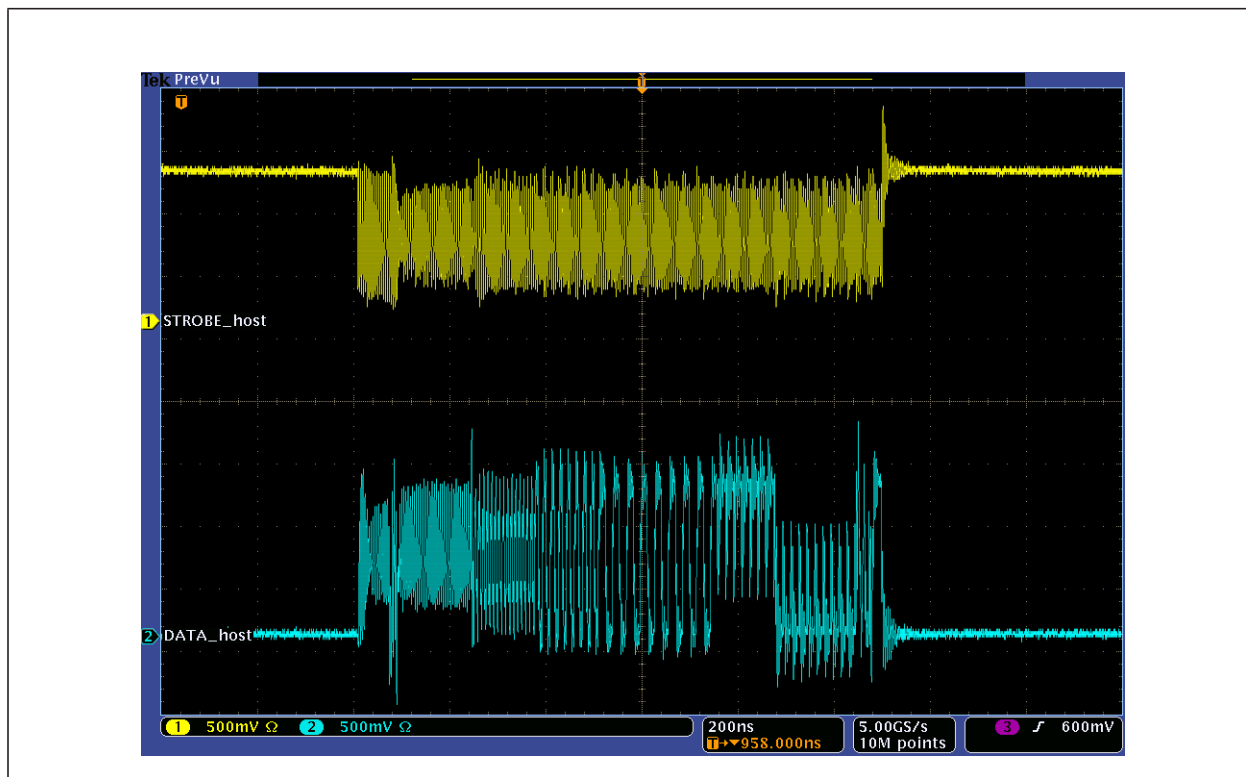


FIGURE 7: SIGNALS PROBED AT HOST SIDE TERMINALS



Connection Procedure

It is important to understand the connection procedure when troubleshooting some issues involving HSIC connectivity. The HSIC interface is structured in such a way that a host or peripheral can be powered on in any order. To ensure that a false connection is not detected, the host, hub, and peripherals must ensure that STROBE or DATA do not float to an undetermined value (also commonly referred to as tri-stated). The sequence of events that lead to a connect event is detailed below.

TABLE 2: DEVICE/HUB DISCOVERY AND CONNECTION SEQUENCE

Conditions	Downstream Facing Host/Hub Action	Upstream Facing Device/Hub Action
Powered ON, HSIC disabled	Must assert STROBE and DATA lines to provide a logic '0' state	No signal assertion
Powered ON, HSIC enabled	Present an IDLE bus state and monitor for a CONNECT bus state	Monitor STROBE and DATA lines for an IDLE bus state
Powered ON, HSIC enabled, and peripheral sends CONNECT signal	Commence enumeration upon receiving a CONNECT bus state	Must assert a CONNECT bus state upon detecting an IDLE state

Figure 1 in the previous section shows an oscilloscope capture of a connect sequence. This connect sequence is much simpler than the USB connect sequence because there are no speeds to negotiate. This sequence can be handled by a very simple state machine, reducing die size requirements.

DISCONNECTION/RECONNECTION AND DISABLE/SUSPEND

With standard USB, the host is capable of determining if a downstream port has been disconnected by monitoring the magnitudes of the DP/DM signal voltages. If the voltage exceeds the disconnect voltage threshold, the host can conclude that the device has been disconnected. HSIC does not support a disconnect protocol because it is intended to be a hard-wired, always on connection. However, it is still possible to get into a situation where a downstream device may appear to have disconnected, and care must be taken to ensure that the host does not permanently lose its connection with the device.

This apparent disconnection, or “standoff”, can occur because the host always maintains an IDLE state while the bus is unused, and the IDLE state is identical to the SUSPEND state from a signal perspective. The host has no way of knowing if or when a downstream device has been powered down or disconnected. Since the SUSPEND signaling is identical to the IDLE signaling, it is possible to reach a state where a downstream device believes it is has been suspended while the upstream host thinks there is no device downstream and waits indefinitely for a CONNECT signal to arrive. A similar standoff condition could occur if the upstream host disables the port while the device believes it has been suspended.

This condition is not likely to occur between hosts and devices that never cycle power or soft reset. In the even that this issue is encountered it must be dealt with in an application specific manner at either the Link or software stack level. This issue can be dealt with by programming the software stack or designing the Link in such a way that prevents the condition from occurring in the first place. Alternatively, the SoC can attempt to deal with a downstream device after it “disconnects” in one of two ways:

- Reset the HSIC hub. The device discovery sequence will occur and the connection will be reestablished.
- On Microchip USB254x/USB3613/USB3813/USB4604/USB4624 family of devices, the SoC can use the VBUS_DET pin to reestablish the connection. Pulling the pin low suspends the hub while pulling the pin high will wake it up.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
REV A (11-26-13)	All	Initial release

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