TB3148

Oscillator Module Technical Brief

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INTRODUCTION

The PIC16(L)F183XX device family contains an oscillator module that has a wide variety of clock sources and selection features that allow it to be used in a wide variety of applications while maximizing performance and minimizing power consumption.

External clock sources are supplied from external oscillators, or from quartz crystal or ceramic resonators.

Internal clock sources are supplied from one of two internal oscillator circuits – the High-Frequency Internal Oscillator (HFINTOSC), or the Low-Frequency Internal Oscillator (LFINTOSC).

The following registers are used to configure the system oscillator:

- Configuration Word 1
- Oscillator Control Register 1 (OSCCON1)
- Oscillator Control Register 2 (OSCCON2)
- Oscillator Control Register 3 (OSCCON3)
- Oscillator Status Register (OSCSTAT1)
- HFINTOSC Frequency Selection Register (OSCFRQ)
- HFINTOSC Tuning Register (OSCTUNE)

REGISTERS

Configuration Word 1

Configuration Word exclusively handles the oscillator configuration.

The FCMEN bit enables or disables the Fail-Safe Clock Monitor (FSCM). The FSCM is designed to detect a failure of the external clock source and automatically switch to an internal clock source to prevent the failure of code execution.

The $\overline{\text{CLKOUTEN}}$ bit enables or disables the output of a scaled system clock (FOSC/4).

The Reset Oscillator bits (RSTOSC<2:0>) allow the user software to begin operation from either an internal or external clock source upon power-up or Reset. There are several oscillator options to choose from:

- External Oscillator
- External Oscillator with 4x PLL
- Secondary Oscillator
- Low-Frequency Internal Oscillator
- High-Frequency Internal Oscillator
- High-Frequency Internal Oscillator with 2x PLL

The FEXTOSC<2:0> bits set the External Oscillator mode based on the type of external clock source that is used – either an external clock or crystal oscillator – upon power-up or Reset. When an external clock source is selected, the FEXTOSC<2:0> bits must be configured to match the type of external source that is used. There are several external oscillator options to choose from:

- EC (External Clock) high (above 8 MHz)
- EC medium (0.5 – 8 MHz)
- EC low (below 0.5 MHz)
- HS (crystal oscillator) (above 8 MHz)
- XT (crystal oscillator) (0.5 – 8 MHz)
- LP (crystal oscillator) (below 0.5 MHz)

The Clock Switch Enable (CSWEN) bit is used to either allow or prevent a clock switch from occurring once the user software begins to execute, except in the case of an external clock source failing and the Fail-Safe Clock Monitor switches to the internal clock. When the CSWEN bit is set, clock switching is allowed and can be done any time after the user code begins execution. When CSWEN is clear, clock switching is prevented, and the oscillator selected by the RSTOSC<2:0> bits will remain the active oscillator.

Oscillator Control Registers 1 and 2 (OSCCON1, OSCCON2)

The OSCCON1 register contains two important bit fields that can be read or written to:

- New Oscillator Source Request bits (NOSC<2:0>)
- New Divider Selection Request bits (NDIV<3:0>)

The NOSC bits can be written to if a new clock source is desired, as long as the CSWEN bit is set, allowing clock switching to take place. The NDIV bits can be written to in order to divide the selected clock source.

The OSCCON2 register also contains two very similar bit fields; however, these are read-only bit fields:

- Current Oscillator Source Select bits (COSC<2:0>)
- Current Divider Select bits (CDIV<3:0>)

The COSC bits can be read at any time to determine the current oscillator selection, and the CDIV bits can be read at any time to determine the current clock divider.

Upon power-up or Reset, the value written into the RSTOSC<2:0> bits of Configuration Word 1 are automatically written into both the NOSC and COSC bit fields. The value of '0100' is automatically written into the NDIV and CDIV bit fields, with the exception of when the 32 MHz HFINTOSC source is selected. In that case, the value of '0000' is written into NDIV and CDIV.

Oscillator Control Register 3 (OSCCON3)

The Clock Switch Hold (CSWHOLD) bit can be used to control when a clock switch takes place.

The New Oscillator is Ready (NOSCR) bit indicates when the new clock source is stable and ready.

The Oscillator Ready (ORDY) bit indicates that the clock source is ready.

Oscillator Status Register 1 (OSCSTAT1)

The OSCSTAT1 register contains the read-only oscillator Status bits, indicating when the selected clock source is ready. When a clock source is selected, its Status bit will remain clear until the source is ready. The oscillator Status bits include the following:

- External oscillator
- HFINTOSC
- LFINTOSC
- Secondary Oscillator
- PLL

HFINTOSC Frequency Selection Register (OSCFRQ)

The OSCFRQ register contains the HFFRQ<3:0> bit field which defines the HFINTOSC frequency.

Upon power-up or Reset, the HFFRQ<3:0> bits are loaded automatically with the value of '0110', which sets the base HFINTOSC clock at 16 MHz.

When the HFINTOSC at 1 MHz clock source is selected by writing '110' into the RSTOSC bits, the value '0110' is loaded into the HFFRQ bit field, and the NDIV and CDIV bit fields are loaded with the value '**0100**', or divide by 16 (see Figure 1).

When the HFINTOSC with PLL clock source is selected by writing '000' into the RSTOSC bits, the same '0110' value is written into the HFFRQ bits; however, the value of '0000', or no divider, is written into the NDIV and CDIV bit fields. The 16 MHz clock signal is then routed through an internal 2x PLL to generate the 32 MHz system clock (see Figure 2).

It is important to consider both the HFFRQ and NDIV bits when changing FOSC frequencies. For example, if the RSTOSC bits were configured for the 1 MHz HFINTOSC, writing to the HFFRQ bits will change the frequency; however, the NDIV bits will remain at a divide by 16 unless a new divider is written (see Figure 3).

HFINTOSC Tuning Register (OSCTUNE)

The OSCTUNE register allows fine tuning of the HFINTOSC source. Fine tuning of the HFINTOSC source can be useful when compensating for oscillator drift over temperature.

CLOCK SOURCE TYPE

Clock sources can be classified as either external or internal. External clock sources rely on external circuitry for the clock source to function. Internal clock sources utilize built-in oscillator blocks.

External Sources

Writing the appropriate bit code into the RSTOSC<2:0> bits of Configuration Word 1 will select one of the following external clock sources:

- External Oscillator
- External Oscillator with 4x PLL
- Secondary Oscillator

EXTERNAL OSCILLATOR

When the External Oscillator is selected, the FEXTOSC<2:0> bits must be configured to match the type and speed of the external clock source, which is determined by the application hardware.

In External Clock (EC) mode, an externally generated logic level signal is used for FOSC. EC mode has three power modes to select from:

- ECH – High-Power mode with a frequency range of 8-32 MHz
- ECM – Medium Power mode with a frequency range of 100 kHz to 8 MHz
- ECL – Low-Power mode with a frequency range below 100 kHz.

When a quartz crystal or ceramic resonator is used as the external clock source, there are also three power modes that can be selected from based on the type and frequency:

- LP mode – selects the lowest gain setting of the internal inverter-amplifier circuit but is designed to drive only a 32.768 kHz tuning-fork type crystal (watch crystal).
- XT mode – selects the medium gain setting of the internal inverter-amplifier circuit and is best suited to drive quartz crystal or ceramic resonators with a medium-drive level specification, with a frequency range of 100 kHz to 8 MHz.
- HS mode – selects the highest gain setting of the internal inverter-amplifier circuit and is best suited for quartz crystal or ceramic resonators that require a high-drive setting, with a frequency range above 8 MHz.

EXTERNAL OSCILLATOR WITH 4X PLL

When the external oscillator with 4x PLL is selected (RSTOSC = 001), an internal 4x PLL circuit is used in combination with an external clock source to provide the FOSC.

It should be noted that when using the 4x PLL, the clock source must be one that will not exceed the maximum allowable device frequency.

The FEXTOSC<2:0> bits must also be configured to match the type and speed of the external clock source.

SECONDARY OSCILLATOR

When the secondary oscillator is selected (RSTOSC = 011), an external 32.768 kHz quartz crystal resonator or externally generated logic level signal is used as the clock source. The secondary oscillator can be used either as the main FOSC or as a secondary source.

Internal Sources

HFINTOSC

When the RSTOSC<2:0> bits are configured so that the High-Frequency Internal Oscillator (HFINTOSC) is selected as the clock source upon power-up or Reset, an internal base clock of 16 MHz is established.

There are two selections for the HFINTOSC:

- HFINTOSC at 1 MHz (no PLL)
- HFINTOSC at 32 MHz (using 2x PLL)

When the HFINTOSC without the 2x PLL is selected, the value of '110' is automatically written into the NOSC and COSC bit fields, and a value of '0100' is automatically written to both the NDIV and the CDIV bit fields. This configures the output of the oscillator circuit to be 1 MHz.

When the HFINTOSC with 2x PLL is selected, the value of '000' is automatically written into the NOSC and COSC bit fields, and the value of '0000' is written into both the NDIV and CDIV bit fields, indicating that no clock divider is needed. The 16 MHz base clock is then routed through the PLL to generate the 32 MHz system clock.

It is important to keep in mind that whenever the HFINTOSC is selected by writing the appropriate code into the RSTOSC bits, a base 16 MHz clock is generated. The base clock is then either divided down to get the 1 MHz system clock, or routed through the internal PLL system to multiply the base clock to the 32 MHz system clock.

LFINTOSC

When the RSTOSC<2:0> bits are configured so that the Low-Frequency Internal Oscillator (LFINTOSC) is selected, a factory calibrated 31 kHz internal clock source as the clock source upon power-up or Reset.

The LFINTOSC is the clock source for the power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

CLOCK SWITCHING

The system clock source can be switched between external and internal clock sources via software using the NOSC and NDIV bits of the OSCCON1 register.

When a new clock source is selected by writing to NOSC, the current oscillator will continue to operate until the new source is stable and ready. When the new source is ready, both the NOSCR bit and the Clock Switch Interrupt Flag (CSWIF) bit of the PIR3 register become set. If Clock Switch Interrupts are enabled, an interrupt will be generated at that time. The ORDY bit can also be polled to determine when the new oscillator is ready.

The current COSC and CDIV values are indicated in the OSCCON2 register up to the moment when the switch actually occurs, at which time OSCCON2 is updated and ORDY is set. NOSCR is cleared by hardware to indicate that the switch is complete.

If CSWHOLD is clear, the oscillator switch will occur as soon as the NOSCR bit is set. If the Clock Switch Interrupts are enabled, the interrupt will be serviced at the new clock setting.

If CSWHOLD is set, the clock switch is suspended, and the oscillator module will continue to operate with the current (old) clock. Once the NOSCR bit is set, the clock switch occurs when the user software clears the CSWHOLD bit. The switch can also be abandoned by leaving the CSWHOLD bit set and writing the value that is currently in COSC into NOSC.

Changing the clock divider without changing the clock source (for example, changing FOSC from 1 MHz to 2 MHz) is handled in the same manner as a clock source switch, with the exception of writing the new divider into NDIV. CSWHOLD must be clear for the switch to complete.

Switching between the PLL and any non-PLL source is managed as described above. The input to the PLL is established when value written into NOSC selects the PLL.

When NOSC and COSC select the PLL with different input sources, the system continues to run using the COSC setting, and the new source is enabled per NOSC. When the new oscillator is ready and CSWHOLD is clear, system operation is suspended while the PLL input is switched and the PLL acquires lock.

There is more than one way to change the FOSC frequency during code execution. The following two examples illustrate different methods to achieve a 4 MHz FOSC clock when the default oscillator is HFINTOSC:

Method 1

1. Configure the RSTOSC bits so that the HFINTOSC at 1 MHz is selected as the clock source (RSTOSC<2:0> = `110`).
2. During code execution, write the value of '`0011`' into the HFFRQ<3:0> bits of the OSCFRQ register, which sets the HFINTOSC frequency to 4 MHz.
3. Write the value '`0000`' to the NDIV bits to select a divide by one clock divider.

Method 2

1. Configure the RSTOSC bits so that the HFINTOSC at 1 MHz is selected as the clock source (RSTOSC<2:0> = `110`).
2. During code execution, write the value of '`0010`' to the NDIV bits to select a divide by four clock divider.

It is important to keep in mind that whenever the HFINTOSC is selected by writing the appropriate code into the RSTOSC bits, a base 16 MHz clock is generated. The base clock is then either divided down to get the 1 MHz system clock, or routed through the internal PLL system to multiply the base clock to the 32 MHz system clock.

When the HFINTOSC is selected during code execution, and was not the default oscillator selected by the RSTOSC bits, it will be necessary to write to two registers:

1. Write the appropriate code into the HFFRQ<3:0> bit field of the OSCFRQ register to select the desired base frequency.
2. Write either '`110`' or '`000`' to the NOSC<2:0> bit field of the OSCCON1 register to select one of the two HFINTOSC sources, and write the appropriate code into the NDIV<3:0> bit field of OSCCON1 to select the desired divider.

FIGURE 1: HFINTOSC = 1 MHz UPON POWER-UP OR RESET

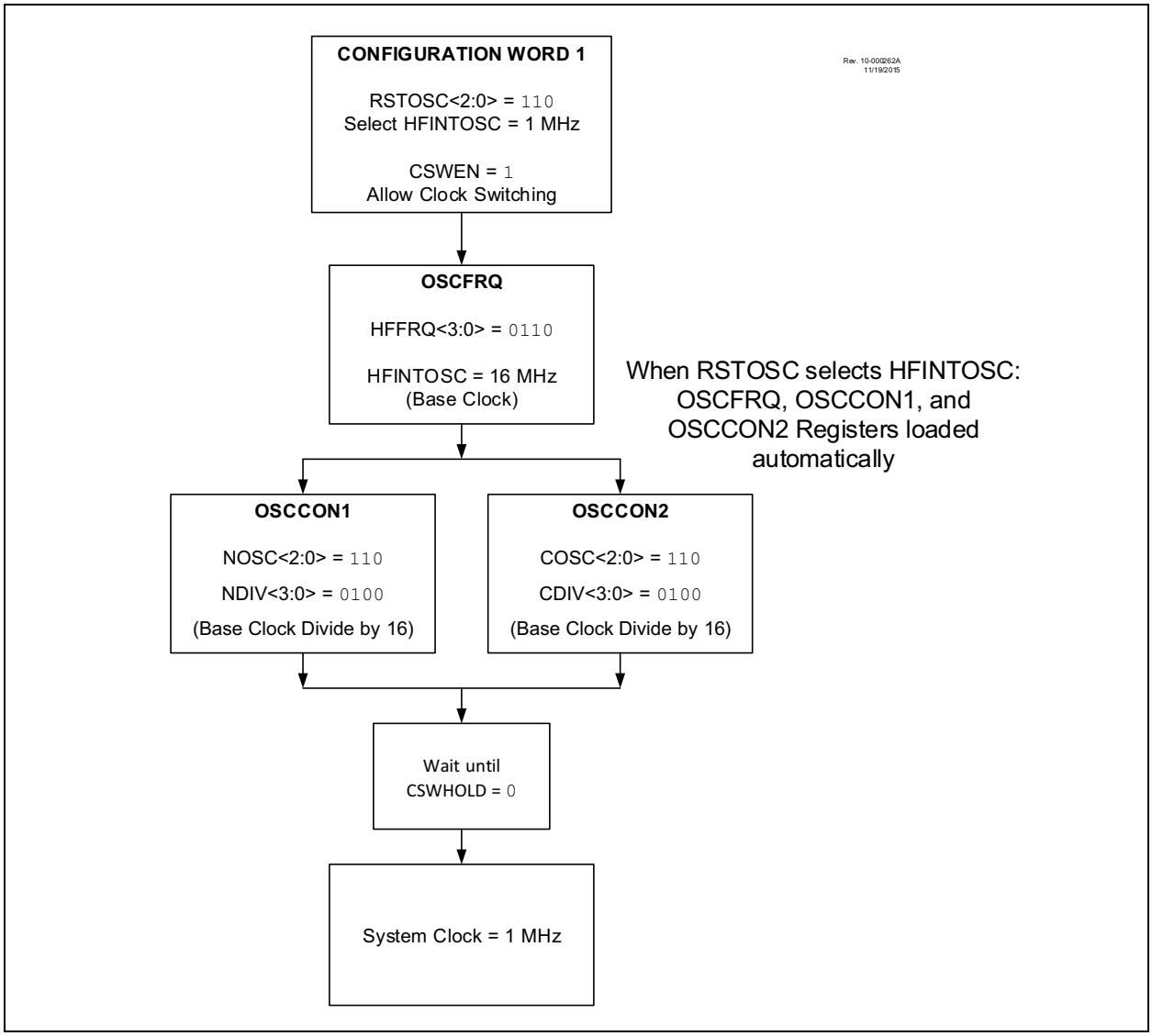


FIGURE 2: HFINTOSC = 32 MHz UPON POWER-UP OR RESET

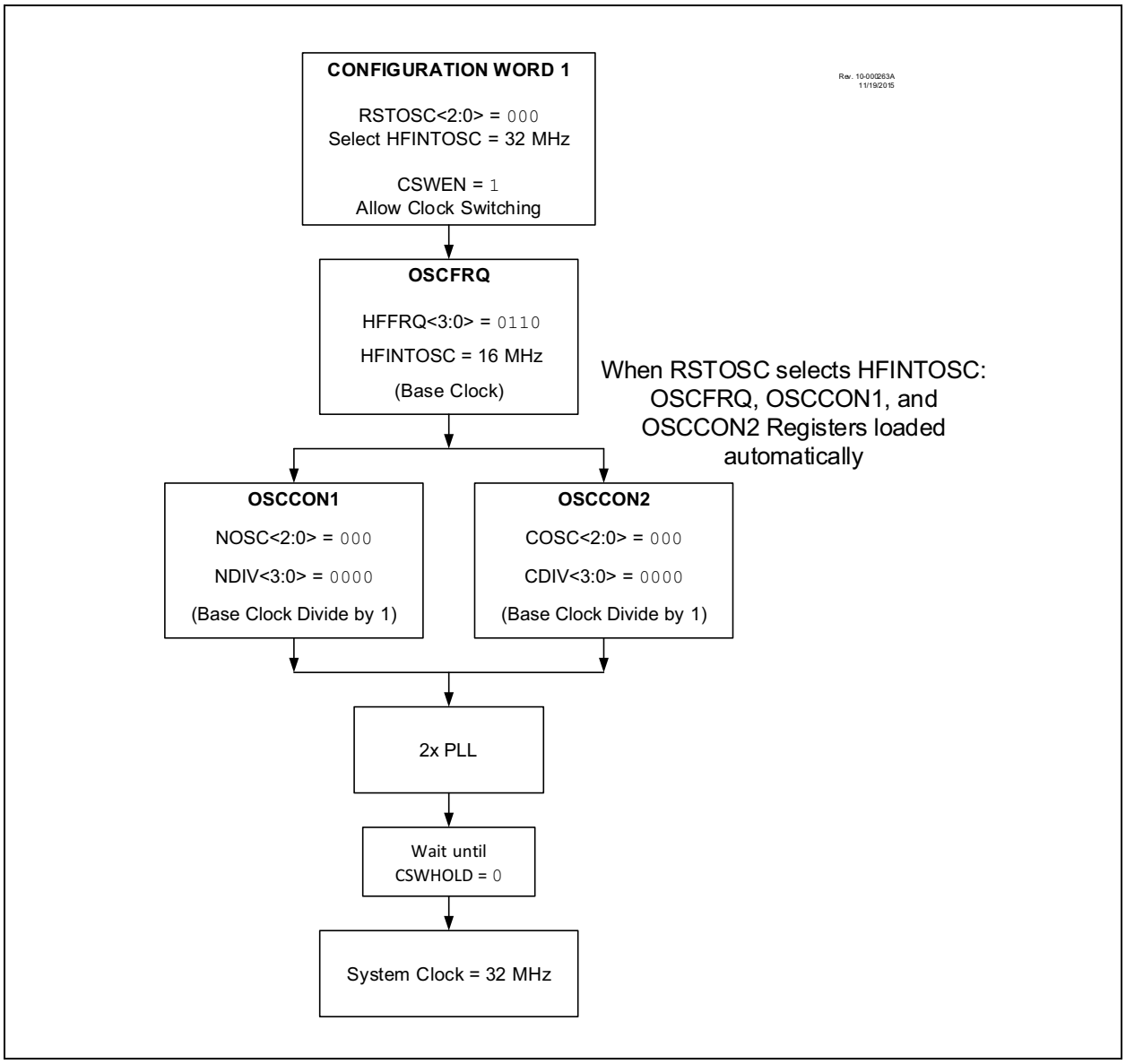
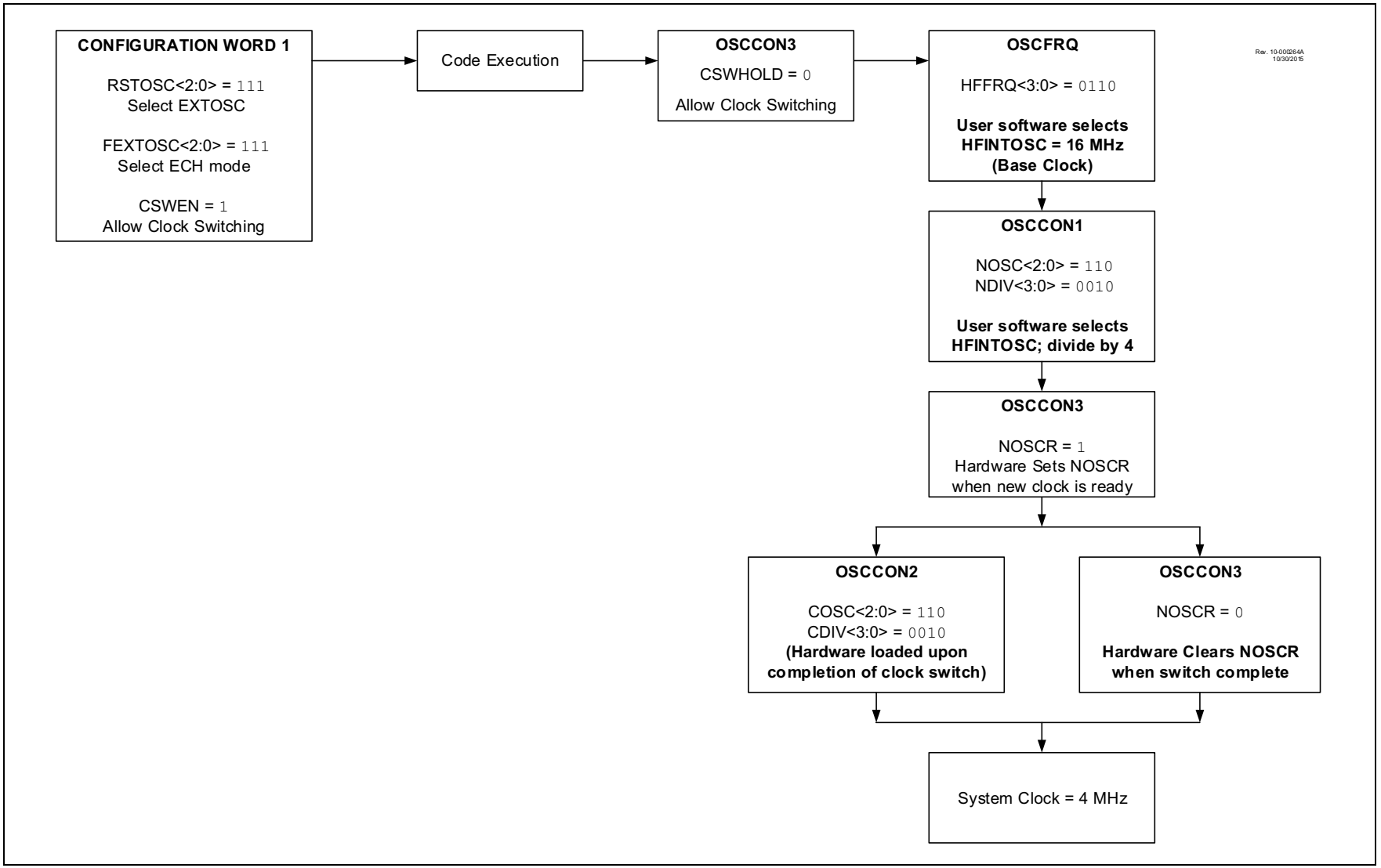


FIGURE 3: EXTERNAL OSCILLATOR TO HFINTOSC CLOCK SWITCH



EXAMPLE 1: SIMPLE EXTOSC TO HFINTOSC CLOCK SWITCH CODE EXAMPLE

```
/*
 * File: main.c
 * Author: Chris Best,
 * MCU8 Applications, Microchip Technologies Inc
 * Created on November 19, 2015, 12:06 PM
 */

#include <xc.h>

// PIC16F18345 Configuration Bit Settings
// CONFIG1
#pragma config FEXTOSC = ECM     // EC (external clock) for 100 kHz to 8 MHz
#pragma config RSTOSC = EXT1X    // EXTOSC operating per FEXTOSC bits
#pragma config CLKOUTEN = ON     // FOSC/4 clock appears at OSC2
#pragma config CSWEN = ON        // Writing to NOSC and NDIV is allowed
#pragma config FCMEN = ON        // Fail-Safe Clock Monitor is enabled

// CONFIG2
#pragma config MCLRE = ON        // MCLR/VPP pin function is MCLR
#pragma config PWRTE = OFF       // PWRT disabled
#pragma config WDTE = OFF        // WDT disabled; SWDTEN is ignored
#pragma config LPBOREN = OFF     // ULPBOR disabled
#pragma config BOREN = ON        // Brown-out Reset enabled, SBOREN bit ignored
#pragma config BORV = LOW        // Brown-out voltage (Vbor) set to 2.45V
#pragma config PPS1WAY = OFF     // The PPS can be set and cleared repeatedly
#pragma config STVREN = ON       // Stack Overflow/Underflow will cause a Reset
#pragma config DEBUG = ON        // Background debugger enabled

// CONFIG3
#pragma config WRT = OFF         // Write protection off
#pragma config LVP = ON          // Low Voltage programming enabled

// CONFIG4
#pragma config CP = OFF          // User NVM code protection disabled
#pragma config CPD = OFF         // Data NVM code protection disabled

#define _XTAL_FREQ 4000000       // For __delay_ms() routine

main()
{
    __delay_ms(5000);            // delay 5s to see clock switch
    OSCFRQbits.HFFRQ = 0b0111;   // set to 32 MHz
    OSCCON1 = 0b01100000;        // set to HFINTOSC no divider
    while(!OSCCON3bits.NOSCR);   // wait until new oscillator ready

    while(1);                    // do nothing
}
```

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