VSC7420/1/2

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC7420/1/2 unmanaged switches. These checklist items should be followed when utilizing the VSC7420/1/2 in a new design. A summary of these items is provided in Section 8.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power/Ground"
- Section 4.0, "Interfaces"
- Section 5.0, "Miscellaneous Signals"
- Section 6.0, "Port Configuration"
- Section 7.0, "Internal Copper PHY Ports"

2.0 GENERAL CONSIDERATIONS

The switches in this family can be summarized in Table 2-1.

TABLE 2-1: UNMANAGED FAMILY

SparX-III Unmanaged Switches		Max	Port Breakdown			
Device	**Mode**	**Ports**	**#1G Copper**	**#1G SGMII**	**#2.5G SGMII**	**#QSGMII**
VSC7420	1	10	8	0	2(E0+E1)	0
VSC7421	0	17	12	0	1(E0)	1(E3)
	1		12	2(E2+E3)	2(E0+E1)	0
VSC7422	0	26	12	0	1(E0)	3(E1+E2+E3)

Note 1: E0-E3 are the Enhanced SerDes macros capable of running up to 6 GHz.

2: QSGMII is enabled in SW_MODE 0 and SGMII in SW_MODE 1. E0 is always 2.5G SGMII, E1-E3 are changeable between either QSGMII and SGMII mode.

2.1 Required References

The VSC7420/1/2 implementor should have the following documents on hand:

- *VSC7420-02_VSC7421-02_VSC7422-02 Data Sheet*
- *Section 15 Design Considerations* in the data sheet (in lieu of an errata document)
- VSC5609EV Reference Design Files (Using VSC7422)
- *ENT-AN1263-4.5 - Application Note - Flash Configuration Design Guide - VPPD-04628*
- *ENT-AN1015-1.0 - Application Note - Using the SparX-III Serial GPIO/LED Controller*
- *SparX-III Switch Pinout Comparisons*

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Strapping Pins

- The pin **VCORE_CFG[2.0]** control the Booting modes of the switch. See Table 2-2.

TABLE 2-2: VCORE-III CONFIGURATION STRAPPING PINS

VCore_CFG[*n*]			Behavior
***n* = 2**	***n* = 1**	***n* = 0**	
Don't Care	Don't Care	0	The 8051 is enabled and boots up from NOR Flash on the SI interface.
	Don't Care	1	Automatic boot is disabled by forcing the 8051 into Reset. SI Client mode is enabled for register access to the Switch core. The 8051 can be manually started from internal RAM (manually loaded with code through SI).

- The VCore-Ie MCU (8051) can automatically boot up and then hand over ownership of the SI to an external CPU (after it boots up from SI Flash).
- The device reference clock can be a 25 MHz, 125 MHz, or 156.25 MHz clock signal. It can be either a differential reference clock or a single-ended clock. However, 25 MHz single-ended operation is not recommended when using QSGMII due to the jitter specification requirements of this interface.
- The reference clock speed is selected by the RefClk_Sel[2:0] pins. See Table 2-3.

TABLE 2-3: REFERENCE CLOCK SPEED

Name	Pin Coding	RefClk_Sel2	RefClk_Sel1	RefClk_Sel0
RefClk_Sel[2:0]	000 = 125 MHz (default)	Pull down or Float	Pull down or Float	Pull down or Float
	001 = 156.25 MHz	Pull down or Float	Pull down or Float	Pull up to VDDIO
	100 = 25 MHz	Pull up to VDDIO	Pull down or Float	Pull down or Float
	All other values are reserved.			

- The reference clock can be either a differential reference clock or a single-ended clock. Refer to the data sheet for the device requirements for maximum clock jitter, which must be accounted for in board design when selecting clock source (oscillator) and clock distribution (buffer) components. For details on using a single-ended reference clock, see *Section 14.3.1 Single-Ended RefClk Input* in the data sheet.
- The reference clock is sourcing an internal 5 GHz PLL, which provides various clock outputs to the Switch core, MCU, and SerDes macros.

3.0 POWER/GROUND

3.1 Power Supplies

The VSC7420/1/2 requires power at:

- 1.0V power supply voltage for core **(VDD)**
- 1.0V power supply voltage for analog circuits **(VDD_A)**
- 1.0V power supply voltage for analog circuits for twisted pair interface **(VDD_AL)**
- 2.5V power supply voltage for analog driver in twisted pair interface **(VDD_AH)**
- 2.5V power supply for MII Management interface, parallel CPU interface, and misc. I/Os **(VDD_IO)**

Note:	The 2V5 IO supply must be within -1% to +4% to meet the minimum high-level input signal on 3V3 sourced devices, such as the JTAG and SPI.

- 1.0V or 1.2V power supply for Enhanced SerDes interfaces **(VDD_VS)**

Note:	When doing a SerDes backplane 1.2V is recommended. For SGMII and QSGMII between Switch and PHY located on the same board 1.0V is sufficient.

3.2 Power Supply Decoupling

- Each power supply voltage should have both bulk and high-frequency decoupling capacitors. Recommended bulk decoupling capacitors are 10 µF, but 47 µF should be used for **VDD_A** due to initial load during power-up. High-frequency decoupling capacitors that are 0.1 µF are also recommended.
- Surface mount decoupling capacitors should be placed as close to the power supply pins as possible. Smaller form factor components are best (i.e., 0402 is better than 0603).
- Analog supplies are recommended to be isolated from the digital supplies using ferrite beads for better performance.

3.3 Ground

- Make at least one unbroken ground plane **(GND)**.
- Use the power and ground plane combination as an effective power supply bypass capacitor. The capacitance is proportional to the area of the two planes and inversely proportional to the separation between the planes. Typical values with a 0.25 mm (0.01 inch) separation are 100 pF/in2. This capacitance is more effective than a capacitor of equivalent value because the planes have no inductance or Equivalent Series Resistance (ESR).
- Do not cut up the power or ground planes to steer current paths. This usually produces more noise, not less. Furthermore, place vias and clearances in a configuration that maintains the integrity of the plane. Groups of vias spaced close together often overlap clearances. This can form a large slot in the plane. As a result, return currents are forced around the slot, which increases the loop area and EMI emissions. Signals should never be placed on a ground plane because the resulting slot forces return currents around the slot.
- Vias connecting power planes to the supply and ground balls must be at least 0.25 mm (0.010 inch) in diameter, preferably with no thermal relief and plated closed with copper or solder. Use separate (or even multiple) vias for each supply and ground ball.
- A chassis ground is necessary for the RJ45 connector for better EMI and ESD.

3.4 Power Supply Sequencing

- During power-on and power-off, **VDD_A** and **VDD_VS** must never be more than 300 mV above **VDD**.
- **VDD_VS** must be powered even if the associated interfaces are not used. These power supplies must not remain at ground or be left floating.
- There is no sequencing requirements for **VDD_IO**.

4.0 INTERFACES

4.1 General Recommendations

High-speed signals require excellent frequency and phase response up to the third harmonic. The best designs provide excellent frequency and phase response up to the seventh harmonic. The following recommendations can improve signal quality and minimize transmission distances:

- Keep traces as short as possible. Initial component placement should be extremely carefully considered.
- The impedance of the traces must match the impedance of the termination resistors, connectors, and cable. This reduces reflections due to impedance mismatches.
- Differential impedance must be maintained in a 100Ω differential application. Routing two 50Ω traces is not adequate. The two traces must be separated by enough distance to maintain differential impedance. When routing differential pairs, keep the two trace lengths identical. Differences in trace lengths translate directly into signal skew. Note that the differential impedance may be affected when separations occur.
- Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities. In other words, avoid using vias.
- Do not group all the passive components together. The pads of the components add capacitance to the traces. At the frequencies encountered, this can result in unwanted reductions in impedance. Use surface-mounted 0603 (or smaller) components to reduce this effect.
- Eliminate or reduce stub lengths.
- Reduce, if not eliminate, vias to minimize impedance discontinuities. Remember that vias and their clearance holes in the power/ground planes can cause impedance discontinuities in nearby signals. Keep vias away from other traces.
- Keep signal traces away from other signals that might capacitively couple noise into the signals. A good rule of thumb is to keep the traces apart by ten times the width of the trace.
- Do not route digital signals from other circuits across the area of the high-speed transmitter and receiver signals.
- The use of grounded guard traces is typically not effective for improving signal quality. A ground plane is more effective. However, a common use of guard traces is to route them during the layout but remove them prior to design completion. This has the benefit of enforcing keep-out areas around sensitive high-speed signals, so that vias and other traces are not accidentally placed incorrectly.
- When signals in a differential pair are mismatched, the result is a Common-mode current. In a well-designed system, Common-mode currents should make up less than one percent of the total differential currents. Mode currents represent a primary source of EMI emissions. To reduce Common-mode currents, route differential traces so that their lengths are the same. For example, a 5 mm (0.2 inch) length mismatch between differential signals having the rise and fall times of 200 ps results in the Common-mode current being up to 18% of the differential current.

Note:	Due to the high application frequency, proper care must be taken when choosing components (such as the termination resistors) in the designing of the layout of a printed circuit board. The use of surface-mount components is highly recommended to minimize parasitic inductance and lead length of the termination resistor.

- Matching the impedance of the PCB traces, connectors, and balanced interconnect media is also highly recommended. Impedance variations along the entire interconnect path must be minimized because these degrade the signal path and may cause reflections of the signal.

4.2 Serial CPU Interface

- If the serial CPU interface is not used, all input signals can be left floating.
- The Serial Interface (SI) bus consists of the SI_Clk clock signal, the SI_DO and SI_DI data signals, and the SI_nCS0 device select signal.
- When routing the SI_Clk signal, be sure to create clean edges. If the SI bus is connected to more than one client devices, route it in a daisy-chain configuration with no stubs. Terminate the SI_Clk signal properly to avoid reflections and double clocking.
- If it is not possible (or desirable) to route the bus in a daisy-chain configuration, the SI_Clk signal should be buffered and routed in a star topology from the buffers. Each buffered clock should be terminated at its source.
- The SI tri-states the SI_Clk and SI_DO signals prior to deasserting the SI_nCS0 signal. This makes it possible to implement CPOL/CPHA as 0/0 or 1/1, if the attached SI devices require it, using termination resistors. If the attached devices support both types of CPOL/CPHA, SI_Clk and SI_DO must still have pull resistors to one of the I/O supply rails to prevent spurious clocks being seen when the signals are tri-stated.

4.3 NOR Flash

- NOR Flash is needed if booting from serial FLASH is enabled for the internal CPU. See *ENT-AN1263-4.5 - Application Note - Flash Configuration Design Guide - VPPD-04628* for Flash configurations.
- The VSC7420/1/2 is a 2.5V I/O device. VOH from this device might not meet requirement by the 3.3V NOR Flash at worst cases. A lower voltage supply (for example 2.8V) for the NOR Flash is recommended. Another suggestion is using a buffer with voltage translation on the SPI interface between switch and the NOR Flash.
- If doing on-board Flash programming, remember to be able to control Switch Reset from the programming header. Otherwise, the active Switch will also drive the SPI interface, when being in Boot mode 000 (SPI boot).

4.4 SGMII and QSGMII Interfaces

The SGMII and QSGMII interfaces (1 Gbps) consist of a **Tx** and **Rx** differential pair operating at 1250 Mbps or 5 Gbps.

- **Tx** output signals in a pair should have matched electrical lengths.
- **Rx** input signals in a pair should have matched electrical lengths
- SerDes **Tx** and **Rx** pairs must be routed as 100Ω differential traces with ground plane as reference.(All input buffers have built-in 100Ω terminations.)
- Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities. In other words, avoid the use of vias wherever possible.
- AC-coupling of **Tx** and **Rx** may be needed, depending on the PHY. If AC-coupled, the inputs are self-biased.
- To reduce the crosstalk between pairs or other PCB lines, it is recommended that the spacing on each side of the pair be larger than four times the track width.

4.5 Enhanced SerDes Interface

- The Enhanced SerDes interface can be used for fiber connections, backplanes, or direct coupler cable connections, such as the DAC cable. The Enhanced SerDes interface can operate in several modes. The physical signal bit rate is between 125 Mbps to 6.25 Gbps.
- The inputs are self-biased and require external AC-coupling. It is recommended to use small form factor components, such as 0603. The small form factor minimizes impedance mismatches by the AC-coupling capacitors because the size of the form factor approximately matches the trace width commonly used for these signals.
- If SFP MSA-defined signals such as TXFault, TXDisable, RXLos, ModuleDetect, and RateSelect are supported through the Serial GPIO interface then ensure that all signals have pull-ups. Likewise, an individual (selectable) I2C clock should be routed to each module slot or cage.
- The Enhanced SerDes interface can be directly connected to either 1 Gbps or 2.5 Gbps SFP modules. For these applications, external AC-coupling capacitors are not required because the SFP module already includes capacitors.

Table 4-1 lists the AC-coupling requirements for common Enhanced SerDes connections.

TABLE 4-1: ENHANCED SERDES INTERFACE COUPLING REQUIREMENTS

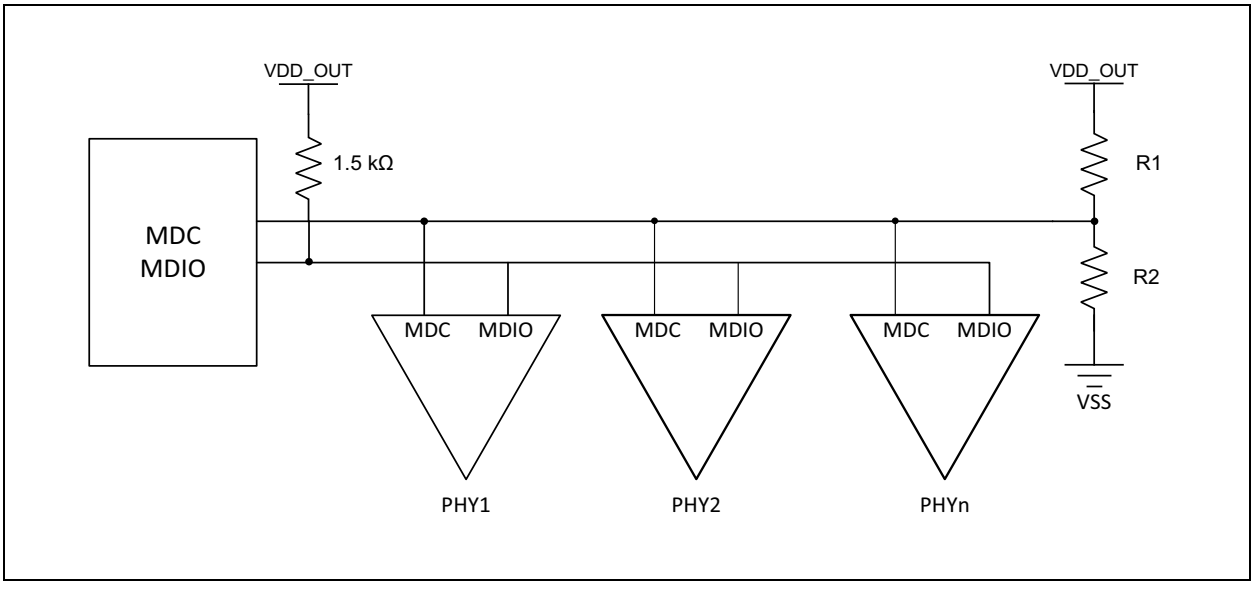
Enhanced SerDes Connection	Mode	External AC-Coupling Requirement
SFP modules	SFP	Not required
SGMII PHY	SGMII	Required
Enhanced SerDes device	Enhanced SerDes	Required

- The Enhanced SerDes interface signals must be routed as a differential pair, with a 100Ω differential characteristic impedance. The differential intra-pair skew must be below 5 ps in the PCB trace.
- To minimize crosstalk between transmitter and receiver, equal drive strength is recommended in both devices in a link.
- To minimize crosstalk between differential pairs, the characteristic differential impedance of the signals must be determined only by the distance to the reference plane and the intra-pair coupling and not the distance to the neighboring traces. To separate the transmitter and receiver signals to minimize crosstalk, it is recommended to route the transmitter and receiver signals on as many different PCB layers as feasible.

4.6 Media-Independent Interface Management (MIIM)

- Also known as the Serial Management Interface (SMI), there are two MIIM controllers – one for internal PHYs and one for external PHYs. The external MIIM controller controls external PHYs via two pins, MDC(MIIM clock) and MDIO (MIIM data input/output).
- External PHYs are attached to the switch using SerDes ports. These PHYs are controlled via a single MIIM control bus. The MIIM controller uses PHY addresses to select one of the external PHYs, so the PHY addresses must be configured differently for all the external PHYs on the external MIIM bus.
- Since MDIO is an open drain output, MDIO should be pulled high with the resistor around 1.5 KΩ. When connecting MDC/MDIO to multiple PHYs, the layout scheme in Figure 4-1 with end termination is recommended.

FIGURE 4-1: CONNECTING THE EXTERNAL MDC/MDIO TO MULTIPLE PHYS



4.7 2-Wire Serial Interface

- The 2-wire serial interface is capable of suppressing small amplitude glitches less than 5 ns in duration, which is less than the 50 ns duration often quoted for similar interfaces. Because the 2-wire serial implementation uses Schmitt-triggered inputs, the VSC7420-02, VSC7421-02, and VSC7422-02 devices have a greater tolerance to low amplitude noise.
- For glitch-free operation, select the proper pull-up resistor value to ensure that the transition time through the input switching region is less than 5 ns given the line's total capacitive load. For capacitive loads up to 40 pF, a pull-up resistor of 510Ω or less ensures glitch-free operation for noise levels up to 700 mV peak-to-peak.

5.0 MISCELLANEOUS SIGNALS

5.1 GPIO Pins

The devices include a GPIO interface with 12 individually configurable pins. Through the GPIOs, various interfaces are supported by the devices:

- 2-wire serial interface (two GPIO pins)
- UART (two GPIO pins)
- External interrupt (one interrupt pin)
- Serial GPIO (SGPIO) and LED interface (four GPIO pins)
- Fan controller with speed input and pulse-width-modulated output (two GPIO pins)

The Serial GPIO and LED interface can be used specifically for driving external LEDs for the internal and external copper PHYs or for serializing external interrupts. As an example, link down events from external PHYs before being input to the devices.

The Overlaid Function of a GPIO pin *N* is enabled by setting GPIO_ALT[1:0][*N*] = 01b and disabled by clearing the field. See Table 5-1.

TABLE 5-1: OVERLAID GPIO FUNCTIONS

Name	Overlaid Function 1
GPIO_0	SIO_CLK
GPIO_1	SIO_LD
GPIO_2	SIO_DO
GPIO_3	SIO_DI
GPIO_4	TACHO
GPIO_5	TWI_SCL
GPIO_6	TWI_SDA
GPIO_7	PTP
GPIO_8	EXT_IRQ0
GPIO_29	PWM
GPIO_30	UART_TX
GPIO_31	UART_RX

5.2 Serial GPIO Controller

- The VSC7420-02, VSC7421-02, and VSC7422-02 devices feature a serial GPIO controller (SIO). By using a serial interface, the SIO controller significantly extends the number of available GPIOs with a minimum number of additional pins on the device. The main purpose of the SIO controller is to connect control signals from SFP modules. However, it can also act as an LED controller.
- The SIO controller supports up to 128 serial GPIOs (SGPIOs) organized into 32 ports, with four SGPIOs per port. For more information, see *ENT-AN1015-1.0 - Application Note – Using the SparXIII Serial GPIO/LED Controller.*

5.3 System Resets

5.3.1 NRESET

- This pin provides a global device Reset when low. On power-up, it is driven high when the clock and all power rails have stabilized. Refer to the data sheet for minimum required delays between clock and power rails and **nReset** going high.
- Note that the internal 5 GHz PLL ramps up at power-up and is not controlled by any Reset signal. This allows all internal clocking to be running once HW Reset is released.

5.3.2 JTAG_NTRST

- The JTAG_nTRST signal is asynchronous to the clock and does not have setup or hold time requirements. It must be held low untill all power supply voltages have stabilized and reached recommended values. For normal device operations, i.e., when the JTAG interface is not in use, JTAG_nTRST should be pulled low. Note that the JTAG interface does not have access to the 8051 MCU. Therefore, ICE debugging is not possible.

Note:	All JTAG signals are **not** 5V tolerant.

5.4 Interrupt Pins

- An interrupt pin (EXT_IRQ as Overlaid Function One of GPIO_8) serves as an input or output to the internal VCore-Ie CPU system or to an external processor. Signal polarity is programmable.

5.5 Coma Mode

- The **COMA_MODE** pin provides an optional feature that may be used to control when PHY become active. It is an output for the Switch and an input to the PHY. It is used to synchronize the operation of multiple PHYs (internal and external) on the same PCB.
- The typical usage is to keep the PHYs from becoming active before they have been fully initialized. Alternatively, the **COMA_MODE** pin may be connected low (ground) by a pull-down resistor and the PHYs will be fully active once out of Reset. When this pin is asserted high, all PHYs are held in a powered down state. When deasserted low, all PHYs are powered up and resume normal operation. This can be used to synchronize the operation of multiple PHYs on the same board to provide visual synchronization for LEDs by separate PHYs.

5.6 Reserved Pins

TABLE 5-2: VSC7420XJQ-02 (302 PIN TQFP) PINS

Reserved Pins	Description
Reserved_[5:8], Reserved_29	These reserved pins should be tied to VDD_IO.
Reserved_4	These reserved pins should be tied to VSS.
Reserved_[10:15], Reserved_[17:18], Reserved_[22:24], Reserved_[50:81], Reserved_[124:127], Reserved_[136:139]	These reserved pins should be left floating (no connect).

TABLE 5-3: VSC7420XJG-02 (672 PIN BGA) PINS

Reserved Pins	Description
Reserved_[5:8], Reserved_29	These reserved pins should be tied to VDD_IO.
Reserved_4	These reserved pins should be tied to VSS.

TABLE 5-3: VSC7420XJG-02 (672 PIN BGA) PINS (CONTINUED)

Reserved Pins	Description
Reserved_[10:25], Reserved_[17:24], Reserved_[31:41], Reserved_[50:81], Reserved_[98:99], Reserved_[104:111], Reserved_[116:148], Reserved_[150:184], Reserved_[186:192], Reserved_[201:209], Reserved_[211:221], Reserved_223, Reserved_225, Reserved_[232:237], Reserved_[240:248]	These reserved pins should be left floating (no connect).

TABLE 5-4: VSC7421XJQ-02 (302 PIN TQFP) PINS

Reserved Pins	Description
Reserved_[6:8], Reserved_29,	These reserved pins should be tied to VDD_IO.
Reserved_[4:5],	These reserved pins should be tied to VSS.
Reserved_[10:15], Reserved_[17:18], Reserved_[22:24]	These reserved pins should be left floating (no connect).

TABLE 5-5: VSC7421XJG-02 (672 PIN BGA) PINS

Reserved Pins	Description
Reserved_[6:8], Reserved_29	These reserved pins should be tied to VDD_IO.
Reserved_[4:5]	These reserved pins should be tied to VSS.
Reserved_[10:15], Reserved_[17:24], Reserved_[31:41], Reserved_[98:99], Reserved_[104:111], Reserved_[116:123], Reserved_[128:135], Reserved_[140:148], Reserved_[150:184], Reserved_[186:192], Reserved_[201:209], Reserved_[211:221], Reserved_223, Reserved_225, Reserved_[232:237], Reserved_[240:248]	These reserved pins should be left floating (no connect).

TABLE 5-6: VSC7422XJQ-02 (302 PIN TQFP) PINS

Reserved Pins	Description
Reserved_5, Reserved_[7:8], Reserved_29	These reserved pins should be tied to VDD_IO.
Reserved_4, Reserved_6	These reserved pins should be tied to VSS.
Reserved_[10:24], Reserved_[31:41], Reserved_[98:99], Reserved_[104:111], Reserved_[116:123], Reserved_[128:135], Reserved_[140:148], Reserved_[150:184], Reserved_[186:192], Reserved_[201:209], Reserved_[211:221], Reserved_223, Reserved_225, Reserved_[232:237], Reserved_[240:248]	These reserved pins should be left floating (no connect).

TABLE 5-7: VSC7422XJG-02 (672 PIN BGA) PINS

Reserved Pins	Description
Reserved_5, Reserved_[7:8], Reserved_29	These reserved pins should be tied to VDD_IO.
Reserved_4, Reserved_6	These reserved pins should be tied to VSS.
Reserved_[10:15]	These reserved pins should be left floating (no connect).

5.7 Analog Bias Signals

Refer to the following information for the analog bias signals:

- **Analog Bias Calibration –** Connect SerDes_Rext1 and SerDes_Rext0 with a 620Ω ±1% resistor.
- **Reference Filters:** Ref_filt_[2:0] **–** Connect a 1.0 µF external capacitor between each pin and ground.
- **Reference External Resistors:** Ref_rext_[2:0] **–** Connect a 2.0 kΩ (1%) resistor between each pin and ground.

6.0 PORT CONFIGURATION

The VSC7420-02 runs in Switch mode 1. The VSC7421-02 can be used in two different port configurations: Switch mode 0 or Switch mode 1. VSC7422-02 devices run in Switch mode 0. The Switch mode is controlled through the register DEVCPU_GCB::MISC_CFG.SW_MODE. See *Section 6.1 Port Mapping* in the data sheet.

7.0 INTERNAL COPPER PHY PORTS

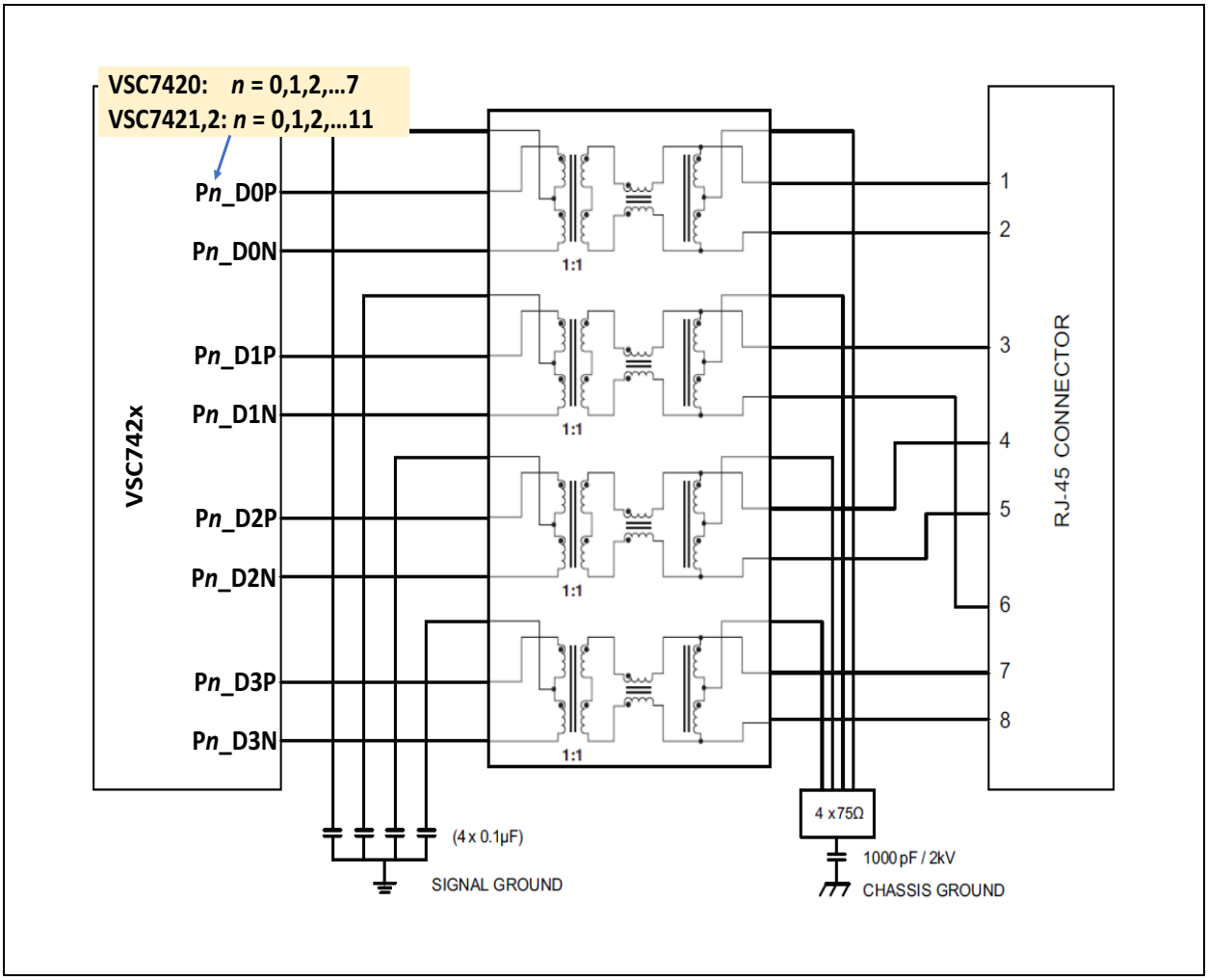
Eight internal copper Gigabit (GbE) PHYs are available on the VSC7420. Twelve internal copper Gigabit (GbE) PHYs are available on the VSC7421/2. More external PHYs can be supported on the QSGMII interface or SGMII interfaces.

7.1 Copper PHY MDI Interface

Figure 7-1 shows the recommended connection from the internal copper PHY to the transformer. The internal copper PHY uses voltage-mode line driver technology, so no center tap voltage is required at the transformer. Each of the four center taps is recommended to be connected to GND through a separate 0.1 µF capacitor because the Common-mode voltage on each pair might be different.

Note:	The PHY has integrated termination resistors, so no external terminations are needed. It is recommended to use a minimum of 8-core magnetics with a Common-mode choke (CMC) at the RJ45/cable side.

FIGURE 7-1: TRANSFORMER CONNECTIONS FOR INTERNAL COPPER PHY PORTS



The MDI interface is organized into four differential pairs (D0, D1, D2, and D3) for each PHY port. Pairs D2 and D3 are only used in Gigabit speed. When routing these pairs on a PCB, the characteristics must match one of the following:

- Route each single-ended trace with a characteristic impedance of 50Ω referenced to ground.
- Route each positive and negative trace on each port as differential pairs with 100Ω characteristic differential impedance.

8.0 HARDWARE CHECKLIST SUMMARY

TABLE 8-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet, and the reference design's use of GPIO is retained as much as possible to minimize software efforts.		
	Section 2.3, "Strapping Pins"	**Vcore_CFG[2:0]** configured to match design's Boot mode.		
		RefClk_Sel[2:0] appropriate for input reference clock speed.		
		25 MHz single-ended reference clock not recommended when using QSGMII.		
		Single-ended reference clock design should follow *Section 14.2.1* in data sheet.		
		Verify if clock jitter will meets data sheet requirements.		
Section 3.0, "Power/Ground"	Section 3.1, "Power Supplies"	The 2V5 IO supply must be within -1%/+4% to meet the minimum high level input signal on 3V3 sourced devices, such as the JTAG and SPI.		
		When doing a SerDes backplane 1.2V is recommended. For SGMII and QSGMII between Switch and PHY located on the same board, 1.0V is sufficient.		
	Section 3.2, "Power Supply Decoupling"	Each power rail should have bulk and high-frequency decoupling capacitors. High-frequency capacitors should be close to the power pin as possible.		
		Analog supplies should be isolated from digital supplies through ferrite beads.		
	Section 3.3, "Ground"	Design in at least on unbroken ground plan. Other recommendations are followed.		
	Section 3.4, "Power Supply Sequencing"	Check if the power sequencing is correct.		
Section 4.0, "Interfaces"	Section 4.1, "General Recommendations"	Recommendations to improve signal quality and minimize transmission distances are followed.		
	Section 4.2, "Serial CPU Interface"	If CPU interface is not used, pins can be left floating (no connect). Recommendations are followed.		
	Section 4.3, "NOR Flash"	Recommendations regarding buffering 3.3V NOR Flash to 2.5 V I/O are followed.		

TABLE 8-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
	Section 4.4, "SGMII and QSGMII Interfaces"	**Tx** and **Rx** differential pairs should have matched electrical cable lengths.		
		Pairs should be routed as 100Ω differential traces with ground plane as reference.		
		Check if PHY needs AC-coupling.		
		Spacing recommendations to reduce crosstalk are followed.		
	Section 4.5, "Enhanced SerDes Interface"	Recommendations are followed.		
	Section 4.6, "Media-Independent Interface Management (MIIM)"	Recommendations are followed.		
	Section FIGURE 4-1:, "Connecting the External MDC/MDIO to Multiple PHYs"	Recommendations are followed.		
Section 5.0, "Miscellaneous Signals"	Section 5.1, "GPIO Pins"	Use GPIO_ALT[1:0][31:1] to configure pin functions. Pins defaulting to GPIO should have GPIO_ALT[1.0][N] = 00b. In general, check for 2V5 level. All GPIO pins have internal pullup. Pins are 3.3V tolerant. All PHY LEDS are active-low and must have a resistor value of 100Ω to 300Ω in series. If LED is unused, it should left as NC.		
	Section 5.2, "Serial GPIO Controller"	Recommendations in the *ENT-AN1015-1.0 - Application Note - Using the SparX-III Serial GPIO/LED Controller* are followed.		
	Section 5.3.1, "nRESET"	Verify if **nReset** is held low until clock and all power rails have stabilized. Follow timing specifications in data sheet.		
	Section 5.3.2, "JTAG_nTRST"	No JTAG signals are 5 V tolerant. For normal operation, **JTAG_nTRST** should be pulled low.		
	Section 5.4, "Interrupt Pins"	Connect interrupt pins to supervisor. Depending on the polarity, remember to pull resistors on interrupt signal.		
	Section 5.5, "Coma Mode"	Make sure that the use of pin is compatible with overall system design.		
	Section 5.6, "Reserved Pins"	Verify that pins are correctly terminated, either to **VDD_IO, VSS** or are left floating.		
	Section 5.7, "Analog Bias Signals"	Recommendations are followed.		
Section 6.0, "Port Configuration"		Port assignments vary by device. See *Section 6.1 Port Mapping* in the data sheet.		
Section 7.0, "Internal Copper PHY Ports"	Section 7.1, "Copper PHY MDI Interface"	Verify pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable.		
		Verify 10/100BT mode of operation is supported on D0/D1.		
		Verify auto crossover only between A/B and C/D.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00005256A (01-23-24)	Initial release	

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