TB3195

Managing Cache Coherency on Cortex-M7 Based MCUs

Introduction

This document provides an overview of the cache coherency issue under different scenarios. It also suggests methods to manage or avoid the cache coherency issue.

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1. Cache Policies Overview

Table 1-1. Cache Policies

Read Policy (Cache miss case):	
Read Allocate	All cacheable locations on Cortex-M7 based MCUs are read allocate. This means that the data cache lines are allocated when a cache miss occurs, bringing 32 bytes (See **Note**) of data from the main memory into the cache memory. As a result, subsequent access to these memory locations will result in a cache hit condition, and the data is directly read from the cache memory.
Write Policy (Cache hit case):	
Write Back	On a cache hit, only the data cache is updated and not the main memory. The cache line is marked as dirty, and writes to the main memory are postponed until the cache line is evicted, or explicitly cleaned.
Write Through	On a cache hit, both the data cache and the main memory are updated.
Write Policy (Cache miss case):	
Write Allocate	On a cache miss, a cache line is allocated and loaded with the data from the main memory. This means that executing a store instruction on the processor might cause a burst read to occur to bring the data from the main memory to cache.
No Write Allocate	On a cache miss, a cache line is not allocated and the data is written directly into the main memory. Here, a line is not cached until a cache miss on a read occurs, which then loads the cache using the Read Allocate policy.

Note: The size of a cache line on Cortex-M7 MCUs is 32 bytes.

2. Supported Configurations

Write-back with read and write allocate: WB-RWA

- Provides the best performance. The cache hits only update the cache memory. Cache misses on a write, copy data from the main memory to the cache. As a result, subsequent access results in a cache hit.

Write-back with read allocate (no write allocate): WB-NWA

- The cache hits only update the cache memory. Cache misses on a write do not bring the data to the cache. This is advantageous only when the data is written, but not immediately read back.

Write-through with read allocate (no write allocate): WT-NWA

- Each write (either cache hit, or cache miss) is performed on the main memory. This negates the main advantage of having cache.
- Partially solves the cache coherency issue.

Non-cacheable

- Each read and write is performed on the main memory.
- No cache coherency related issues.

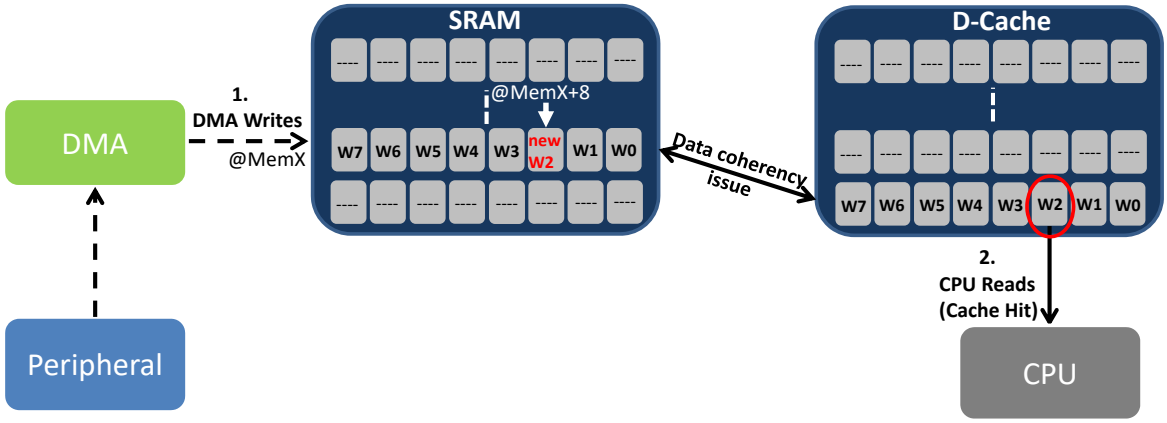
3. Cache Coherency Issues

A memory region is said to be coherent when multiple bus masters, for example, CPU and DMA have the same view of the memory shared between them.

Consider an application where the DMA writes to the SRAM.

Conditions: Cache is enabled on SRAM and the cacheability attribute is set to write-back with read and write-allocate (WB-RWA). The CPU has previously read the DMA buffer and therefore, the same is available in the cache memory due to the read allocate policy.

Figure 3-1. Cache Coherency Issue - DMA Writes to SRAM



Where,

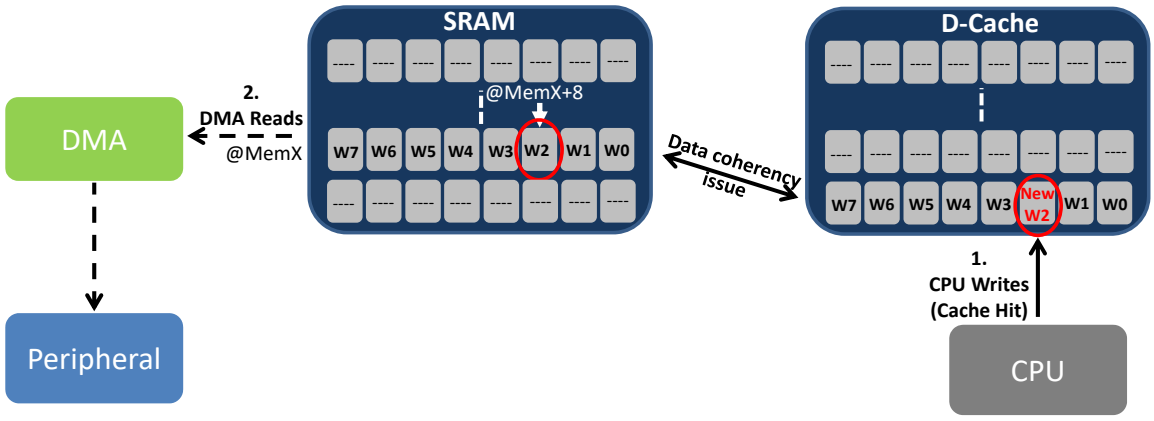
1. The DMA reads the data from the peripheral and updates the receive buffer in the SRAM.

2. When the CPU tries to read the receive buffer, it will read the data present in the cache and not the new data available in the SRAM.

Consider another example, where the DMA reads from the SRAM.

Conditions: The cache is enabled on the SRAM, and the cacheability attribute is set to WB-RWA.

Figure 3-2. Cache coherency Issue - DMA Reads from SRAM



Where,

1. The CPU updates the data to be transmitted in a transmit buffer as the cache policy is set to WB-RWA, only the cache is updated and not the main memory.

2. When the DMA reads the transmit buffer, it reads the old value present in the main memory and not the latest value updated by the CPU which is still in the cache.

4. Using Cache Maintenance APIs to Handle Cache Coherency

This solution requires the application to manage the cache at run-time using the Cortex-M7 cache maintenance operations. The cache maintenance APIs enable users to perform these actions:

1. Enable or disable cache – Cache on or off.

2. Invalidate cache – Marks the cache lines as invalid. Subsequent access forces the data to be copied from the main memory to the cache, due to the read-allocate and write-allocate policies.

3. Clean cache – Writes the cache lines, which are marked as dirty, back to the main memory.

The Cortex Microcontroller Software Interface Standard (CMSIS) provides the following D-Cache maintenance APIs:

Table 4-1. CMSIS Data Cache Maintenace APIs

Cache Maintenance API	Description
SCB_EnableDCache (void)	Enables data cache. Invalidates the entire data cache before enabling it.
SCB_DisableDCache (void)	Disables data cache. Cleans the data cache to flush dirty data to main memory before disabling the cache.
SCB_InvalidateDCache(void)	Invalidate the entire data cache.
SCB_InvalidateDCache_by_Addr (uint32_t * addr, int32_t dsize)	Invalidate the data cache line by address.
SCB_CleanDCache(void)	Cleans the data cache.
SCB_CleanDCache_by_Addr (uint32_t *addr, int32_t dsize)	Cleans the data cache line by address.
SCB_CleanInvalidateDCache(void)	Cleans and Invalidates the entire data cache.
SCB_CleanInvalidateDCache_by_Addr(uint32_t *addr, int32_t dsize)	Cleans and Invalidates the data cache line by address.

When using the cache clean and cache invalidate by address APIs:

addr – Must be aligned to the cache line size boundary. This means that the DMA buffer address must be aligned to the 32-byte boundary.

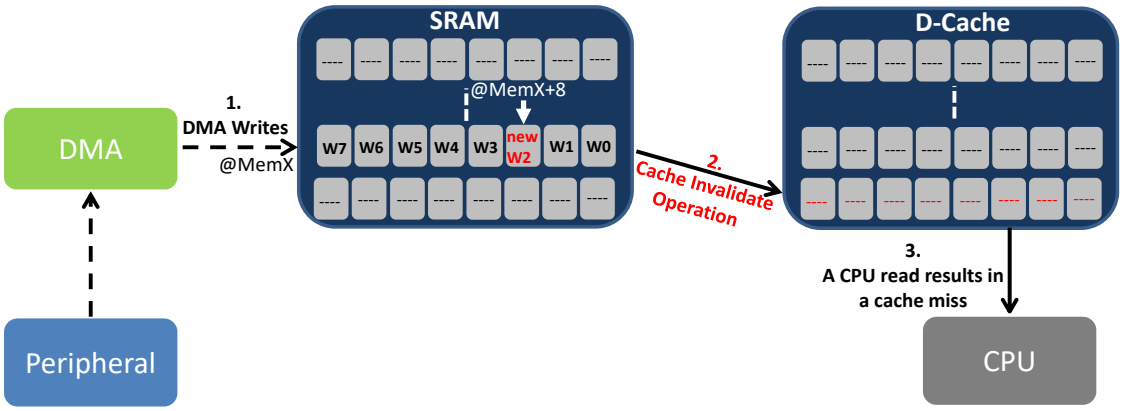
dsize – Must be a multiple of the cache line size. This means that the DMA buffer size must be a multiple of 32-bytes.

Using cache maintenance API when DMA writes to SRAM

Conditions: The cache policy is WB-RWA. The CPU initially accessed the receive buffer (rx_buffer[]), and cached it in the D-Cache.

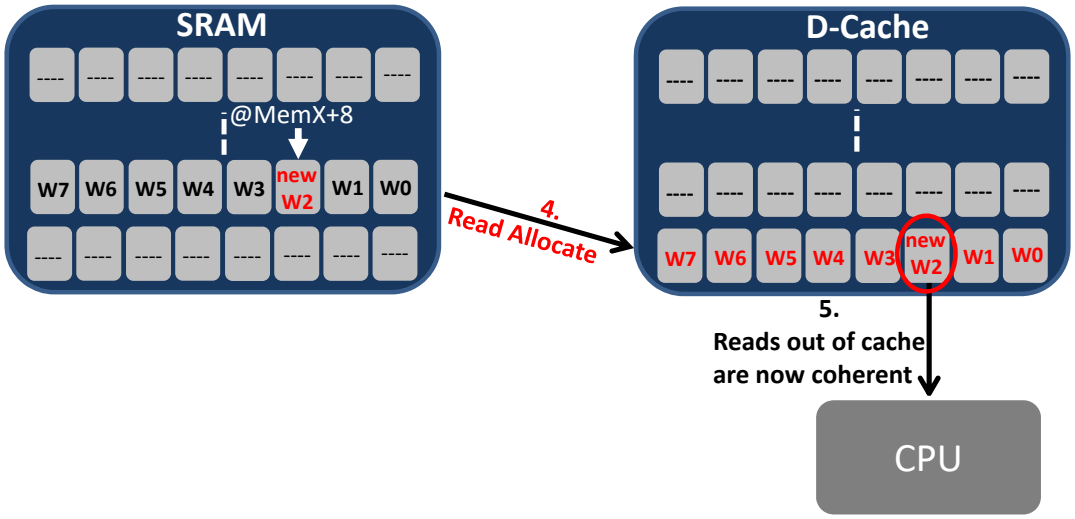
1. DMA writes data to the rx_buffer[].
2. A cache invalidate operation is performed to invalidate the cached rx_buffer[].
3. CPU tries to read the rx_buffer[] and results in a cache miss as rx_buffer[] was invalidated in step 2.

Figure 4-1. Cache Invalidate Operation After DMA Writes to SRAM



4. Due to the read-allocate policy, a cache line is allocated and copies data from the rx_buffer[] in the SRAM to the allocated cache line.
5. The CPU reads from the cache will then be coherent.

Figure 4-2. After a Cache Invalidate Operation, Reads Out of D-Cache by CPU are Coherent



The following code sample shows (using the GCC compiler) how to define the DMA buffers aligned to the cache line size boundary. The BUFFER_SIZE must be a multiple of the cache line size (32-bytes). The DMA_TRANSFER_SIZE is the number of bytes transferred by the DMA. Once the DMA read operation is complete, the receive buffer in cache is invalidated using the cache invalidate API. The main function enables the data cache, using the cache maintenance APIs.

Note: All the code samples provided in this tech brief refer to the API functions available under Microchip's Atmel Software Framework (ASF3).

Code Showing Cache Invalidate Operation After DMA Transfer is Complete

```
/* The rx_buffer is aligned to 32-byte boundary. The BUFFER_SIZE is a multiple of cache line
size (32-bytes)*/
#define BUFFER_SIZE         32

__attribute__ ((aligned (32))) uint8_t rx_buffer[BUFFER_SIZE];

volatile bool rx_xfer_done;
/**
 * \brief XDMAC interrupt handler.
 */
void XDMAC_Handler(void)
{
    uint32_t dma_status;

    dma_status = xdmac_channel_get_interrupt_status(XDMAC, XDMA_CH_RX);

    if (dma_status & XDMAC_CIS_BIS)
    {
        rx_xfer_done = true;
        SCB_InvalidateDCache_by_Addr((uint32_t*)rx_buffer, DMA_TRANSFER_SIZE);
    }
}
int main (void)
{
    ……
    /* Enabling the D-Cache */
    SCB_EnableDCache();
    /* Setup and trigger a DMA transfer */
    ……
    while (false == rx_xfer_done);
    /* Access to the rx_buffer[] is coherent now */
}
```

Using cache maintenance API when DMA reads from SRAM

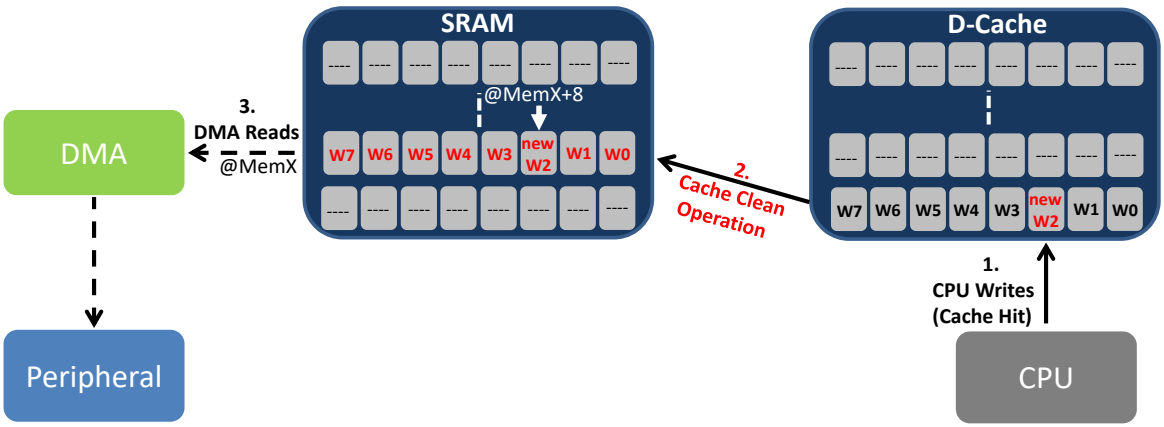
Conditions: The cache policy is set to WB-RWA. The CPU initially accessed the transmit buffer (tx_buffer[]), and cached it in the D-Cache.

1. The CPU writes data to the tx_buffer[] which will be transmitted by the DMA.

2. A cache clean operation is performed to flush the cached tx_buffer[] into the SRAM before enabling the DMA transfer.

3. The DMA reads from the SRAM will now be coherent.

Figure 4-3. Cache Clean Operation After CPU Writes to D-Cache



Code Showing A Cache Clean Operation after the CPU writes to D-Cache

```
int main (void)
{
     ……

    strcpy(tx_buffer, "DMA Transmit String");

    SCB_CleanDCache_by_Addr((uint32_t*)tx_buffer, DMA_TRANSFER_SIZE);

    xdmac_channel_enable(XDMAC, XDMA_CH_TX);
}
```

In the previous code sample, before enabling the DMA transfer, a cache clean operation by CPU writes the updated data in the transmit buffer to the SRAM.

Note: If the DMA link descriptors are used, then every time the descriptors are updated, the application must clean the cache corresponding to the link descriptor addresses to maintain coherency between the DMA and the CPU.

Important: All the cache operations are performed on a cache line of 32-bytes. As a result, if the size of the transmit and receive buffers in the above example are not a multiple of 32-bytes, a cache invalidate or cache clean operation could lead to unexpected behavior as shown in the following code sample.

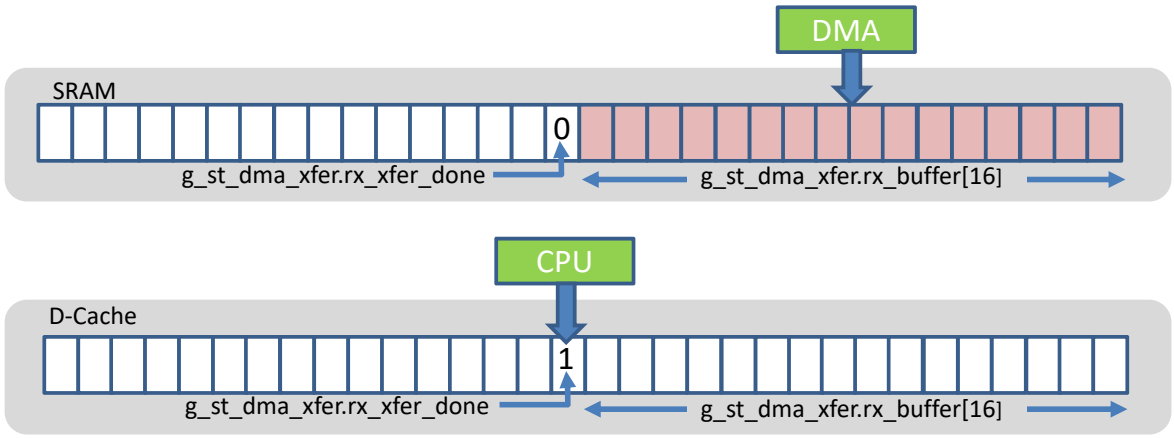
Code Illustrating the Effect of DMA Buffers That are Not a Multiple of 32-Bytes

```
#define BUFFER_SIZE        16

typedef struct
{
    /* The rx_buffer is aligned to 32-byte boundary.
       The BUFFER_SIZE is 16-bytes which is not a multiple of the cache line size.
    */
    __attribute__ ((aligned (32))) uint8_t rx_buffer[BUFFER_SIZE];

    bool rx_xfer_done;

}st_dma_xfer;

static st_dma_xfer g_st_dma_xfer;

/**
 * \brief XDMAC interrupt handler.
 */
void XDMAC_Handler(void)
{
    uint32_t dma_status;

    dma_status = xdmac_channel_get_interrupt_status(XDMAC, XDMA_CH_RX);

    if (dma_status & XDMAC_CIS_BIS)
    {
        g_st_dma_xfer.rx_xfer_done = true;
        SCB_InvalidateDCache_by_Addr((uint32_t*)g_st_dma_xfer.rx_buffer,
              DMA_TRANSFER_SIZE);
    }
}
```

In the previous code sample, the receive buffer is16 bytes. The DMA reads 16 bytes from the peripheral into the g_st_dma_xfer.rx_buffer[] in SRAM and generates a DMA interrupt. In the DMA ISR, the CPU sets the g_st_dma_xfer.rx_xfer_done flag to 1 in D-cache. This memory location was previously

accessed by the CPU and therefore it is available in the D-cache. A cache invalidate operation is then performed, thereby invalidating the cached line.

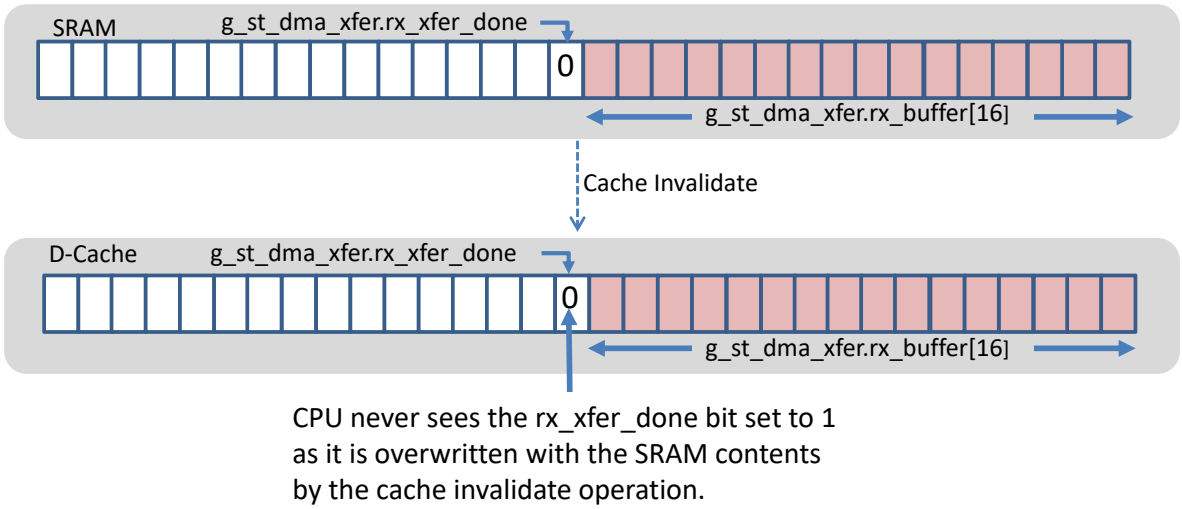
Figure 4-4. DMA Updates the Receive Buffer in SRAM and CPU Updates a Flag in D-Cache



Since the cache line is invalidated, access to the g_st_dma_xfer.rx_xfer_done flag by the CPU in the main function, result in the entire cache line of 32 bytes copied from the SRAM to the D-cache (due to the read allocate policy). This overwrites the g_st_dma_xfer.rx_xfer_done flag back to 0.

As a result, the CPU never sees the g_st_dma_xfer.rx_xfer_done flag set to 1.

Figure 4-5. A Cache Invalidate Operation Inadvertantly Corrupts Data Present in the Data Cache



This issue is caused as the DMA buffer is not a multiple of 32 bytes. Note that even if the DMA is configured to transfer a non-integer multiple of 32 bytes of data to/from a peripheral, the DMA buffer must be an integer multiple of 32 bytes to avoid corruption of variables defined in the same cache line. For example, if the DMA is configured to read/write 50 bytes to/from a peripheral then the DMA buffers must be of size 64.

5. Disabling Cache on Memory Regions Shared by the DMA and CPU

In this approach, the memory regions shared by the CPU and DMA are defined as non-cacheable using the Memory Protection Unit (MPU), while leaving the memory regions that are only accessed by the CPU as cacheable.

Use case: Shared memory can be updated by the CPU and DMA simultaneously. For example, the Ownership bit in the *GMAC receive buffer descriptor entry* can be updated simultaneously by the CPU and DMA.

Advantage: Transparent to the application. No cache maintenance is required. Porting a driver from a MCU without cache to a MCU with cache becomes easy.

Drawbacks: Requires the use of an MPU to create a dedicated non-cacheable memory region. This requires a complex linker script file.

Configuring the MPU to create a non-cacheable memory region:

Using the SAM Cortex-M7 MCUs users can create up to 16 MPU regions. The following table shows the MPU registers used to configure and enable a memory region. For detailed information, refer to the http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0646b/BIHJJABA.html

Table 5-1. MPU Registers

MPU Register	Description
MPU_RNR	Selects which memory region is referenced by the MPU_RBAR and MPU_RASR registers. Valid values range from 0-15 corresponding to the 16 MPU regions.
MPU_RBAR	Defines the base address of the MPU region. The region start address must align to the size of the region. (i.e., A 64KB region must be aligned on a multiple of 64KB, at 0x00010000 or 0x00020000).
MPU_RASR	Defines the region size and memory attributes of the MPU region and then enables that region. The smallest permitted region size is 32 bytes and must be a power of 2.
MPU_CTRL	Enables/Disables MPU

The TEX, C and B bits of the MPU_RASR register define the cacheability of the memory regions. The following table shows the encoding for the normal memory type.

Table 5-2. MPU Access Permission Attributes

TEX	C	B	Shareable	Memory Type	Description
000	1	0	Yes	Normal	Write-through, no write allocate
000	1	1	Yes	Normal	Write-back, no write allocate
001	0	0	Yes	Normal	Non-cacheable
001	1	1	Yes	Normal	Write-back, write and read allocate (Default cache policy on SAM Cortex-M7 MCUs when cache is enabled)

For detailed information, refer to the "section 4.6.6 MPU access permissions attributes", available on the ARM Information Center. For more details on configuring the MPU, refer to the TB3179 - How to Configure the Memory Protection Unit (MPU).

The following code example disables the MPU and then configures and enables a section of the SRAM memory region starting at 0x2045F0000 and of size 4096 bytes, as non-cacheable. Leaving the remaining SRAM memory region as cacheable with the default (WB-RWA) cache policy. The Access Permission (AP) is set to Full access which allows both privileged and non-privileged software to have RW access, and later it enables the MPU.

Code Showing MPU Configuration to Create a Non-Cacheable Memory Region

```
#define SRAM_NOCACHE_START_ADDRESS          (0x2045F000UL)
#define NOCACHE_SRAM_REGION_SIZE            0x1000
#define MPU_NOCACHE_SRAM_REGION             (11)
#define INNER_OUTER_NORMAL_NOCACHE_TYPE(x)  ((0x01 << MPU_RASR_TEX_Pos ) | ( DISABLE <<
MPU_RASR_C_Pos ) | ( DISABLE << MPU_RASR_B_Pos ) | ( x << MPU_RASR_S_Pos))

    /* Disable the MPU region */
    MPU->CTRL = MPU_DISABLE;
    dw_region_base_addr =
        SRAM_NOCACHE_START_ADDRESS |
        MPU_REGION_VALID |
        MPU_NOCACHE_SRAM_REGION;

    dw_region_attr =
        MPU_AP_FULL_ACCESS    |
        INNER_OUTER_NORMAL_NOCACHE_TYPE( SHAREABLE ) |
        mpu_cal_mpu_region_size(NOCACHE_SRAM_REGION_SIZE) |
        MPU_REGION_ENABLE;

    MPU->RBAR = dw_region_base_addr;
    MPU->RASR = dw_region_attr;

    /* Enable the MPU region */
    MPU->CTRL = (MPU_ENABLE | MPU_PRIVDEFENA);
    __DSB();
    __ISB();
```

The linker script file may be modified to define a non-cacheable memory space, and place the DMA buffers to be linked to the non-cacheable memory area as shown in the following code sample for GNU linker script.

Linker Script Modifications to Create Memory Sections for Non-Cacheable Data

```
/* Memory Spaces Definitions */
MEMORY
{
  rom (rx)  : ORIGIN = 0x00400000, LENGTH = 0x00200000
  ram (rwx) : ORIGIN = 0x20400000, LENGTH = 0x0005F000
  ram_nocache (rwx) : ORIGIN = 0x2045F000, LENGTH = 0x00001000
}
/* Section Definitions */
SECTIONS
{
    …….
        .ram_nocache (NOLOAD):
        {
        . = ALIGN(4);
        _s_ram_nocache = .;
        *(.ram_nocache)
        . = ALIGN(4);
        _e_ram_nocache = .;
           } > ram_nocache

    .ram_nocache_data : AT (_etext + SIZEOF(.relocate))
        {
        . = ALIGN(4);
        _s_ram_nocache_vma = .;
        _s_ram_nocache_lma = LOADADDR(.ram_nocache_data);
        *(.ram_nocache_data)
        . = ALIGN(4);
        _e_ram_nocache_vma = .;
        } > ram_nocache
```

```
    …….
}
```

The previous linker script example specifies the load memory address of the `.ram_nocache_data` section to be at the end of the `.text` and the `.relocate` sections.

Use the following code in the Reset Handler to zero the uninitialized variables defined under the `.ram_nocache` section, and to copy (from Flash to the SRAM) the initial values of initialized variables in `.ram_nocache_data`.

C Startup Code Modifications to Initialize the Memory Sections for Non-Cacheable Data

```
extern uint32_t _s_ram_nocache;
extern uint32_t _e_ram_nocache;
extern uint32_t _s_ram_nocache_vma;
extern uint32_t _e_ram_nocache_vma;
extern uint32_t _s_ram_nocache_lma;

void Reset_Handler(void)
{
    uint32_t *pSrc, *pDest;
    ……

    /* Initialize the no cache data segment */
    pSrc = &_s_ram_nocache_lma;
    pDest = &_s_ram_nocache_vma;

    if (pSrc != pDest) {
        for (; pDest < &_e_ram_nocache_vma;) {
            *pDest++ = *pSrc++;
        }
    }

    /* Clear the no cache zero segment */
    for (pDest = &_s_ram_nocache; pDest < &_e_ram_nocache;) {
        *pDest++ = 0;
    }
    ……
}
```

In the application, the DMA buffers can be allocated to the `.ram_nocache` memory region as shown in the following code sample. If the application has initialized variables in the no-cache memory region, then they must be defined to go under the `.ram_nocache_data` section.

Application Code to Define Buffers in Non-Cacheable Memory Section

```
__attribute__ ((section (".ram_nocache"), aligned (32))) uint8_t rx_buf[BUFFER_SIZE];
__attribute__ ((section (".ram_nocache"), aligned (32))) uint8_t tx_buf[BUFFER_SIZE];
```

Another way to avoid cache coherency is to use Tightly Coupled Memory (TCM) as the contents of TCM are not cached and can be accessed by both the CPU and the DMA. It can be accessed at similar speeds as accessing cache, without the penalty of a cache-miss and cache coherence issues.

Use case: Buffers with a size larger than the cache size (16 KB).

Advantages: No impact on performance. Transparent to the application (no cache maintenance required).

Drawbacks: Requires the linker script to be modified.

For more information on using TCM, refer to the links provided in the references section.

6. Relevant Resources

For additional information, refer to the following documents which are available for download from the following location:

1. ARM Cortex-M7 Processor Technical Reference Manual – L1 caches
2. ARM Cortex-M7 Processor Technical Reference Manual – Memory Protection Unit
3. http://ww1.microchip.com/downloads/en/AppNotes/Atmel-44047-Cortex-M7-Microcontroller-Optimize-Usage-SAM-V71-V70-E70-S70-Architecture_Application-note.pdf
4. How to Configure the Memory Protection Unit (MPU)
5. Atmel SMART SAM V7x TCM Memory
6. Atmel SMART SAM E70 TCM Memory

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ISBN: 978-1-5224-2966-1

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