

KSZ8895/KSZ8864 Silicon Errata and Data Sheet Clarification

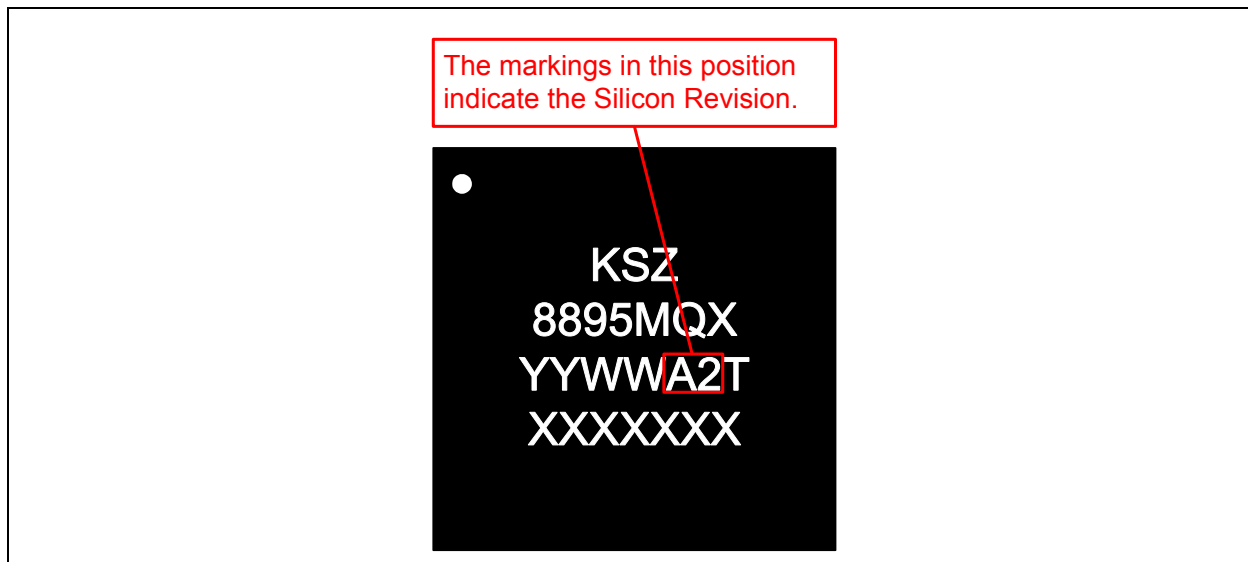
- KSZ8895MQX
- KSZ8895RQX
- KSZ8895FQX
- KSZ8895ML
- KSZ8895MLUB
- KSZ8864CNX
- KSZ8864RMNUB

The silicon errata discussed in this document are for silicon with silicon revisions as listed in [Table 1](#). The silicon revision can be determined by the device's top marking as indicated in [Figure 1](#). A summary of KSZ8895/KSZ8864 silicon errata, and the silicon revisions they apply to is provided in [Table 2](#).

TABLE 1: AFFECTED SILICON REVISIONS

Part Numbers	Silicon Revisions
KSZ8895MQX, KSZ8895RQX, KSZ8895FQX, KSZ8864CNX	A4
KSZ8895MQXCA, KSZ8895RQXCA, KSZ8895FQXCA, KSZ8895MQXIA, KSZ8895RQXIA, KSZ8895FQXIA, KSZ8864CNXCA, KSZ8864CNXIA	A2, A3
KSZ8895ML (SPNZ801061 for B3, KSZ8895MLX for A4)	B3, A4
KSZ8895MLUB, KSZ8864RMNUB	B2

FIGURE 1: TOP MARKING SILICON REVISION INDICATION



Note: The purpose of [Figure 1](#) is to detail the top markings of an example part and highlight the location of the silicon revision. Other top marking values may differ (lot codes, location of manufacture, etc.).

KSZ8895/KSZ8864

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	In I ² C mode, the EEPROM contents cannot be downloaded after reset	A2, A3, B2, B3, A4
2.	Packet loss due to long/short cable length	A2, A3, B2, B3
3.	Packet loss due to 20m cable length	A2, B2

Silicon Errata Issues

Module 1: In I²C mode, the EEPROM contents cannot be downloaded after reset

DESCRIPTION

In I²C mode, the EEPROM contents cannot be downloaded after a reset.

END USER IMPLICATIONS

When using I²C mode, the device will fail to read the EEPROM contents after a reset.

Work Around

Writing 0x0 to register 1 bits 7:4 (chip ID) in EEPROM will correct this issue.

PLAN

This errata is not planned to be corrected in a future revision.

Module 2: Packet loss due to long/short cable length

DESCRIPTION

Depending on the PCB implementation and quality of the cable, a minority of devices may exhibit packet losses with the LED always blinking on any PHY port. Typically this is likely to occur with long cable (>100m) or short cable (<2m or capacitor AC coupling).

END USER IMPLICATIONS

If using a long cable (>100m) or short cable (<2m or capacitor AC coupling), minor packet loss may be observed along with a blinking LED.

Work Around

Run the following initialization script after device power up, hardware reset and software power up:

```
w 0x47 1 // data 1
w 0x27 0 // write
w 0x37 0 // indirect register address 0x0
w 0x47 1 // data 1
w 0x27 0 // write
w 0x37 1 // indirect register address 0x1
w 0x79 0 // write 0x00 to direct register 0x79
// re-link each PHY port
w 0xnD 8 // Port n PHY power down
w 0xnD 0 // Port n PHY power up
// now configure the device as normal
```

Where *n* is 1 through 5 for the KSZ8895MQX/RQX/FQX/ML, 1 through 4 for the KSZ8895MLUB, and 2-3 for the KSZ8864CNX and KSZ8864RMNUB. The “w” in the script indicates a write to the specified register address.

If the switch ports are not connected to a link partner or the link partner is unpowered, it is not necessary to run the re-link section of this script.

PLAN

This errata has been corrected in silicon revision A4.

Module 3: Packet loss due to 20m cable length

DESCRIPTION

Depending on the PCB implementation and quality of the cable, there may be minor packet loss (approximately 2ppm) observed on any PHY port when using a cable length of approximately 20m +/- 2m.

END USER IMPLICATIONS

If using a cable length of approximately 20m +/- 2m, minor packet loss may be observed.

Work Around

Run the following initialization script after device power up, hardware reset and software power up:

```
w 0xAC 5 // write 0x05 to direct register 0xAC - this sets the receiver of the PHY to adjust
          DSP EQ (equalizer) settings.
w 0xAD 1 // write 0x01 to direct register 0xAD - this enables the new EQ settings configured in
          0xAC.
          // now configure the device as normal
```

The “w” in the script indicates a write to the specified register address.

PLAN

This errata has been corrected in silicon revisions A3/B3 and A4.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000697B (08-16-17)	Table 1 and Work Around for Module 3	Updated for clarity.
DS80000697A (04-18-16)	All	Initial release

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