KSZ9031MNX

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip KSZ9031MNX. These checklist items should be followed when utilizing the KSZ9031MNX in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 13. Detailed information on these subjects can be found in the corresponding section:

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The KSZ9031MNX implementor should have the following documents on hand:

- *KSZ9031MNX Data Sheet* (www.microchip.com/DS00002096)
- *Application Note ANLAN206*

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

3.0 POWER

- The analog supply (**AVDDH**) is located on pins 1 and 16, and requires a connection to **VDDA** (created from +3.3V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100-220Ω (at 100 MHz) ferrite bead is used. The AVDDH power supply line should have a 10 µF bulk capacitor, and each **AVDDH** pin should be decoupled with a 0.1 µF capacitor. The capacitor size should be SMD_0603 or smaller.
- The **AVDDL** (pins 4, 5, 12, and 13) is the analog core voltage supply. It should be connected to a +1.2V supply (created from +1.2V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100-220Ω (at 100 MHz) ferrite bead is used. The AVDDL power supply line should have a 10 µF bulk capacitor, and each **AVDDL** pin should be decoupled with a 0.1 µF capacitor. The capacitor size should be SMD_0603 or smaller.
- The **DVDDH** (pins 18, 30, 40, and 46) is the variable supply voltage for the I/O pads. It should be connected to the +3.3V, 2.5V, or 1.8V supply. A bulk capacitor must be placed close to the source to prevent any droop in the supply when the part starts. Decoupling capacitors must be placed as close to the part as possible to reduce high-frequency noise being injected through EMI interference.
- The **DVDDL** (pins 20, 25, 36, 42, and 54) is the digital core voltage supply. It should be connected to the +1.2V

supply. A bulk capacitor must be placed close to the source to prevent any droop in the supply when the part starts. Decoupling capacitors must be placed as close to the part as possible to reduce high-frequency noise being injected through EMI interference.

- **AVDDL_PLL** (pin 59) supplies power to the KSZ9031MNX PLL. Decouple **AVDDL_PLL** with a 4.7-10 µF capacitor, a 0.1 µF capacitor, and a 0.01 µF capacitor to ground, and join them to the +1.2V power trace or plane through a ferrite bead.

Power and ground connections without a Low-dropout (LDO) regulator are shown in Figure 3-1. Power and ground connections with a LDO (using an external MOSFET) are shown in Figure 3-2.

FIGURE 3-1: POWER AND GROUND CONNECTIONS WITHOUT LDO

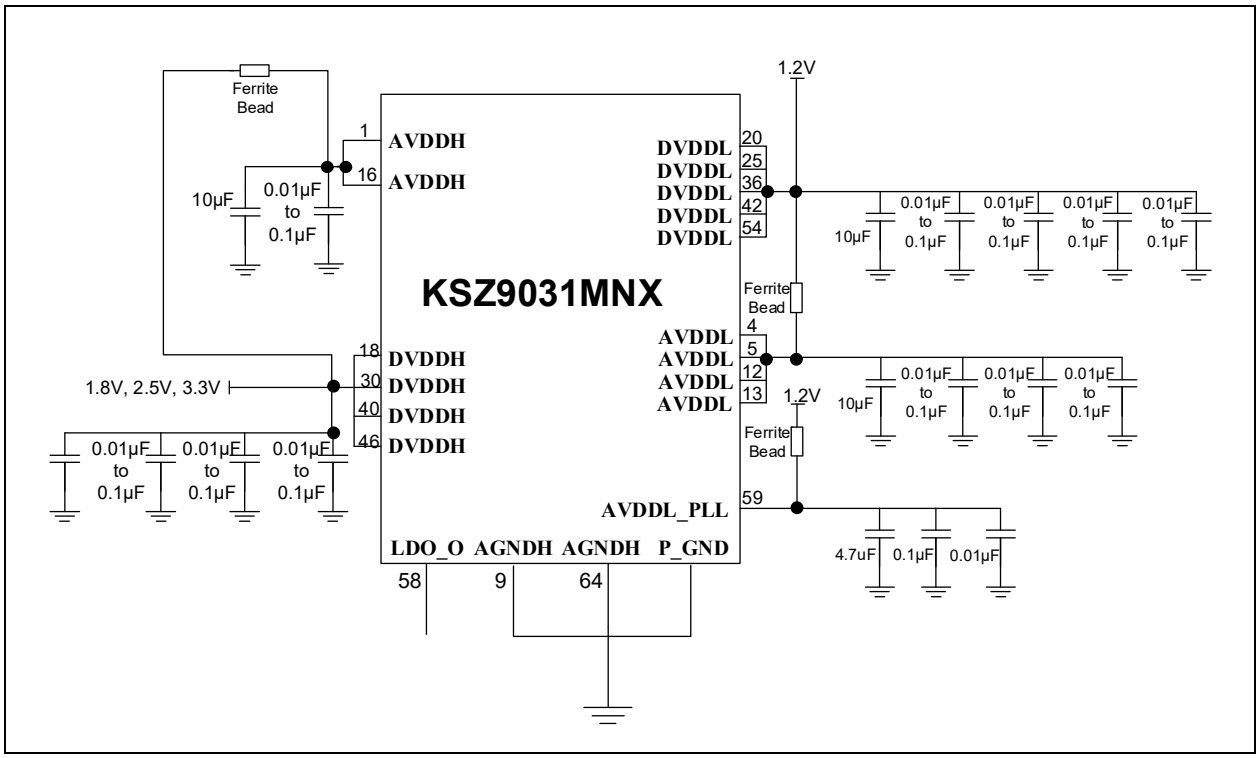
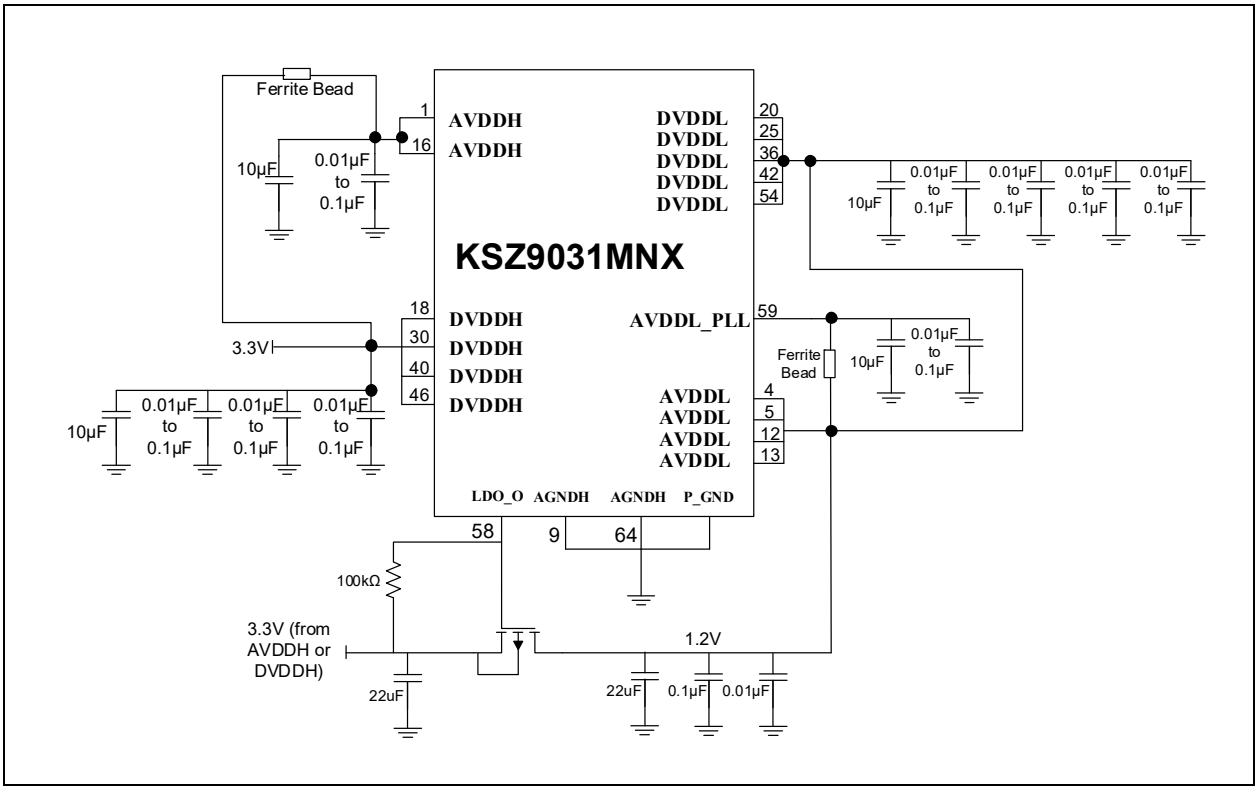


FIGURE 3-2: POWER AND GROUND CONNECTIONS WITH LDO



Caution: This +1.2V supply is for internal logic only. **Do not** power other circuits or devices with this supply.

The internal LDO controller is an optional feature that can reduce BOM cost by using one MOSFET as against multiple regulators for the 1.2V supply to the KSZ9031MNX. This 1.2V supply is not meant to power any other devices outside the KSZ9031MNX.

The LDO drives the gate of the MOSFET using 3.3V (either AVDDH or DVDDH) to the 1.2V core voltage to the **AVDDL**, **AVDDL_PLL**, and **DVDDL** supplies. The MOSFET should have a -VGS less than 2.5V with the ability to handle 250 mA of current at VDS of 1.9V. In addition, a 100 kΩ resistor should be added between the MOSFET gate and source to alleviate in-rush current from the 3.3V during LDO power-up.

If the LDO is not used, the **LDO_O** pin can be left as a No Connect (NC).

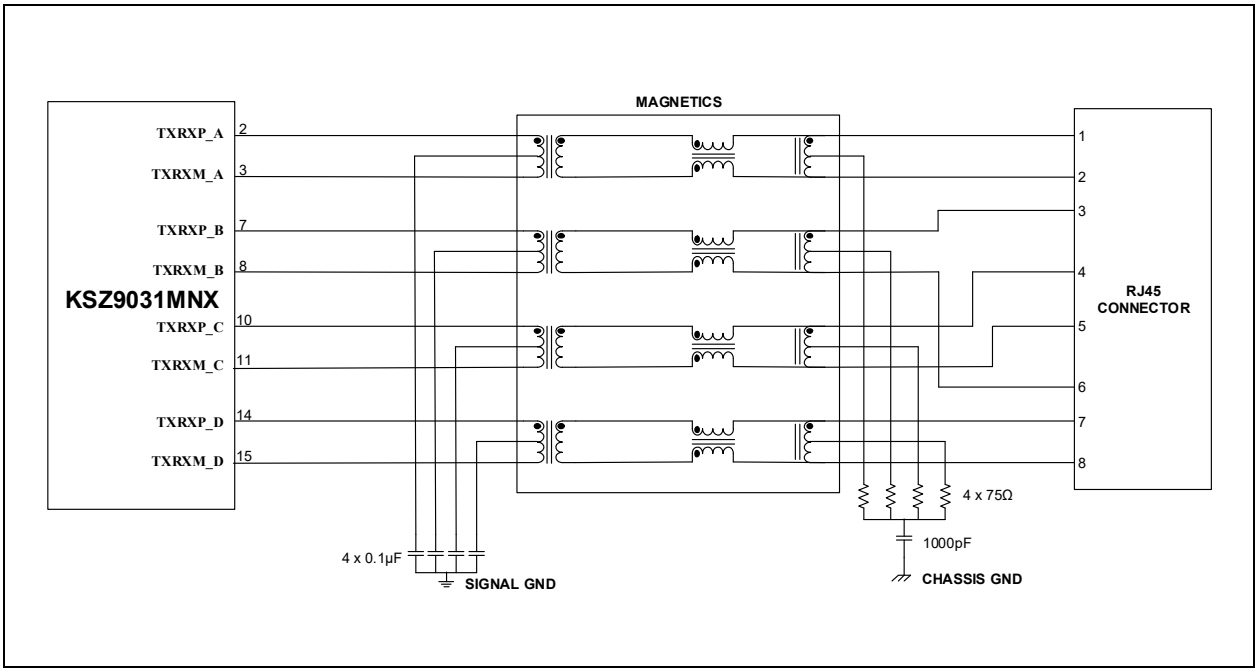
4.0 ETHERNET SIGNALS

4.1 10/100/1000 Mbps Interface Connection

- The following pins connect to the 10/100/1000 magnetics, and no external terminator and bias are needed:
  - **TXRXP_A** (pin 2): This pin is the transmit/receive (TX/RX) positive connection from pair A of the internal PHY.
  - **TXRXM_A** (pin 3): This pin is the TX/RX negative connection from Pair A of the internal PHY.
  - **TXRXP_B** (pin 7): This pin is the TX/RX positive connection from Pair B of the internal PHY.
  - **TXRXM_B** (pin 8): This pin is the TX/RX negative connection from Pair B of the internal PHY.
  - **TXRXP_C** (pin 10): This pin is the TX/RX positive connection from Pair C of the internal PHY.
  - **TXRXM_C** (pin 11): This pin is the TX/RX negative connection from Pair C of the internal PHY.
  - **TXRXP_D** (pin 14): This pin is the TX/RX positive connection from Pair D of the internal PHY.
  - **TXRXM_D** (pin 15): This pin is the TX/RX negative connection from Pair D of the internal PHY.

For 10/100/1000 Mbps channel connections details, refer to Figure 4-1.

FIGURE 4-1: 10/100/1000 MBPS CHANNEL CONNECTIONS



4.2 10/100/1000 Magnetics Connection

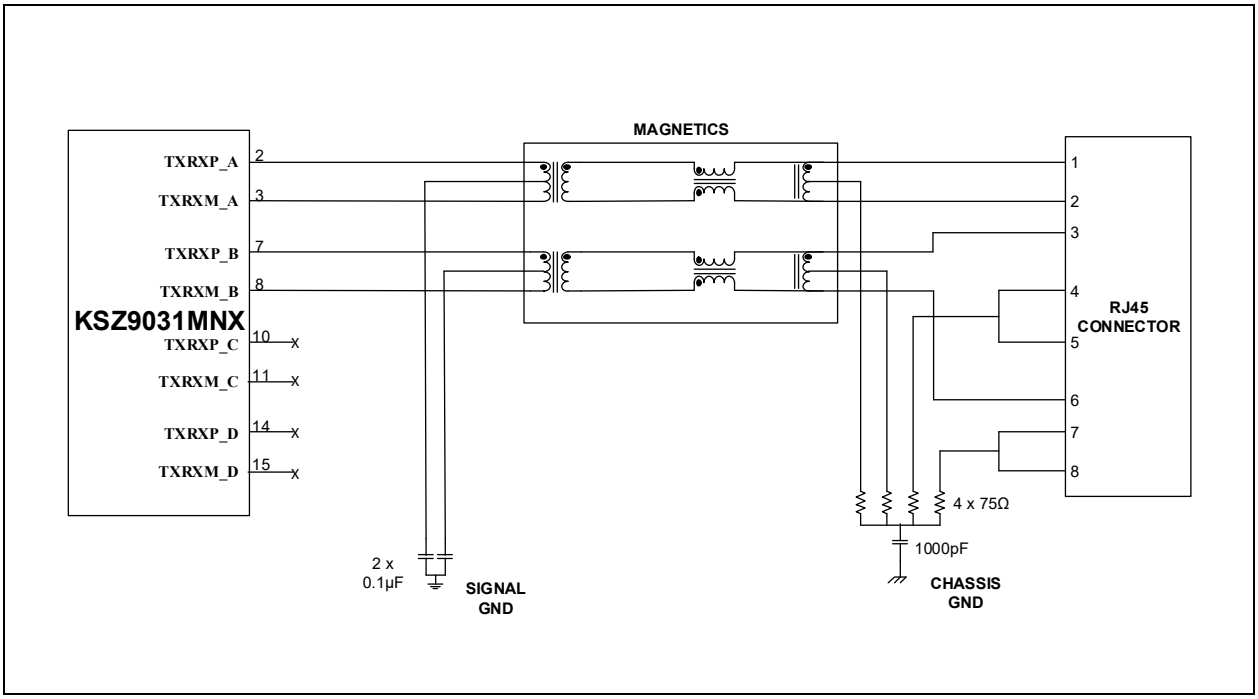
- The center taps on the chip side of the magnetics for all pairs should not be connected together without the 0.1 µF to ground. This is because the common-mode voltage can be different between pairs, especially for 10/100 operation (pairs A and B are active while pairs C and D are inactive).
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- The RJ45 shield should connect to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 8.2, "Other Considerations" for guidance on how the chassis ground should be created from digital/signal ground.

4.3 10/100 Mbps Interface Connection

- For designs needing only a 10/100 connection, the 1000 Mbps capability must be removed. The following removes the 1000 Mbps advertisement for Auto-Negotiation.
  1. Set Port Register 0x00, Bit [6] = '0' to remove 1000 Mbps speed.
  2. Set Port Register 0x09, Bits [9:8] = '00' to remove Auto-Negotiation advertisements for 1000 Mbps.
  3. Write a '1' to Register 0x00, Bit [9], a self-clearing bit, to force a restart of Auto-Negotiation.
- **TXRXP_A** (pin 2): This pin is the TX/RX positive connection from Pair A of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **TXRXM_A** (pin 3): This pin is the TX/RX negative connection from Pair A of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **TXRXP_B** (pin 7): This pin is the TX/RX positive connection from Pair B of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **TXRXM_B** (pin 8): This pin is the TX/RX negative connection from Pair B of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **TXRXP_C** (pin 10): This pin can be left as NC.
- **TXRXM_C** (pin 11): This pin can be left as NC.
- **TXRXP_D** (pin 14): This pin can be left as NC.
- **TXRXM_D** (pin 15): This pin can be left as NC.

For 10/100 Mbps channel connections details, refer to Figure 4-2.

FIGURE 4-2: 10/100 MBPS CHANNEL CONNECTIONS



4.4 10/100 Magnetics Connection

- The center tap connection on the KSZ9031MNX side for Pair A (TX Channel) only connects a 0.1 µF capacitor to GND, and no bias is needed.
- The center tap connection on the KSZ9031MNX side for Pair B (RX Channel) only connects a 0.1 µF capacitor to GND, and no bias is needed.
- The center taps of the magnetics of the TX and RX channels should not be connected together. This is because the common-mode voltage can be different between pairs.
- The center tap connection on the KSZ9031MNX side for the RX channel is connected to the TX channel center tap on the magnetics.
- The center tap connection on the cable side (RJ45 side) for Pair A should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for Pair B should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by both Pair A and Pair B center taps.
- MDI Connections:
  - Pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXRXP_A (pin 2) of the KSZ9031MNX.
  - Pin 2 of the RJ45 is TX- and should trace through the magnetics to TXRXM_A (pin 3) of the KSZ9031MNX.
  - Pin 3 of the RJ45 is RX+ and should trace through the magnetics to TXRXP_B (pin 7) of the KSZ9031MNX.
  - Pin 6 of the RJ45 is RX- and should trace through the magnetics to TXRXM_B (pin 8) of the KSZ9031MNX.
- MDIX Connections:
  - Pin 3 of the RJ45 is TX+ and should trace through the magnetics to TXRXP_B (pin 8) of the KSZ9031MNX.
  - Pin 6 of the RJ45 is TX- and should trace through the magnetics to TXRXM_B (pin 7) of the KSZ9031MNX.
  - Pin 1 of the RJ45 is RX+ and should trace through the magnetics to TXRXP_A (pin 2) of the KSZ9031MNX.
  - Pin 2 of the RJ45 is RX- and should trace through the magnetics to TXRXP_A (pin 3) of the KSZ9031MNX.
- When using the KSZ9031MNX device in the Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module (that is, the one where the two channels are identical) is required.

4.5 10/100 Mbps RJ45 Connection

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of accomplishing this:
  - Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of accomplishing this:
  - Pins 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- The RJ45 shield should be attached directly to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 8.2, "Other Considerations" for guidance on how chassis ground should be created from digital/signal ground.

5.0 CLOCK CIRCUIT

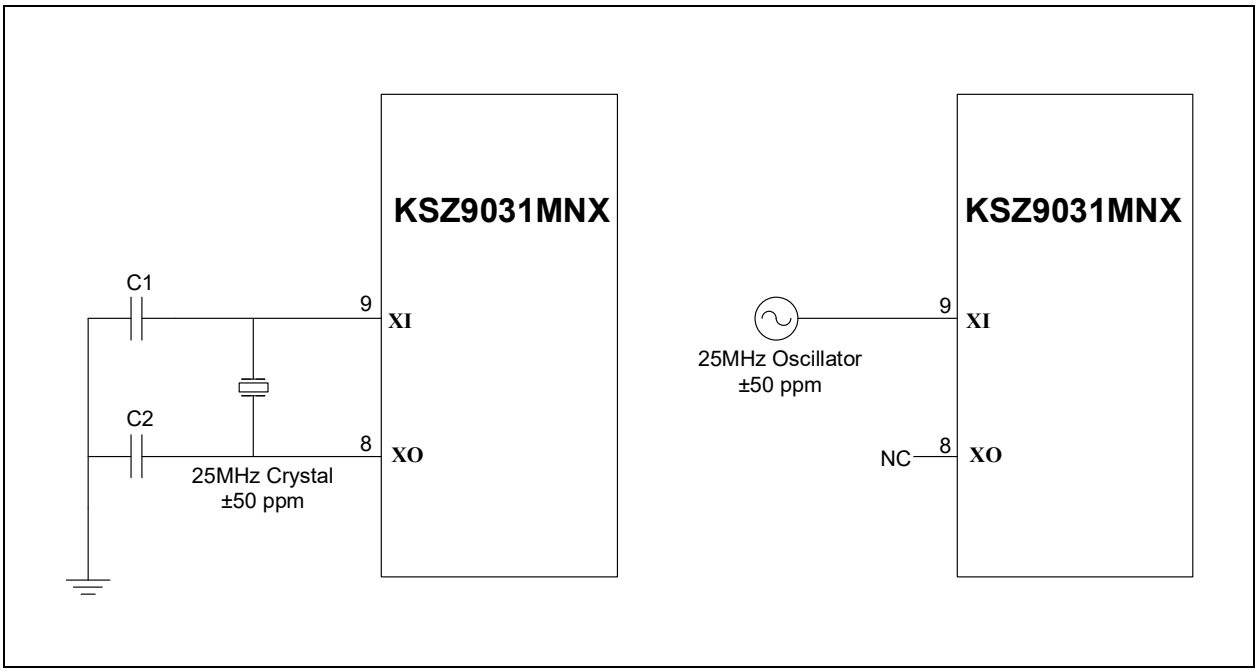
5.1 Crystal and External Oscillator/Clock Connections for MII Mode

A 25.000 MHz (±50 ppm) crystal should be used to provide the clock source. For exact specifications and tolerances, refer to the latest revision of the *KSZ9031MNX Data Sheet*.

- **XI** (pin 9) is the clock circuit input for the KSZ9031MNX device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XO** (pin 8) is the clock circuit output for the KSZ9031MNX device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system-dependent, based on the C_L spec of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.

Alternately, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the KSZ9031MNX. When using a single-ended clock source, **XO** (pin 8) should be left floating as a No Connect (NC).

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS

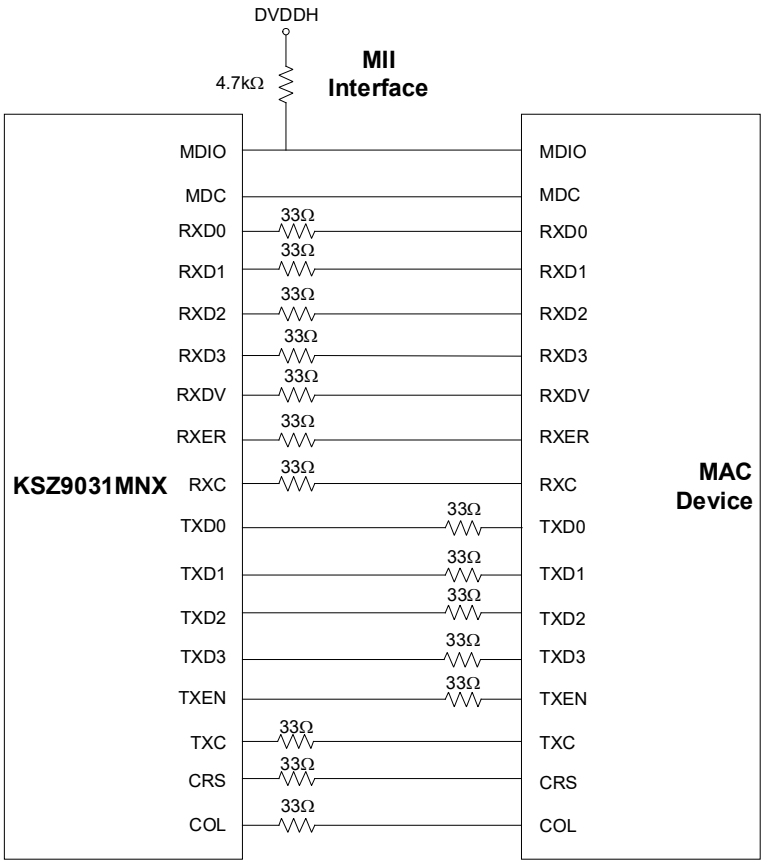


6.0 DIGITAL INTERFACES

6.1 MII Interface

- When utilizing either an external MII MAC interface or an MII connector, Figure 6-1 shows the proper connections for the 17 signals, including two management pins (MDC and MDIO).
- The KSZ9031MNX does not provide a TX_ER pin (Transmit error functionality on MII bus). Therefore, the TX_ER contact on the MII connector should be a No Connect (NC). Please see the MAC interface's data sheet for details on the TX_ER connection.
- Provisions should be made for series terminations for all outputs on the MII interface. Series resistors enable the designer to closely match the output driver impedance of the KSZ9031MNX and the PCB trace impedance to minimize ringing on the signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors is 33Ω.

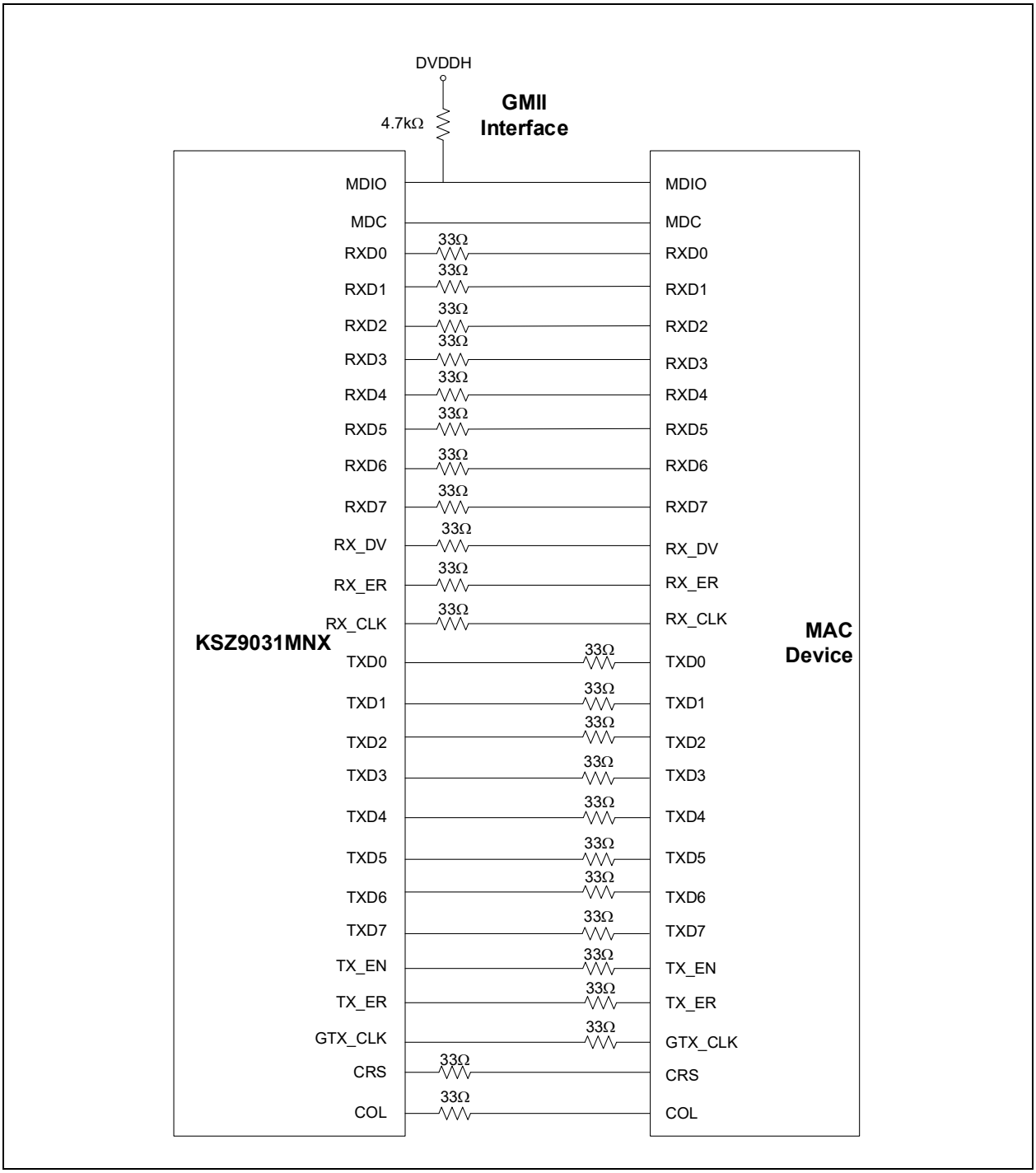
FIGURE 6-1: KSZ9031MNX MII CONNECTIONS



6.2 GMII Interface

- When utilizing either an external GMII MAC interface, Figure 6-2 indicates the proper connections for the 24 signals, including two management pins (MDC and MDIO).
- Provisions should be made for series terminations for all outputs on the GMII interface. Series resistors enable the designer to closely match the output driver impedance of the KSZ9031MNX and the PCB trace impedance to minimize ringing on the signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors is 33Ω.

FIGURE 6-2: KSZ9031MNX GMII CONNECTIONS



6.3 Required External Pull-Ups

- When using the KSZ9031MNX MDC/MDIO management pins, a pull-up resistor of 1 kΩ to 4.7 kΩ on the **MDIO** signal (pin 51) is required.
- If used, the **INTRP** (pin 53) requires a 4.7 kΩ external pull-up resistor since this output is an open drain. If the **INTRP** pin is not used then this pin can float.

7.0 STARTUP

7.1 Reset Circuit

RST# (pin 56) is an active-low reset input. This signal resets all logic and registers within the KSZ9031MNX. A hardware reset (RST# assertion) is required following power-up. Please refer to the latest copy of the *KSZ9031MNX Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the KSZ9031MNX when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

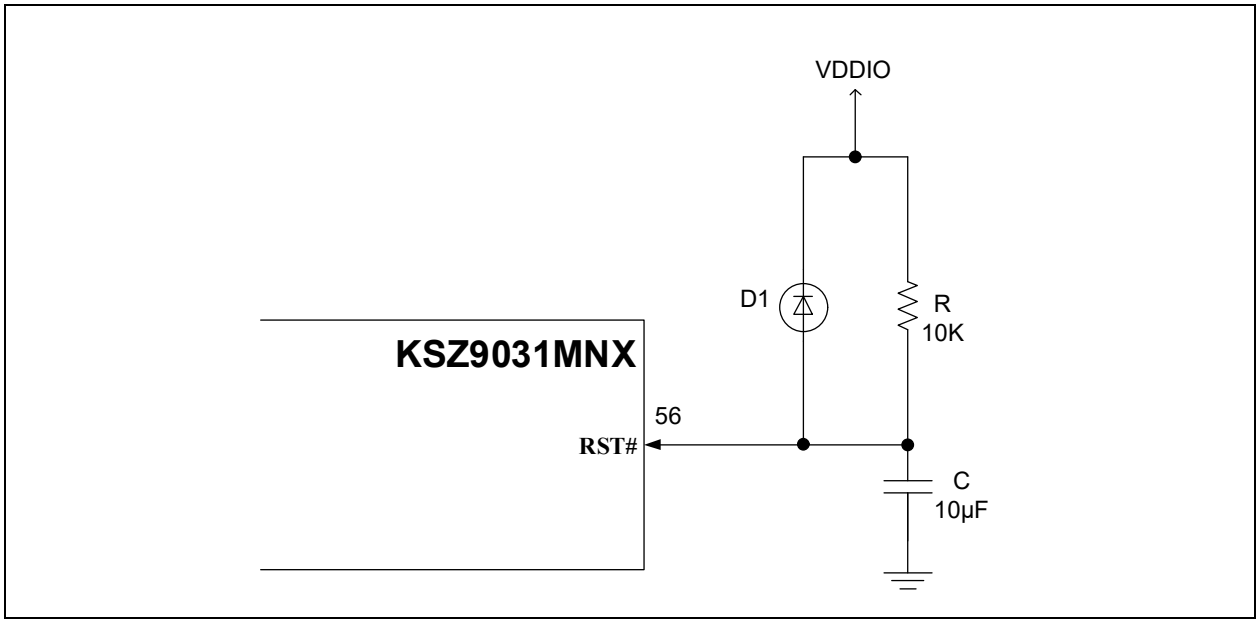


Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU or FPGA. The reset out pin (RST_OUT_n) from the CPU/FPGA provides the warm reset after power-up. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be directly connected.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT

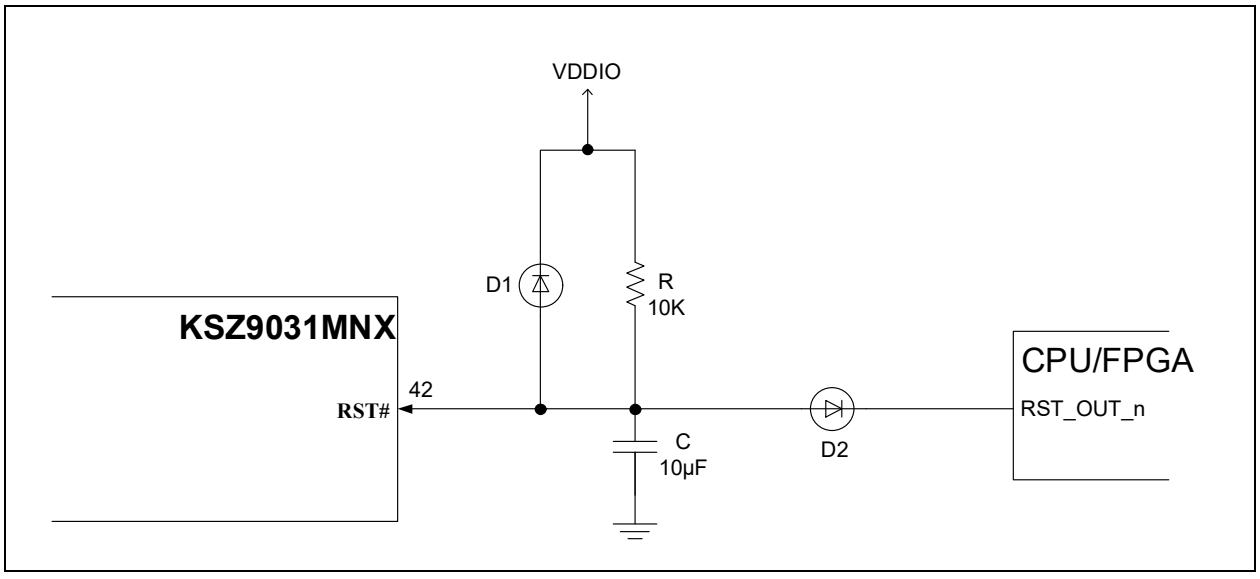
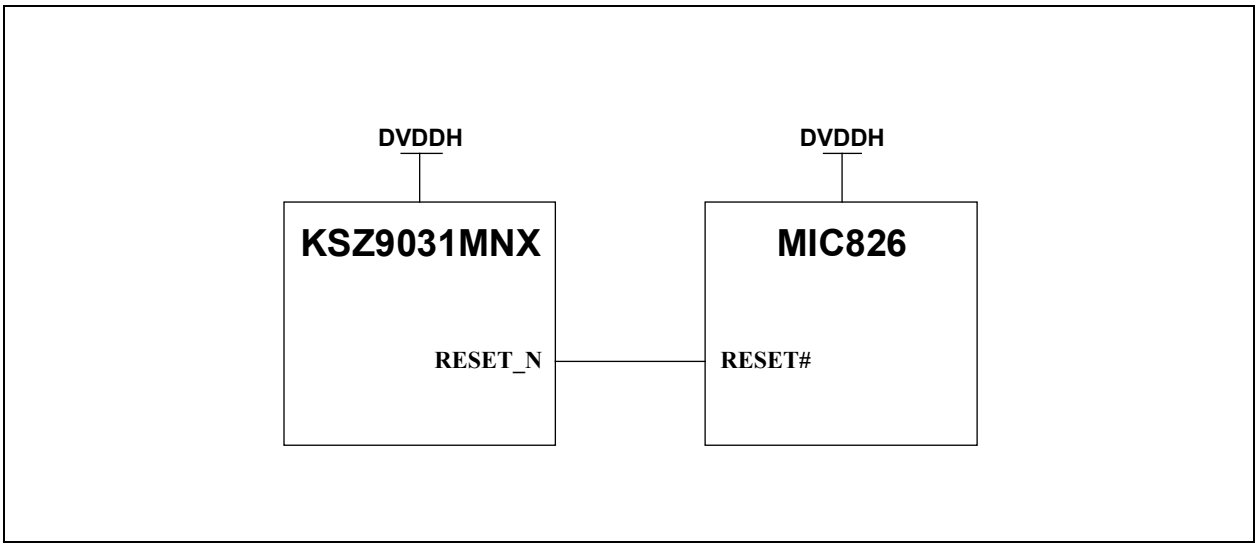


Figure 7-3 illustrates the reset circuit with an MIC826 voltage supervisor driving the KSZ9031MNX reset input.

FIGURE 7-3: RESET BY VOLTAGE SUPERVISOR



7.2 Configuration Mode Pins (Strapping Options)

The configuration mode pins of the KSZ9031MNX (**MODE[3:0]**) control the default configuration of the 10/100 PHY. The value of these three pins are latched upon power-up and reset. The configuration straps should be strapped either high (4.7-10 kΩ) or low (1-4.7 kΩ). Refer to the *"Strapping Options - KSZ9031MNX"* table of the data sheet.

7.3 LED Pins

- The KSZ9031MNX provides two LED signals. These indicators display speed, link, and activity information about the current state of the PHY. The LED pins drive low to light up the LED indicators, which should have their anode ends tied to 3.3V and their cathode ends tied through a series resistor (typically 220-470Ω). Refer to the *KSZ9031MNX Data Sheet* for further details on how to connect each pin for correct operation.
- The LED functionality signal pins are shared with the following pin strapping functions:
  - LED2 is shared with **PHYAD1** on pin 17 for KSZ9031MNX.
  - LED1 is shared with **PHYAD0** and **PME_N1** on pin 19 for KSZ9031MNX.

Note 1: For 1.8V VDDIO, LED indication support is not recommended due to the low voltage. Without the LED indicator, the PHYAD1 and PHYAD0/PME_N1 strapping pins are functional with a 4.7 kΩ pull-up to 1.8V VDDIO (or be floated) for a value of '1', and with a 1.0 v pull-down to ground for a value of '0'.

2: If using RJ45 jacks with integrated LEDs and 1.8V VDDIO, a level shifting is required from LED 3.3V to 1.8V. In this case, a BJT or MOSFET or a level shifting device can be used.

8.0 MISCELLANEOUS

8.1 ISET Resistor

The **ISET** pin on the KSZ9031MNX must connect to ground through a 12.1 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the embedded 10/100/1000 Ethernet physical device. Maintain spacing between the ISET trace and resistor, and the XI clock trace, to avoid coupling between them.

8.2 Other Considerations

- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This allows some flexibility at EMI testing for different grounding options. Leaving the footprint open allows the two grounds to remain separate. Shorting them together with a zero ohm resistor connects them. For best performance, short them together with a cap or a ferrite bead.
- Be sure to incorporate enough bulk capacitors (4.7-22 µF) for each power plane.
- If using CLK125_NDO, this 125 MHz clock should not go directly to the RGMII MAC unless there is a PLL in the RGMII MAC. If CLK125_NDO is unused, it should be disabled by pulling down RX_DV/CLK125_EN.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.2, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.3, "Ground"	Verify that the grounds are tied together.		
Section 3.0, "Power"	Section 3.0, "Power"	• Ensure **VDDA_3.3** and **VDDIO** are in the range 3.135-3.465V, and a 10 µF capacitor is on each pin. **VDDIO** can also be 1.8V or 2.5V. • **VDD_1.2** requires two 0.1 µF capacitors. • For LDO designs, check that the capacitance on both the drain and source of FET have at least 22 µF. • For LDO designs, make sure the 100 kΩ resistor is in place (see Figure 3-2) to prevent inrush current.		
Section 4.0, "Ethernet Signals"	Section 4.1, "10/100/1000 Mbps Interface Connection"	Verify that each pair's positive and negative connections go to the following: Pair A - Pair 1 of the magnetics Pair B - Pair 2 of the magnetics Pair C - Pair 3 of the magnetics Pair D - Pair 4 of the magnetics		
	Section 4.2, "10/100/1000 Magnetics Connection"	Verify that each of Pair A, Pair B, Pair C, and Pair D center taps goes from a 0.1 µF capacitor to digital/signal GND. There cannot be a shorting of connections to a common point before these capacitors.		
		Verify that the magnetics on each cable-side center-tap goes through a 75Ω resistor.		
		Verify that the center taps of all pairs go to a common point through a 1000 pF, 2 kV capacitor to chassis GND.		
	Section 4.3, "10/100 Mbps Interface Connection" (10/100 only)	Verify that each pair's positive and negative connections go to the following: Pair A - Pair 1 of the magnetics Pair B - Pair 2 of the magnetics Pair C - No Connect (NC) Pair D - No Connect (NC)		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 4.0, "Ethernet Signals"	Section 4.4, "10/100 Magnetics Connection" (10/100 only)	Verify that each of Pair A and Pair B center taps go from a 0.1 µF capacitor to digital/signal GND. There cannot be a shorting of the connections to a common point before these capacitors.		
		Verify that the cable sides of the two magnetic center taps, RJ45 pins 4/5 and RJ45 pins 7/8, are each terminated with a 75Ω resistor to a signal 1000 pF, 2 kV capacitor to ground.		
	Section 4.5, "10/100 Mbps RJ45 Connection" (10/100 only)	Verify pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable and are terminated to chassis ground through a 1000 pF, 2 kV capacitor.		
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Oscillator/Clock Connections for MII Mode"	Verify usage of 25 MHz ±50 ppm crystal or 25 MHz ±50 ppm clock source.		
Section 6.0, "Digital Interfaces" (KSZ9031MNX GMII/MII)	Section 6.1, "MII Interface", Section 6.2, "GMII Interface", and Section 6.3, "Required External Pull-Ups"	Confirm proper GMII/MII signals between MAC and PHY interface based on Figure 6-1 (MII) or Figure 6-2 (GMII). Confirm proper GMII/MII signals between MAC and PHY interface with correct termination resistors (33Ω) and external pull-up for MDIO signal.		
Section 7.0, "Startup"	Section 7.1, "Reset Circuit"	Confirm proper reset circuit design: standalone reset or external CPU/FPGA reset.		
	Section 7.2, "Configuration Mode Pins (Strapping Options)"	Confirm Mode Settings and PHYAD (PHY Address) Settings		
		Make sure each strapping pin has a pull-up or pull-down resistor.		
	Section 7.3, "LED Pins"	If used, confirm proper connections, taking into consideration shared functionality on select LED pins.		
Section 8.0, "Miscellaneous"	Section 8.1, "ISET Resistor"	Confirm proper ISET resistor (6.49 kΩ, 1.0%).		
	Section 8.2, "Other Considerations"	• Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the chip ground instead of the digital ground. • Incorporate sufficient power plane bulk capacitors (4.7-22 µF).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003390A (02-20-20)	Initial release	

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

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Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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