
ATA6560 - CAN Transceiver VHDL-AMS Model (Level 2)

ATAN0132

Introduction

This document contains the documentation for the simulatable, simulation-runtime-optimized behaviorally modeled high-speed-CAN transceiver Atmel® ATA6560 according to [1] and was tested according to [2]. The implementation level of the provided model is according to the “Level 2” model requirements of [1], see [Section 1. “Implementation” on page 3](#) for more details. This “Level 2” model is intended to be used only for bus signal integrity checks, network power-up/downs and reduced diagnosis and does not cover the full functionality of the real transceiver device.

Terms, Definitions and Abbreviations

Table 1. Terms, Definitions and Abbreviations

Short Name	Definition
BUS	CAN BUS
CANH	CAN BUS high channel
CANL	CAN BUS low channel
CM	Common mode = $(CANH + CANL) / 2$
CAND	Differential mode = $(CANH - CANL)$
STBY	Standby mode
NSIL/SIL	Silent mode, only listen to the BUS
RXD	Receiver pin / receiver signal
TXD	Transceiver pin / transceiver signal
VCC	Supply pin / supply level / supply signal
GND	Ground pin / ground level / ground signal

List of References

- [1] Requirement Specification for Transceiver Simulation Models V1.1, ICT/GIFT, 2010-02-22
- [2] Model Conformance Test Specification V1.1, ICT/GIFT, 2010-02-22
- [3] Road vehicles – Controller Area Network, Highspeed medium access unit, ISO 11898-2, 2003
- [4] Road vehicles – Controller Area Network, Highspeed medium access unit with low power mode, ISO 11898-5, 2007

1. Implementation

1.1 Implementation Language

The provided model is completely implemented in VHDL-AMS (IEEE 1076.1-1999). The implementation body is encrypted according to VHDL (IEEE 1076-2008) directives under SABER framework. An encrypted version for SystemVision framework may be available on customer demand. The model is implemented and tested to be compliant and executable at the following simulator environment:

- Synopsys SABER (Version B-2008.09-SP2 or newer)
- Mentor Graphics SystemVision (Version 5.9 or newer)

1.2 Functionalities and Properties

The model is implemented as a “Level 2” model according to [1] and therefore covers the following functionalities:

- Transmitter function (output voltages and currents, rise and fall times, propagation delays, ground offset)
- Receiver function (thresholds, propagation delays, ground offset)
- Bus biasing (impedances)
- Operating modes (current consumption at supply pins, impedance behavior on bus pins for all modes)
- Diagnosis (under-voltage detection levels and timings)
- Bus wake-up (wake-up receiver timings and thresholds)

Notes:

1. The current model implementation cannot be initialized with an operating mode stimulus other than “power down” meaning all supplies are off. The device shall be powered up like the real device. For more info about the possible operating mode state transitions, please see the datasheet of the device. An example implementation is shipped with the demo test bench.
2. This level 2 model implementation introduces operational mode state transition timings in a functional manner. That means the model reflects the timings between state transitions, but may not reflect the analogue real device behavior at all output pins while during the active transition, e.g. in terms of impedance changing.

1.3 Functionalities not Implemented

The current model implementation does not cover correct short circuit behavior in terms of flowing currents and their value. The real device sets an internal flag, when the current exceeds some limits, but this diagnosis functionality is not required for a “Level 2” model.

2. Interface

As required, the level 2 of the model is pin-out compatible with the real device (see [Figure 2-1](#)) and the interface is implemented according to section 3.3 and 3.6 of [1] with all mandatory pins and parameters. Refer to [Table 2-1](#) for a short description of each pin.

Figure 2-1. Real Device Pin-out

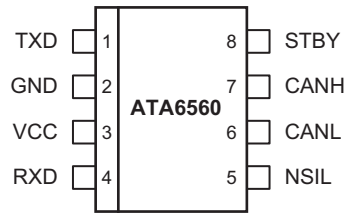


Table 2-1. Model Interface for Level 2

PIN Name	Description
CANH	CAN BUS high channel
CANL	CAN BUS low channel
STBY	Standby mode
NSIL	Silent mode
RXD	Receiver
TXD	Transceiver
VCC	Supply
GND	Ground

3. Parameters

The model is parameterized regarding the high, low and typical characteristics of the device. The interface contains the model parameter “TEMP”. The following values are possible.

Table 3-1. Parameter “TEMP”, Possible Values

“TEMP” Value	Description
–1	This setting covers the low temp behavior based on real device measurements and minimal characteristics as stated in the device datasheet
0	This setting covers the room temp behavior based on real device measurements and typical characteristics as stated in the device datasheet
1	This setting covers the high temp behavior based on real device measurements and maximal characteristics as stated in the device datasheet

3.1 Time Delays Implementation

In order to reach a balance between the specification in datasheet and the values obtained from the verification process measures, an interpolation was made with the delays parameters. In [Table 3-2](#), the parameters from datasheet are shown while in [Table 3-3](#) the interpolated values implemented in this model are shown.

It is worth to mention that the delay at the edge from dominant to recessive state was over-delayed with respect to the interpolation rule. This was done in order to achieve a typical delay based in our laboratory measurements, as no information was provided from the manufacturer. The results are clearly visible for a room temperature in a star topology ringing behavior (see [Section 7. “Network Behavior” on page 17](#)).

Table 3-2. Propagation Delays from Datasheet

Delay	Transition	Measurement			Unit
		Low	Room	Max	
TXD to RXD	DOM to REC	40	-	200	[ns]
	REC to DOM	40	-	200	[ns]
TXD to CAN	DOM to REC	40	-	130	[ns]
	REC to DOM	40	-	130	[ns]
CAN to RXD	DOM to REC	20	-	100	[ns]
	REC to DOM	20	-	100	[ns]

Table 3-3. Propagation Delays, Implemented Values

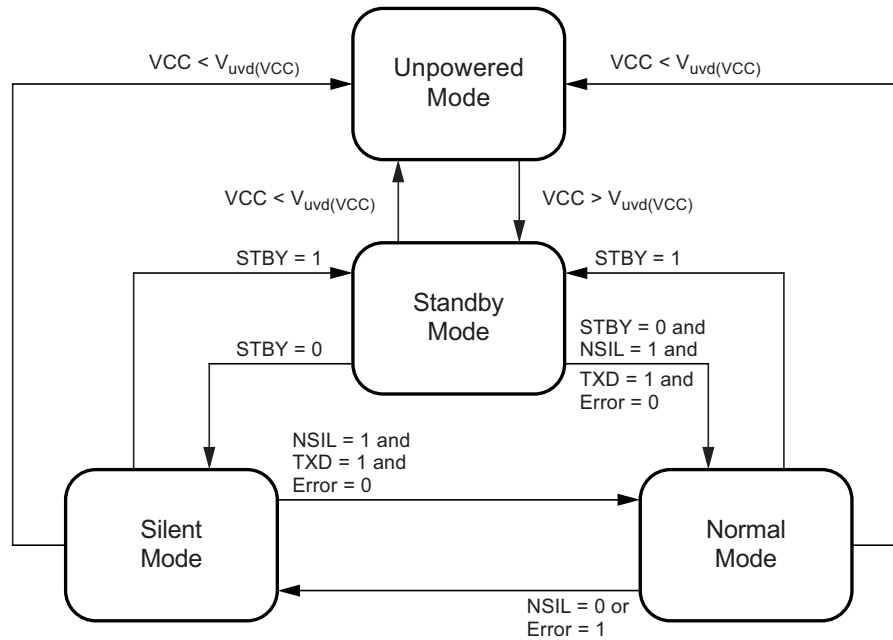
Delay	Transition	Measurement			Unit
		Low	Room	Max	
TXD to RXD	DOM to REC	40	116.25	195.5	[ns]
	REC to DOM	40	116.25	195.5	[ns]
TXD to CAN	DOM to REC	26.666	67.083	110.5	[ns]
	REC to DOM	26.666	67.083	110.5	[ns]
CAN to RXD	DOM to REC	13.333	49.1666	85	[ns]
	REC to DOM	13.333	49.1666	85	[ns]

4. Modeled States

A series of tests were performed in order to show the actual behavior of the model, which was developed in a level 2 approach with full compatibility with the states of the real device. In [Figure 4-1](#) the state machine is shown.

The states are analyzed in the detail for the 3 temperature scenarios (high, room and low) in the following sections.

Figure 4-1. Real Device State Machine



4.1 Behavior for 3 Parameterized Scenarios

4.1.1 Initial State, Standby and Normal Mode

As mentioned in [Section 1. "Implementation" on page 3](#), the model requires that an external test-bench perform a supply level similar as the reality, i.e. starting from zero energy and then rising-up to a certain value in a certain time. In all our test-benches this kind of approach is implemented for external signals in order to avoid initialization problems.

In [Figure 4-2 on page 7](#) the initial state "reset" is shown as well as the change to standby mode for all 3 possible scenarios (parameter "TEMP" in low, room, and high). On each scenario a different parameter value may be applied for characteristics such as delays or voltage levels.

In [Figure 4-3 on page 7](#) a further analysis shows how after shifting the STBY level to low, the state changes from standby to normal, with the respective delay for Low, Room and High scenarios.

Figure 4-2. Initialization

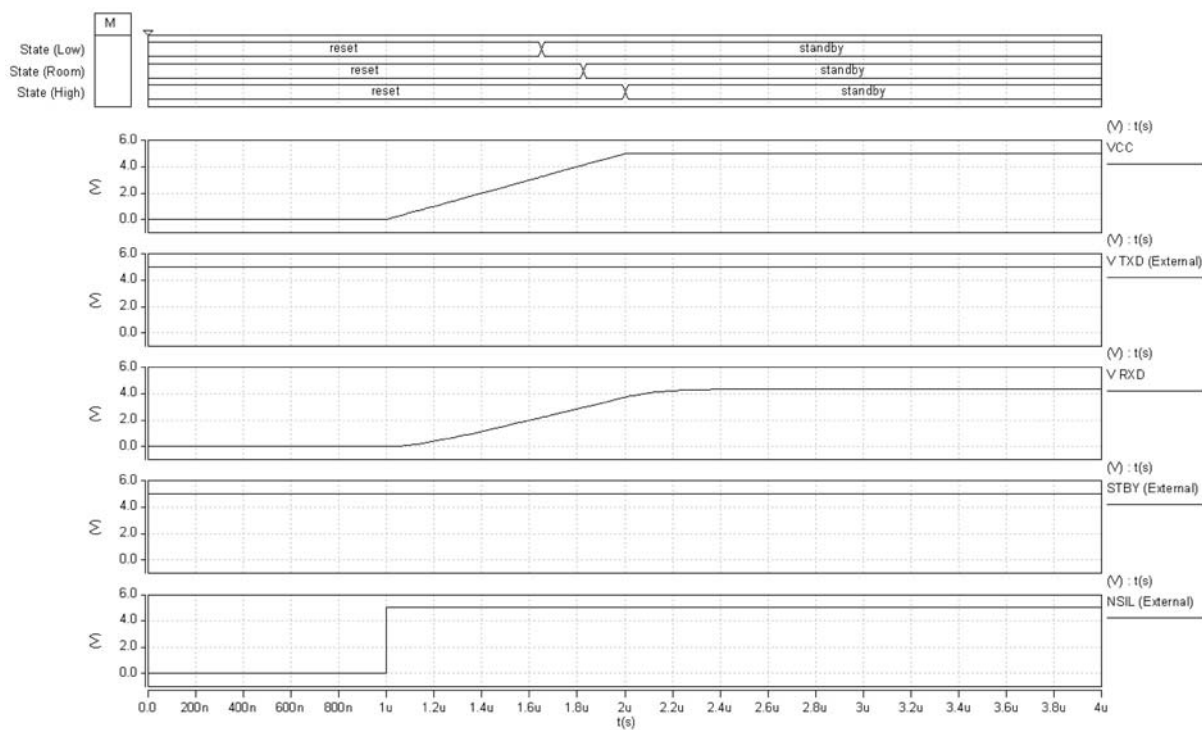
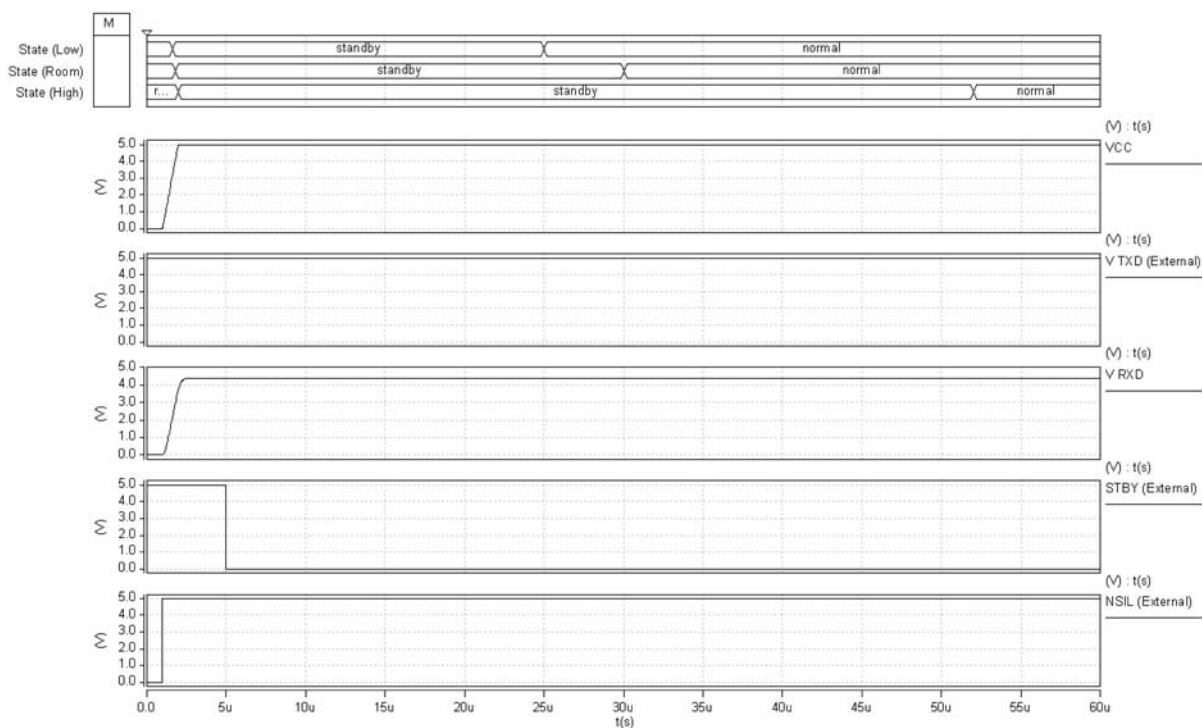


Figure 4-3. Reaching Normal State



4.1.2 Standby Mode (STBY)

Figure 4-4 and Figure 4-5 on page 9 show the behavior of the model during standby mode. In Figure 4-4 only the delays for the three possible scenarios are shown while in Figure 4-5 on page 9 the neglecting of external pulses at the BUS is shown. Pulses are neglected before the device enters in normal mode.

Figure 4-6 on page 9 shows the wake signal at RXD pin when a dominant pulse longer than t_{wake} arrives to the BUS. If the pulse duration is longer than t_{to_BUS} , then the RXD is switched automatically to high level with the intention to prevent a clamped dominant BUS.

Figure 4-4. Activating / Deactivating Standby Mode

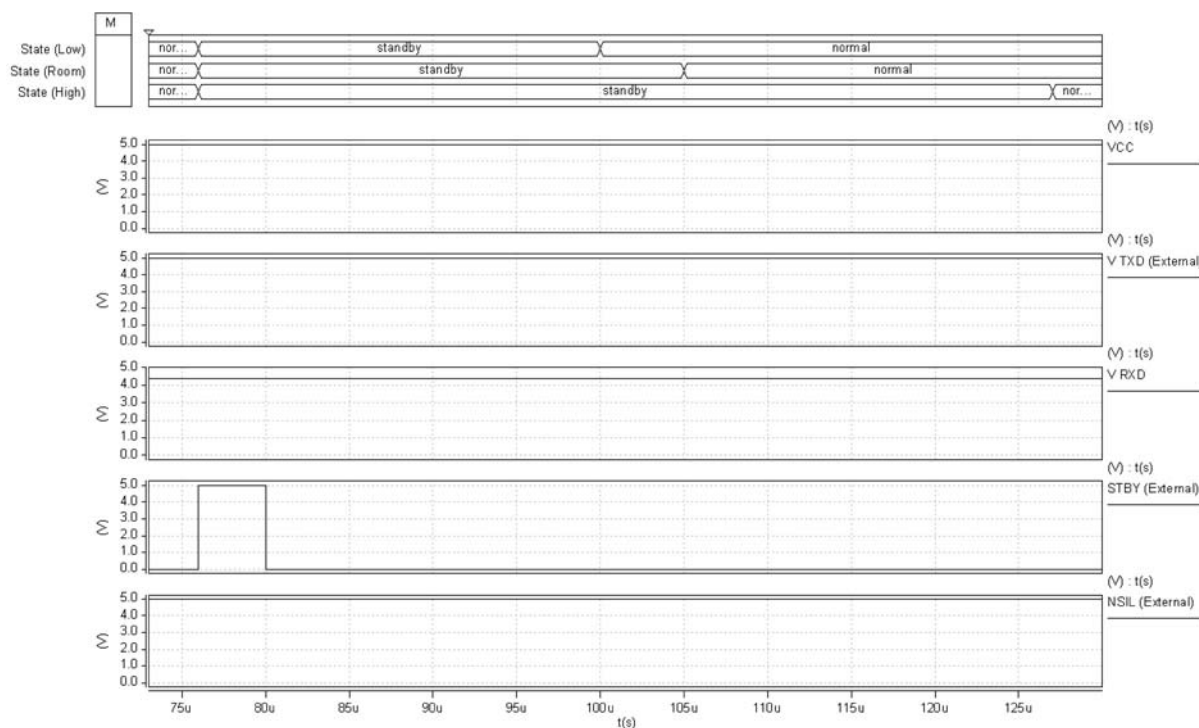


Figure 4-5. Standby Mode Behavior

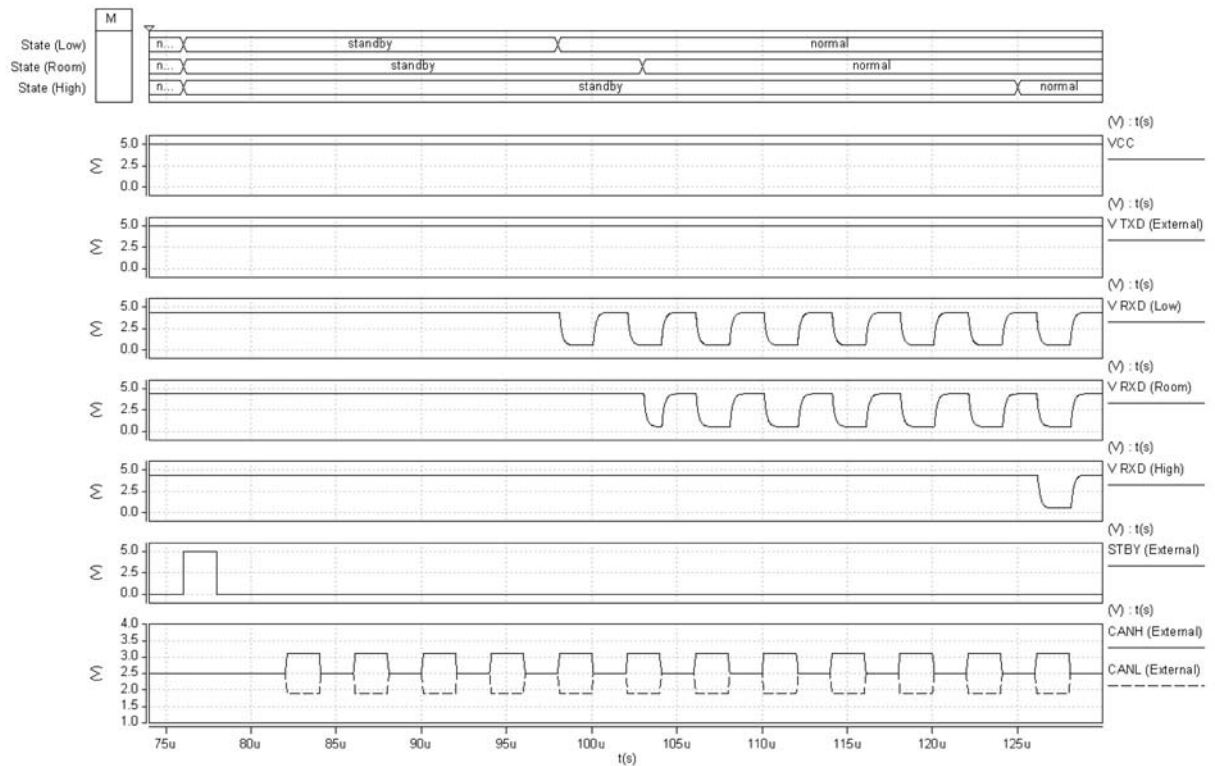
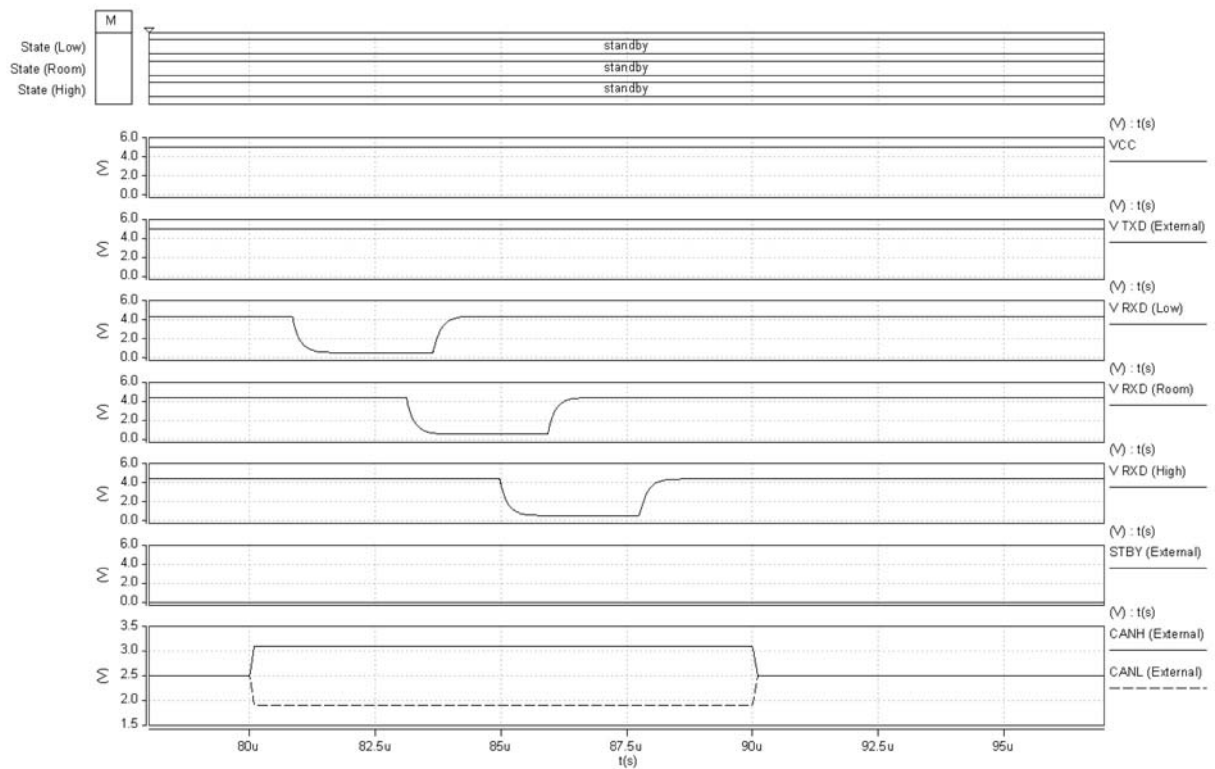


Figure 4-6. Standby Mode, Wake from Bus, Signaling at RXD Pin



Note: In [Figure 4-5 on page 9](#), the wake signal at RXD was avoided in the Low case scenario. In this scenario the requested time for a dominant pulse in the BUS is minimal and it was not possible to show the neglecting of the BUS signals for bit times of 2 μs .

4.1.3 Silent Mode (NSIL)

[Figure 4-7](#) shows the use of the NSIL pin to activate and deactivate the silent mode (only listen). [Figure 4-8](#) shows also the behavior of the model during this mode. A TXD signal will be neglected during silent mode and any dominant pulse at the BUS will be transmitted to the RXD pin.

Figure 4-7. Activating / Deactivating Silent Mode

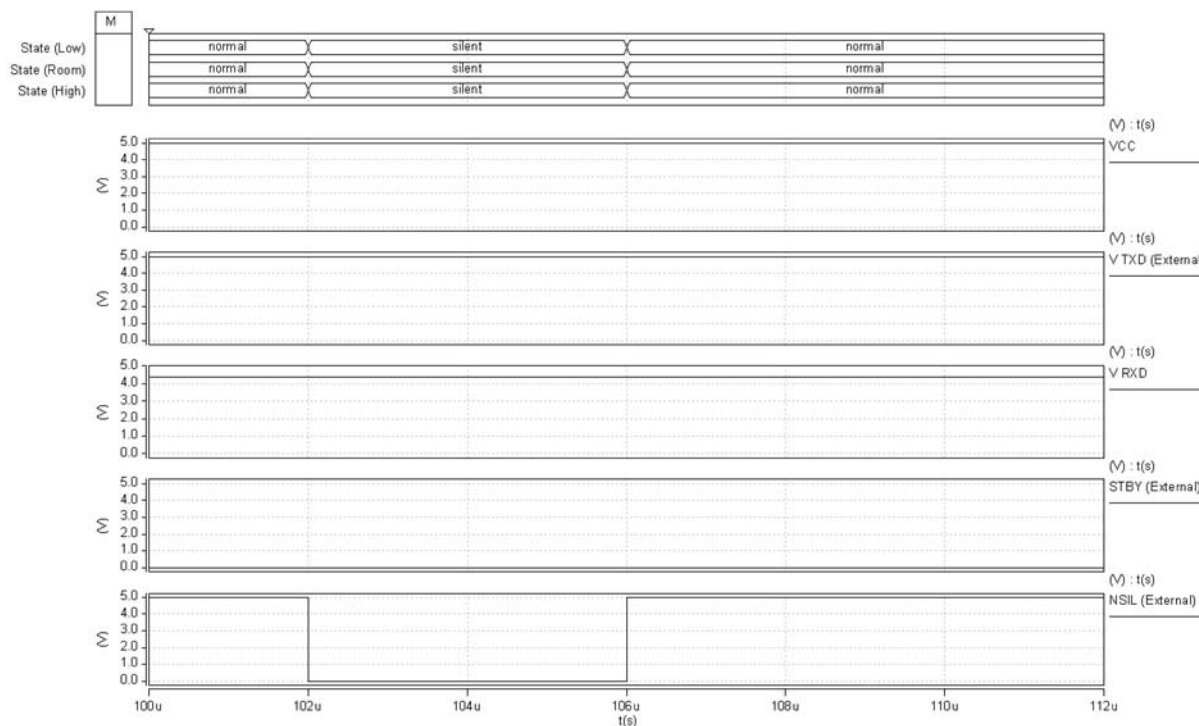
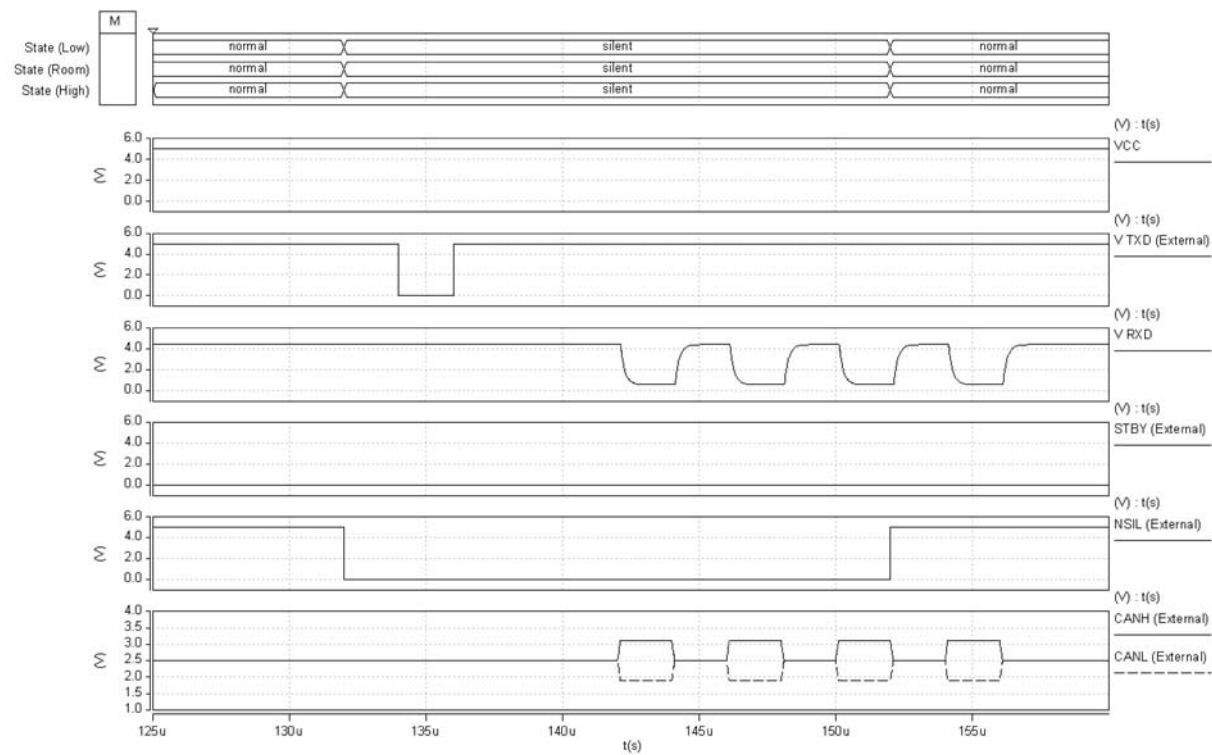


Figure 4-8. Silent Mode Behavior

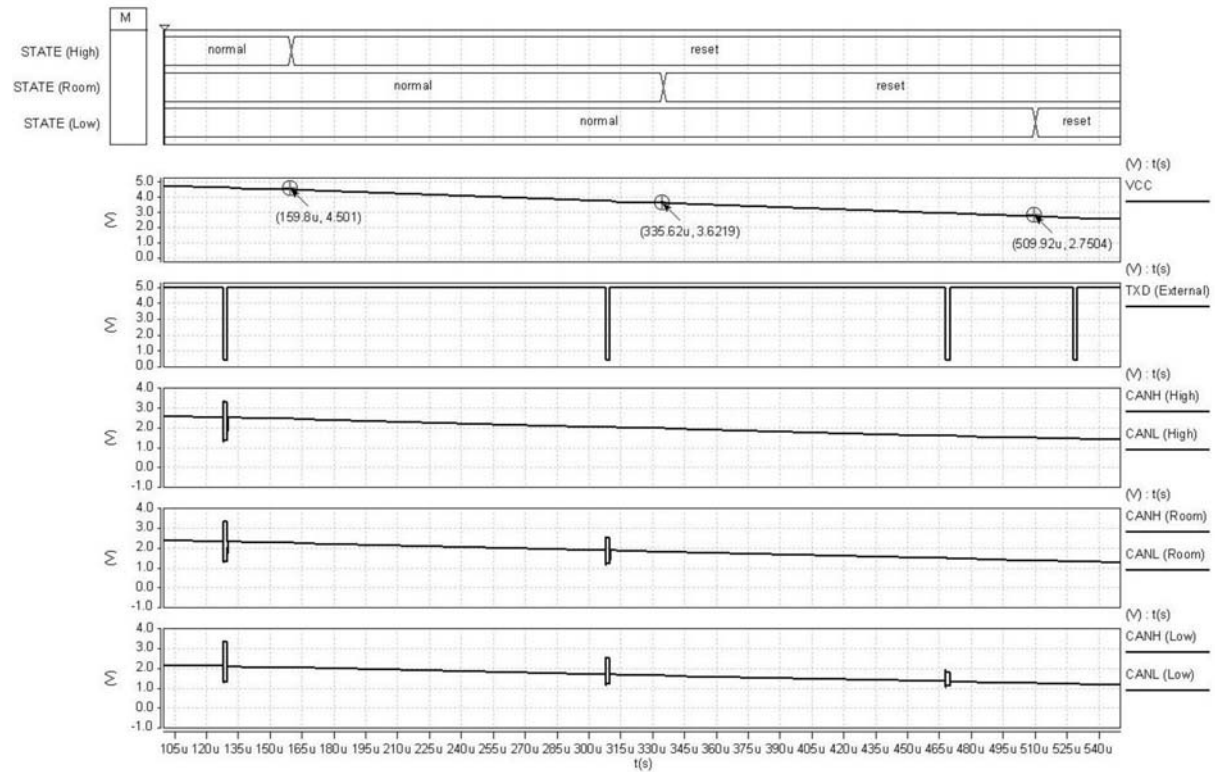


5. Undervoltage Detection

The undervoltage detection thresholds were modeled as described by the parameters in the datasheet. In Figure 5-1 is shown a test where the model in its 3 possible temperature parameterization is run. At the top of the figure the internal states of the model are shown (high, low and room scenarios). The supply (VCC) and the dominant bits at the TXD pin are common in the 3 test cases, while CANH and CANL are shown separately in the same figure.

In this test case a falling voltage is applied to VCC. The slew rate is very slow in order to appreciate when the model changes its internal state.

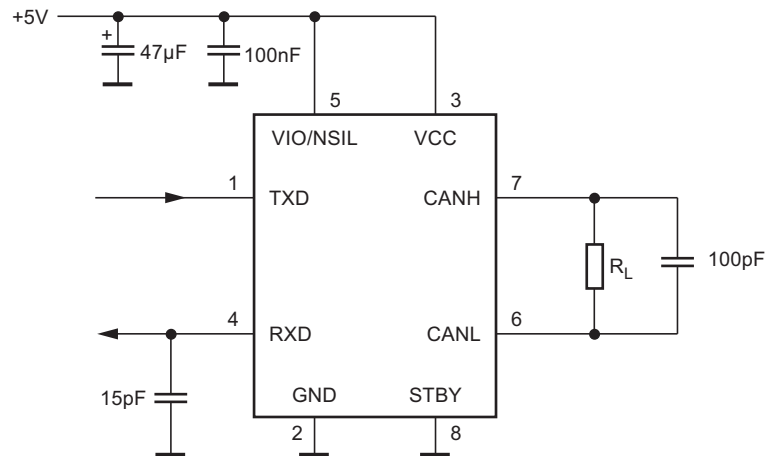
Figure 5-1. Undervoltage Behavior



6. Signal Matching

In this section is shown a match between the measured waveforms and the simulation results of the model. This test was performed in the 3 temperatures scenarios and analyzed in maximal detail for dominant to recessive and recessive to dominant edges. The results are shown from Figure 6-2 to Figure 6-7. Figure 6-1 shows the implemented test circuit, which is the same as the datasheet specifies. R_L is 62 $[\Omega]$

Figure 6-1. Test Circuit



6.1 Dominant to Recessive Edge

Figure 6-2. Dominant to Recessive Edge (High)

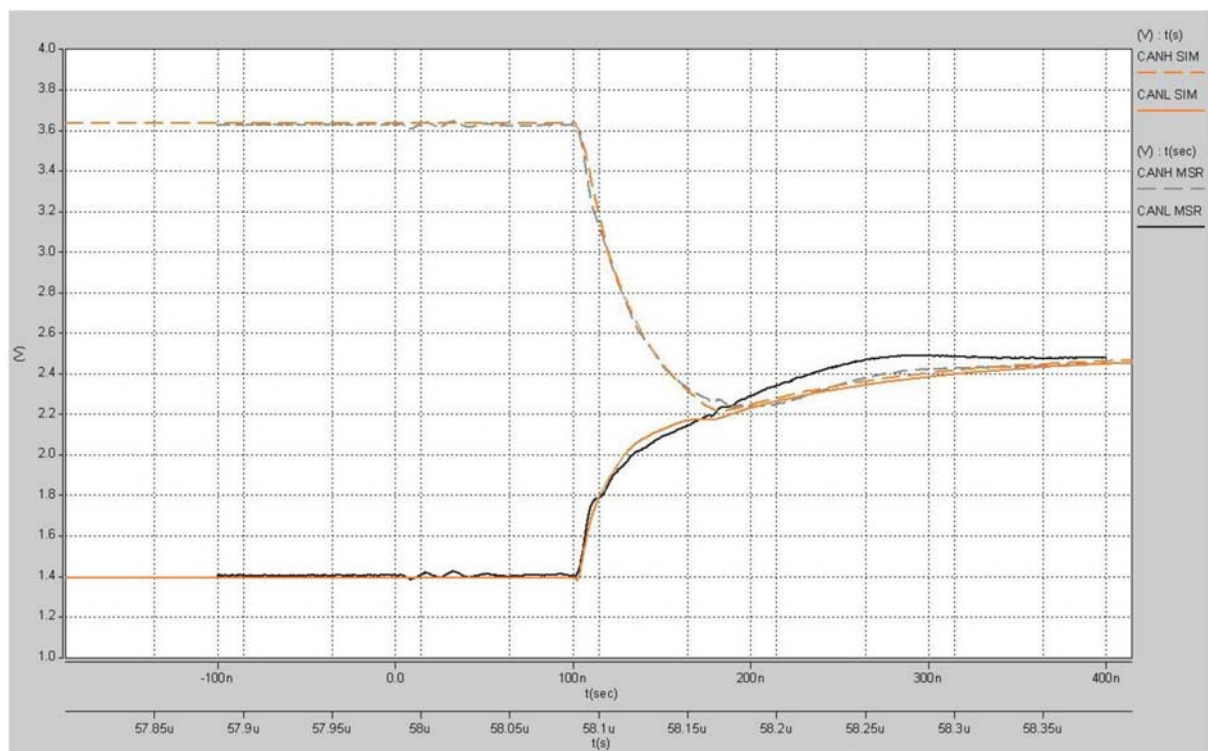


Figure 6-3. Dominant to Recessive Edge (Low)

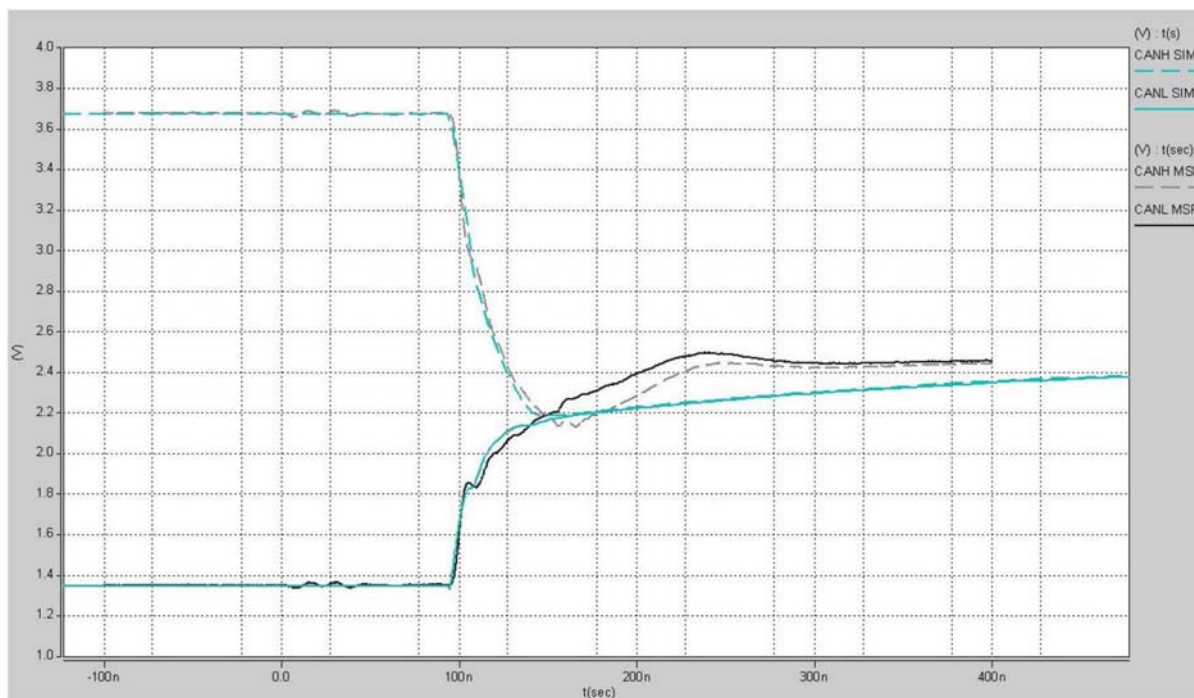
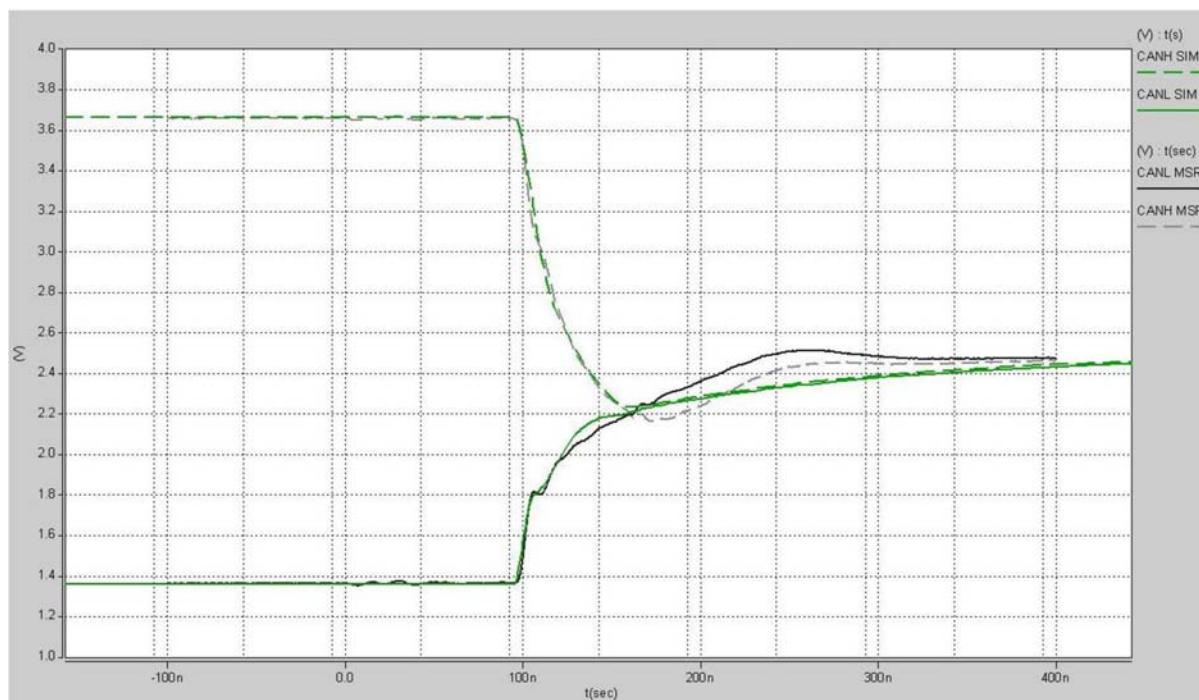


Figure 6-4. Dominant to Recessive Edge (Room)



6.2 Recessive to Dominant Edge

Figure 6-5. Recessive to Dominant Edge (High)

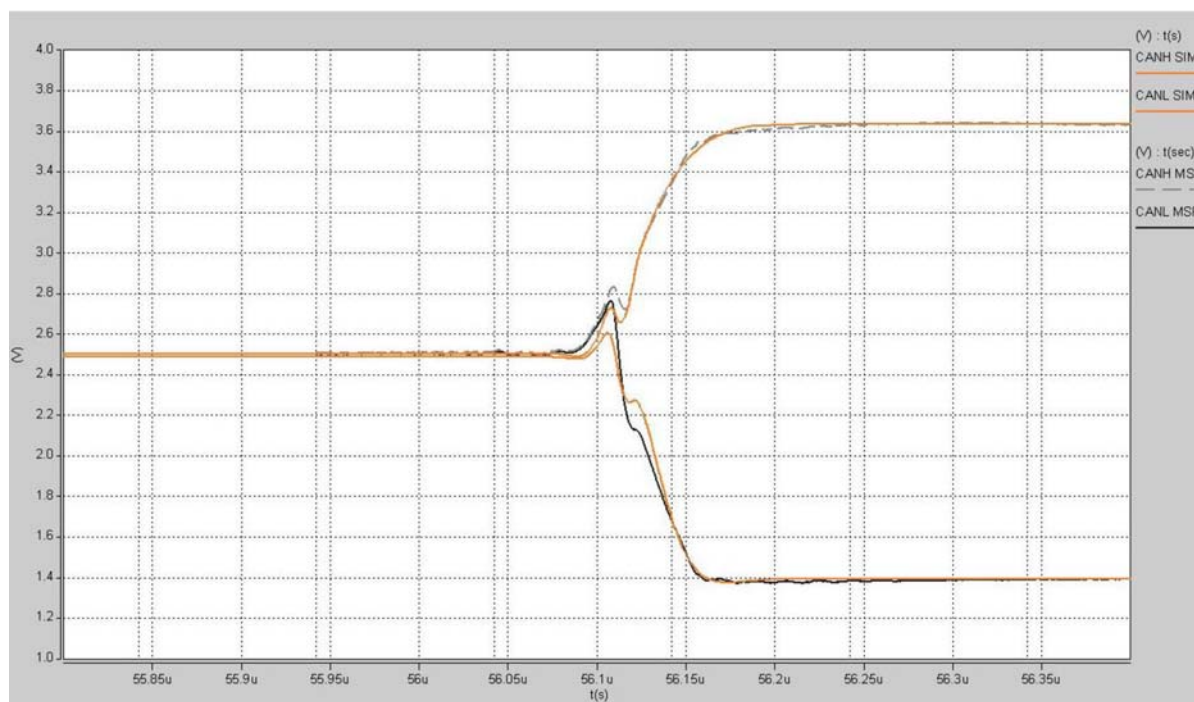


Figure 6-6. Recessive to Dominant Edge (Low)

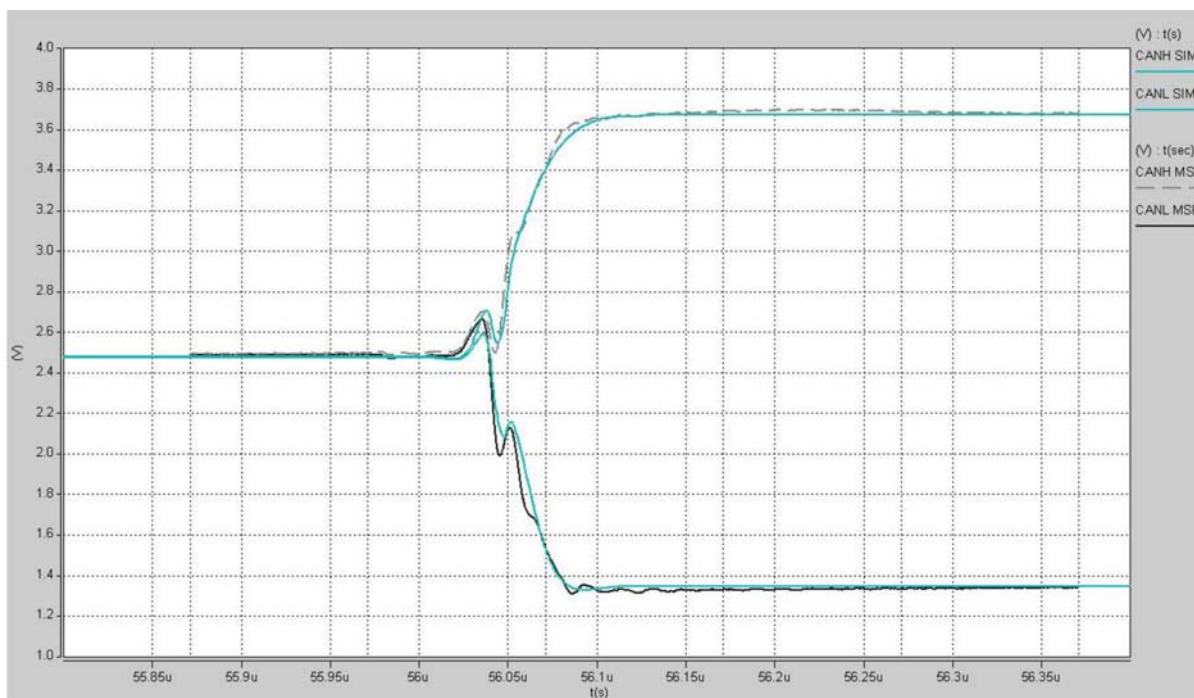
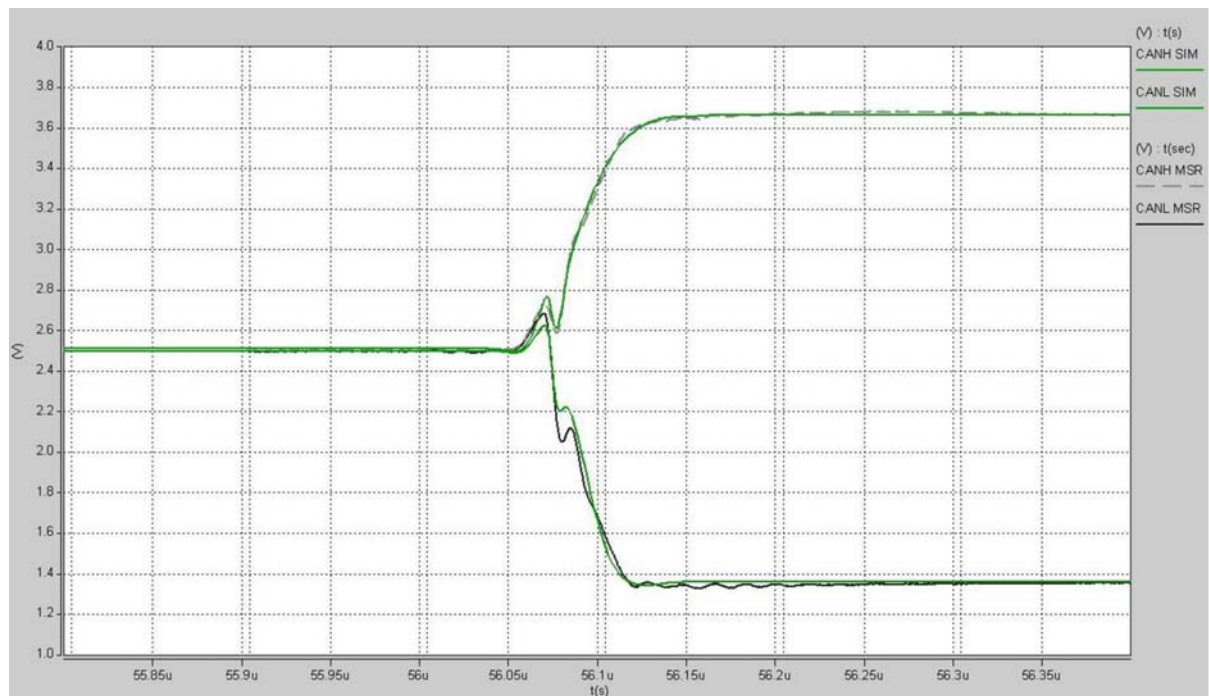


Figure 6-7. Recessive to Dominant Edge (Room)



7. Network Behavior

A test was performed in order to analyze the behavior of the model in a network of 8 devices. The network, as defined in [2], contains the characteristics described in [Figure 7-1](#) and [Table 7-1](#). The network topology is a Star ended with typical application resistor which in this case was 62 [Ω] and no load capacitance was implemented.

Figure 7-1. Network Topology

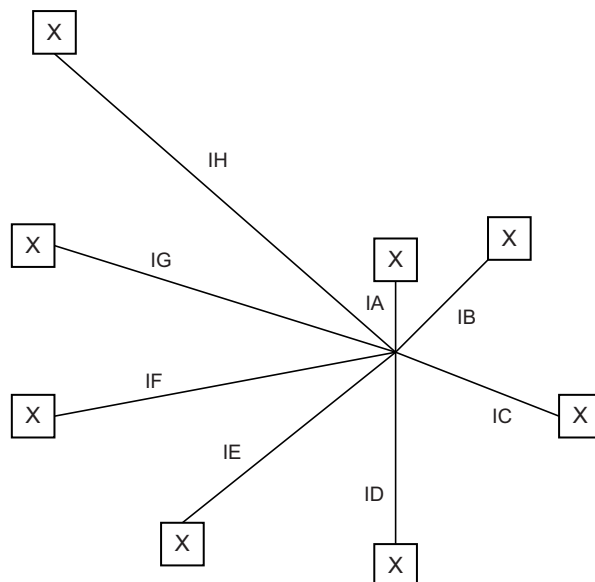


Table 7-1. Network Characteristics

Name	Node Number	Length [m]
IA	1	1.2
IB	2	2
IC	3	3.1
ID	4	4.5
IE	5	5.2
IF	6	5.9
IG	7	7.1
IH	8	8.1

[Figure 7-2](#) and [Figure 7-3 on page 18](#) show the behavior of the model in this kind of network. These figures show the measured signals CANH and CANL and the simulated signals as well. Common mode (CM) and differential mode (CAND) are computed from the mentioned signals.

Only the best and worst case are here shown, i.e. Node 1 and Node 8. The rest of the nodes show a behavior which can be interpreted as interpolation between the behavior of Node 8 and the behavior of Node 1. In this way Node 7 behaves worse than Node 2 but better than Node 8 and so on. This is understandable when looking at [Table 7-1](#), which shows the length of each stub. The non-perfect-matching ringing signals are because of the mismatch between the characteristics of the real components (termination, transmission line, connections, etc.) and the ones used for simulation.

In Figure 7-2 a dominant bit is generated in Node 1 and observed with the scope on its output. In Figure 7-3 a dominant bit is generated in Node 8 and observed with the scope on its output.

Figure 7-2. Node 1 Sending and Observed

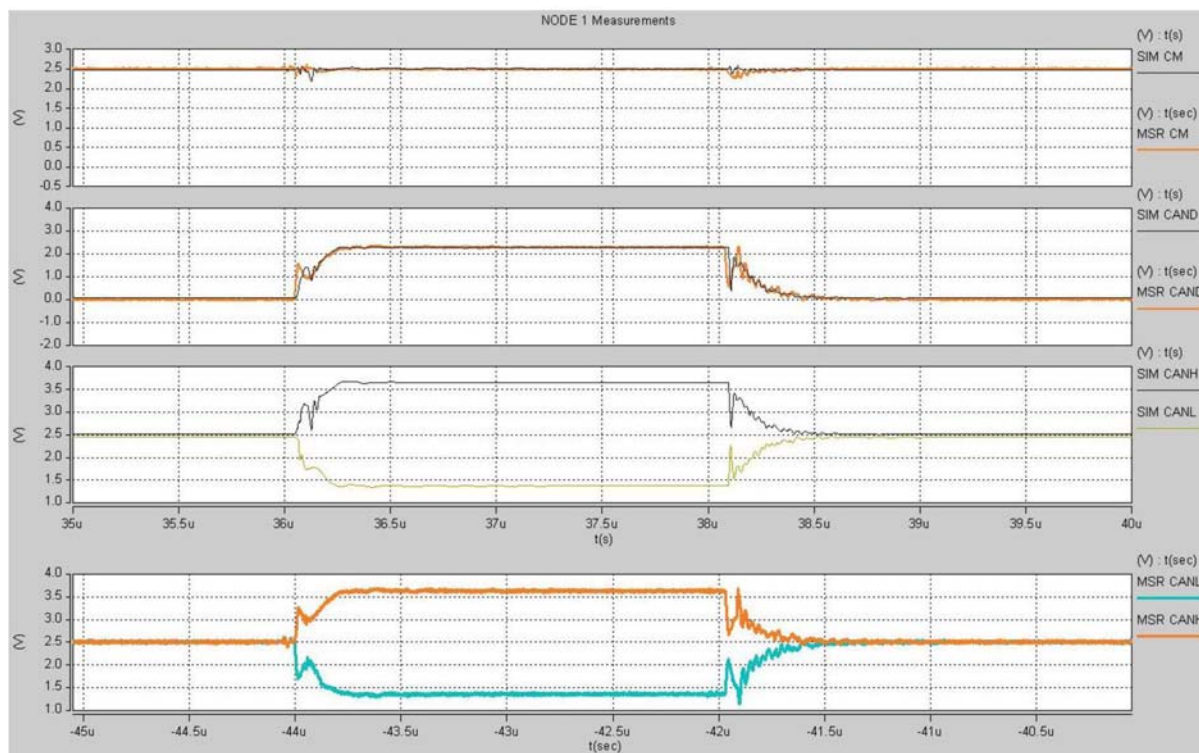


Figure 7-3. Node 8 Sending and Observed

