VSC8664

Application Note

The VSC8664 PHY in Synchronous Ethernet Applications

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first release of this document. It was published in May 2008.

2 Introduction

The growth of Ethernet in telecommunication applications has created a demand for Ethernet PHYs capable of supporting Synchronous Ethernet, as described in the ITU-T G.8261 and IEEE 1588 standards. The purpose of this application note is to assist a system developer or high-speed board designer in using the VSC8664 Quad Gigabit Ethernet PHY for Synchronous Ethernet applications.

Meeting the carrier demands for redundancy, the VSC8664 features dual recovered clocks to enable a primary and secondary timing reference. Programmable clock squelch control is included to inhibit undesirable clocks from propagating and to help prevent timing loops. Fast link fail indication (<1 ms) provides early indication of a link failure on critical metro Ethernet traffic and synchronization links.

2.1 Audience

The target audiences for this document are system or high-speed board designers using the VSC8664 for Synchronous Ethernet applications.

2.2 References

- VSC8664 Datasheet
- IEEE-802.3, CSMA/CD—Access Method and Physical Layer Specification
- IEEE-802.3ah—Ethernet in the First Mile
- IEEE-1588—Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems
- ITU-T G.8261/Y.1361—Timing and synchronization aspects in packet networks

2.3 Terms and Abbreviations

Table 1 • Terms and Abbreviations

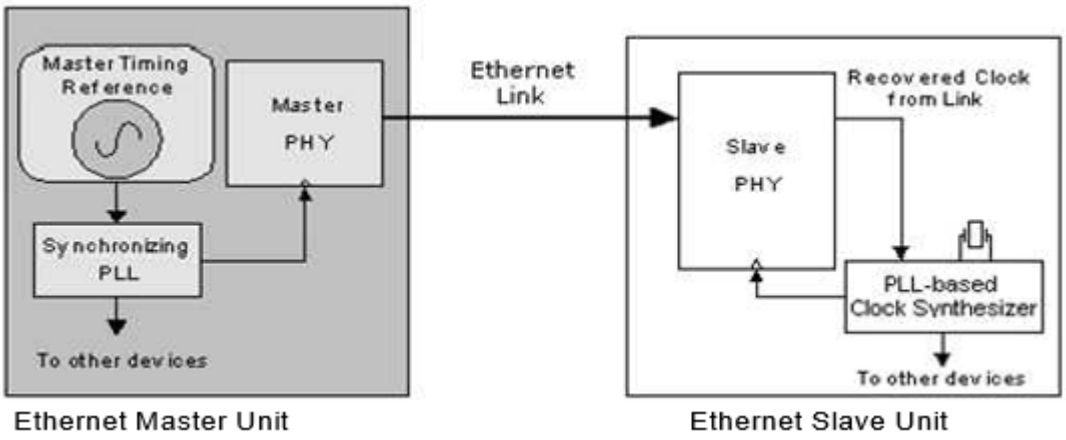
Term	Explanation
BER	Bit Error Rate
I^2C	Inter-Integrated Circuit (interface)
PHY, PMA	Physical layer (device), Physical Medium Attachment (sublayer)
PoE	Power over Ethernet
SCL, SDA	Serial Clock, Serial Data
SFP	Small Form-factor Pluggable (module)

3 Synchronous Ethernet Overview

Modern 100-Megabit and 1-Gigabit per second Ethernet PHY devices are now available, in both copper and optical physical layer variants, to enable system vendors to develop synchronous Ethernet systems for the delivery of voice, video, and data in accord with ITU-T Recommendation G.8261/Y.1361. Unlike the older 10 BASE-T protocol with indeterminate pauses between frame transfers, the VSC8664 represents a new class of Ethernet PHYs that transmit data continuously, thereby making possible the necessary clock recovery needed for synchronous data transfer.

To achieve synchronization, one of the two linked parties must derive (recover) its clock from the signal received from the other to form a Master—Slave link connection, as shown in the following figure. In this scheme, the Ethernet link transmission includes a clock signal obtained from a master timing source (such as, primary reference clock), which is recovered and passed along throughout an entire Ethernet network.

Figure 1 • Generic Synchronous Ethernet Scheme



The Master–Slave frequency lock sequence is achieved as follows.

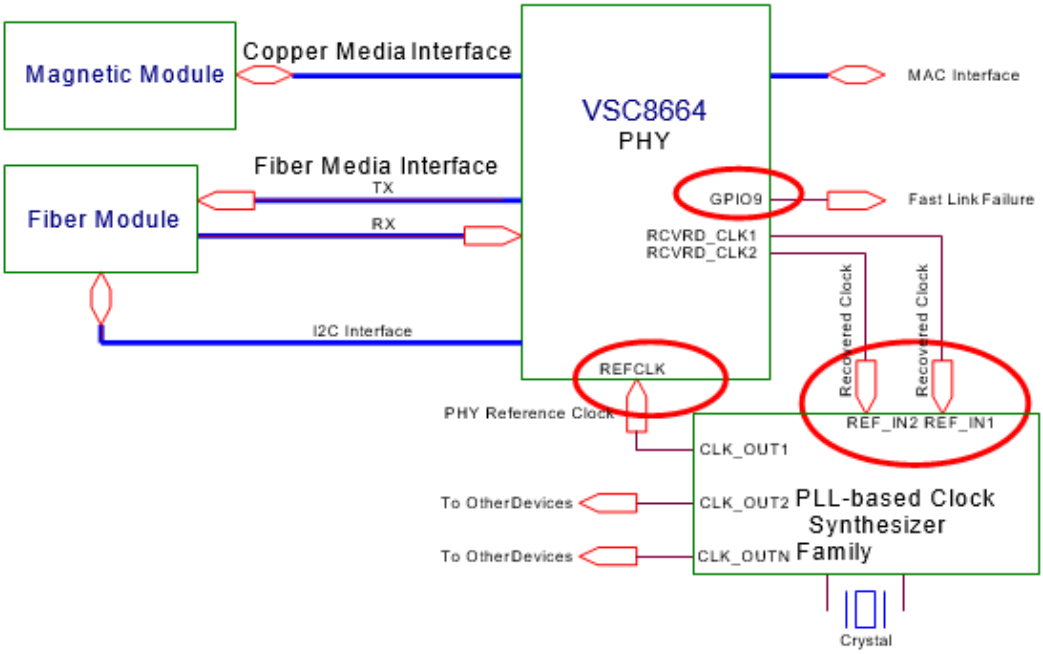
1. Before the link between the two parties is established, the PLL-based Clock Synthesizer in the Slave unit must provide the Ethernet PHY device with a free-running clock, with a frequency offset and jitter in compliance with the IEEE 802.3 standard requirements. This initial reference clock enables the Slave unit to link up with the transmitting Master.
2. Once Ethernet linkage has been established, the Clock Slave starts deriving (recovering) its clock from the signal received from the Clock Master and in turn feeds the recovered clock to the Clock Synthesizer as the new reference.
3. The Clock Synthesizer locks onto the recovered clock and the PLL then distributes synchronized clocks throughout the board; this enables the entire Ethernet Slave unit to lock to the transmission clock of the relevant ports for the given frequency reference. This switching must occur smoothly enough to not disturb the existing Ethernet link or interfere in any way with the operation of the other ICs in the specific customer's design using the other clocks produced by the Clock Synthesizer.
4. If the established link disconnects, the same smooth switching must take place in the opposite direction.

As an option, the multi-port Clock Slave device may simultaneously have several established Ethernet links, each potentially producing its own recovered clock. In this case, the local system host must make a choice in selecting which of the received links to use for the Clock Synthesizer to lock onto, in accord with the requirements of the given application.

4 VSC8664-based Synchronous Ethernet Scheme

An example of a VSC8664-based implementation of the Synchronous Ethernet Scheme is presented in the following figure, in which two clocks are recovered from either or both Copper and Fiber media. An intelligent PLL-based Clock Synthesizer is configured to lock on either of the two recovered clocks, with one selected as the primary and the other as the secondary reference. Thus, if the primary clock disappears on the Clock Synthesizer input, the VSC8664 switches to the secondary clock, switching back to the primary when it reappears. The VSC8664 uses its Fast Link Failure output to immediately notify the system host whenever switching occurs. (that is, either switching between the two recovered clocks or to a “free running” clock when both links are down.) The PHY Reference Clock, Recovered Clocks, and Fast Link Failure indicator are described in the following sections.

Figure 2 • VSC8664-based Synchronous Ethernet Clocking Scheme



4.1 Reference Clock (REFCLK) Input Requirements

4.1.1 Frequency Value

The PHY accepts reference clock frequency of either 25 MHz or 125 MHz.

4.1.2 Frequency Tolerance

To meet the IEEE requirements, the maximum frequency tolerance of ±50 ppm is recommended.

4.1.3 Jitter Tolerance

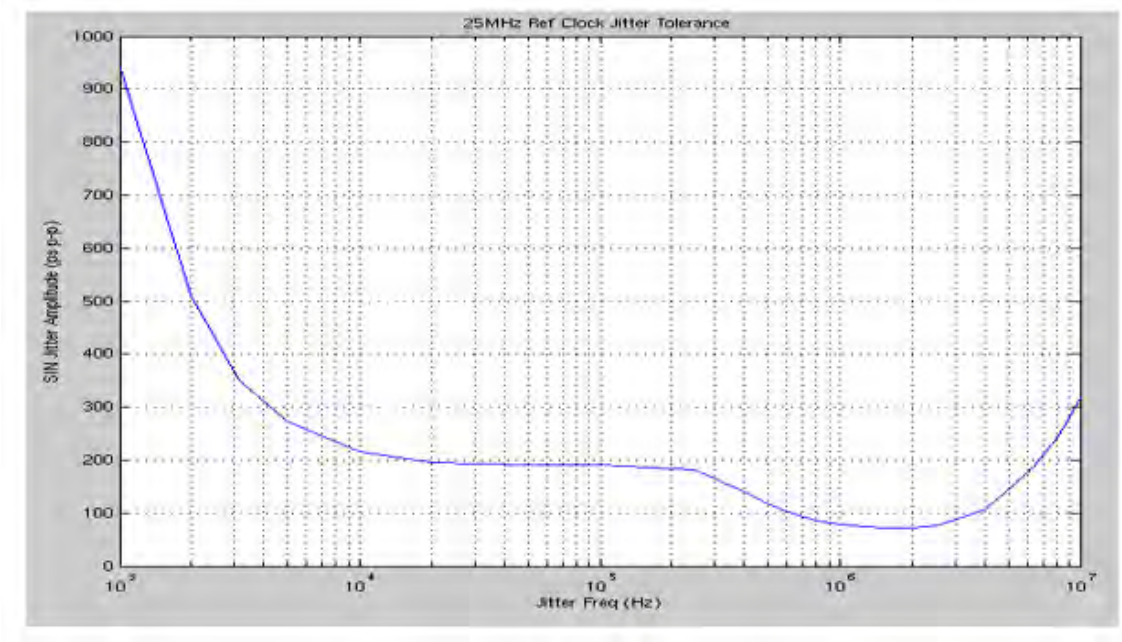
To guarantee a maximum BER of 10^{-12}, RMS jitter should not exceed 40/s (pk pk/14.1)

The following figure illustrates the VSC8664 jitter tolerance curve vs. frequency for a 25 MHz reference clock. The plot shows the maximum allowed peak-to-peak sinusoidal jitter that can be allowed in the PHY reference clock, to still meet the IEEE requirements for both Copper and Fiber media types.

Note: Measurements were made at nominal voltage supply values.

Although reference clock jitter above the plotted values would cause the transmitted PHY signal to violate the IEEE specified limit, the link partner can generally tolerate levels of jitter somewhat above the strict limit (that is, the link will still function normally), so meeting this limit allows for a more robust design in real life operating conditions.

Figure 3 • Maximum peak-to-peak Sinusoidal Jitter (25 MHz Reference Clock) to meet IEEE requirements for both Copper and Fiber Media



4.2 Recovered Clock Outputs

Two recovered clock output pins, RCVRD_CLK1 and RCVRD_CLK2, are synchronized to the active media link's clock and controlled by registers 23G and 24G, respectively.

These pins are not active when the NRESET or NSRESET pin is asserted. When disabled, the pin is held low.

4.2.1 Enabling or Disabling Recovered Clock Output

The recovered clock output is enabled or disabled by 1-bit of register 23G or 24G.

4.2.2 Recovered Clock Frequency Selection

The frequency value of each recovered clock pin is individually configured to be either 25 MHz or 125 MHz by bit 8 of register 23G or 24G. It does not depend on the media type or communication speed used.

4.2.3 Recovered Clock Jitter

The amount of jitter present in the received signal influences the jitter figures of the clock recovered from it. The following figures 4, 5, 6, and 7 illustrate the jitter transfer characteristics of the VSC8664 in providing the recovered clock signals obtained at the various Ethernet transfer rates and media types.

Note: The data was recorded at the nominal VSC8664 voltage supply settings.

This data makes it possible to evaluate the amount of jitter contained in the recovered clock signal for a given media input, and is therefore useful in selecting an appropriate PLL-based Clock Synthesizer type, that is able to tolerate the jitter levels at the frequencies covered.

The 1000BASE-T and 100BASE-T Copper media data, plotted in Figures 4 and Figure 5 illustrate that the input jitter is transferred with practically no change until a sufficiently high enough frequency is reached (in the 30 KHz—80 KHz range) before the jitter is sharply attenuated at higher frequencies. In contrast, the jitter transfer characteristics for the 1000BASE-X and 100BASE-FX Fiber media, as illustrated in Figures 6 and Figure 7, is flat at the lower frequencies, but starts increasing and peaking (by 2 dB–3 dB) before rapidly falling off at 8 MHz and 500 KHz, respectively. The two different types of jitter transfer behavior are caused by the difference in the clock recovery approaches used for Copper and Fiber physical layer types. So, the media type used in the given application is an important factor in selecting the appropriate clock synthesizer.

Figure 4 • 1000BASE-T Jitter Transfer

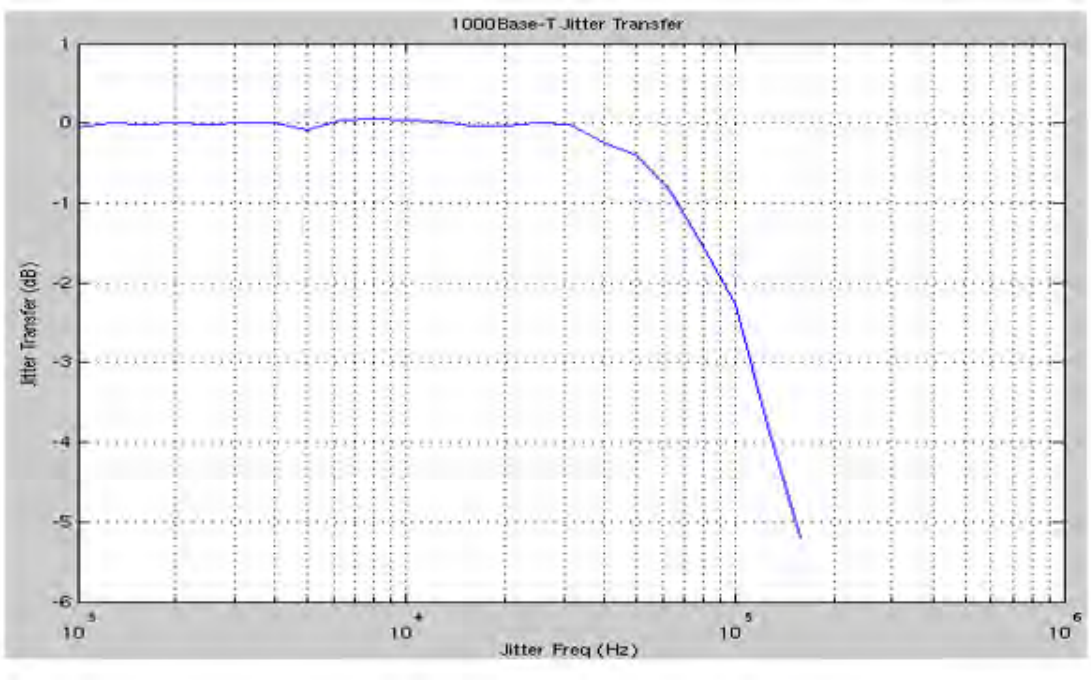


Figure 5 • 100BASE-T Jitter Transfer

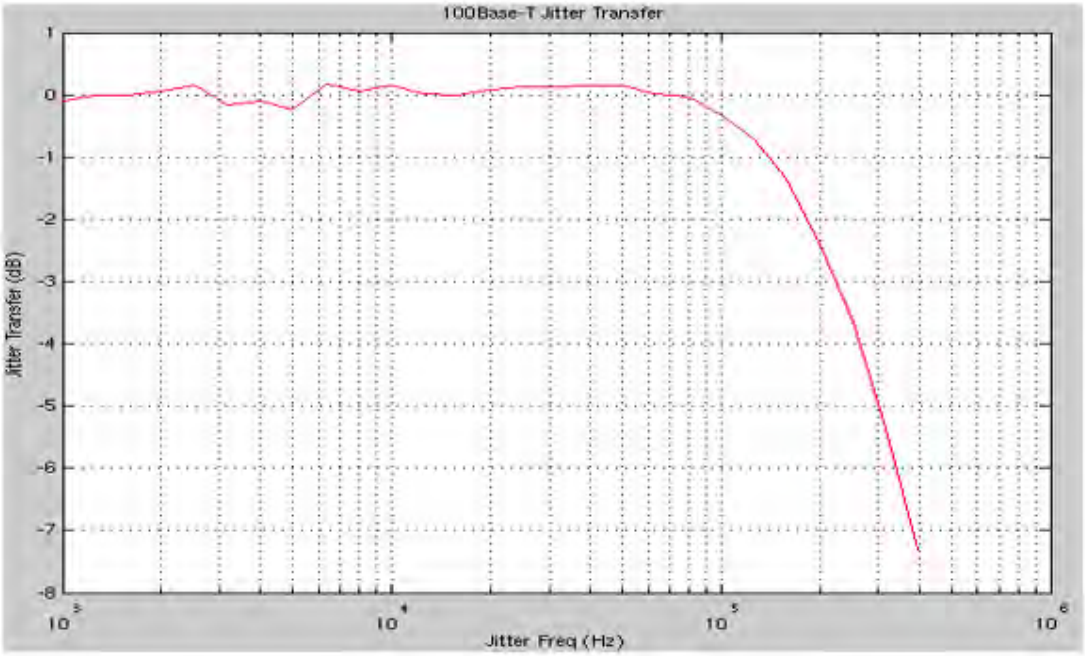


Figure 6 • 1000BASE-X Jitter Transfer

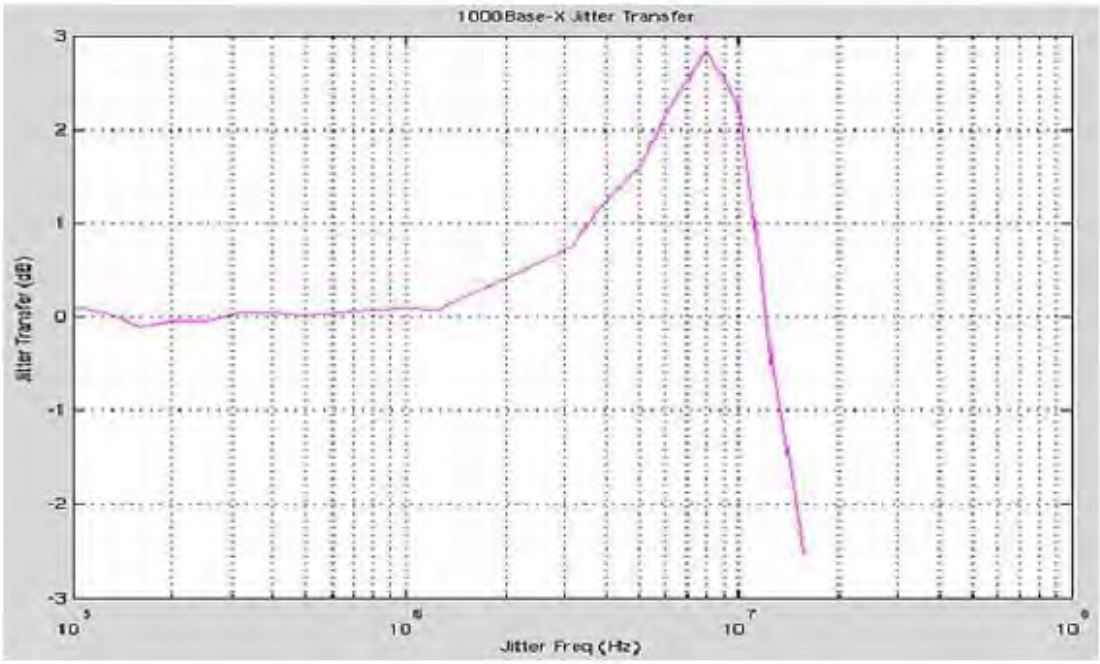
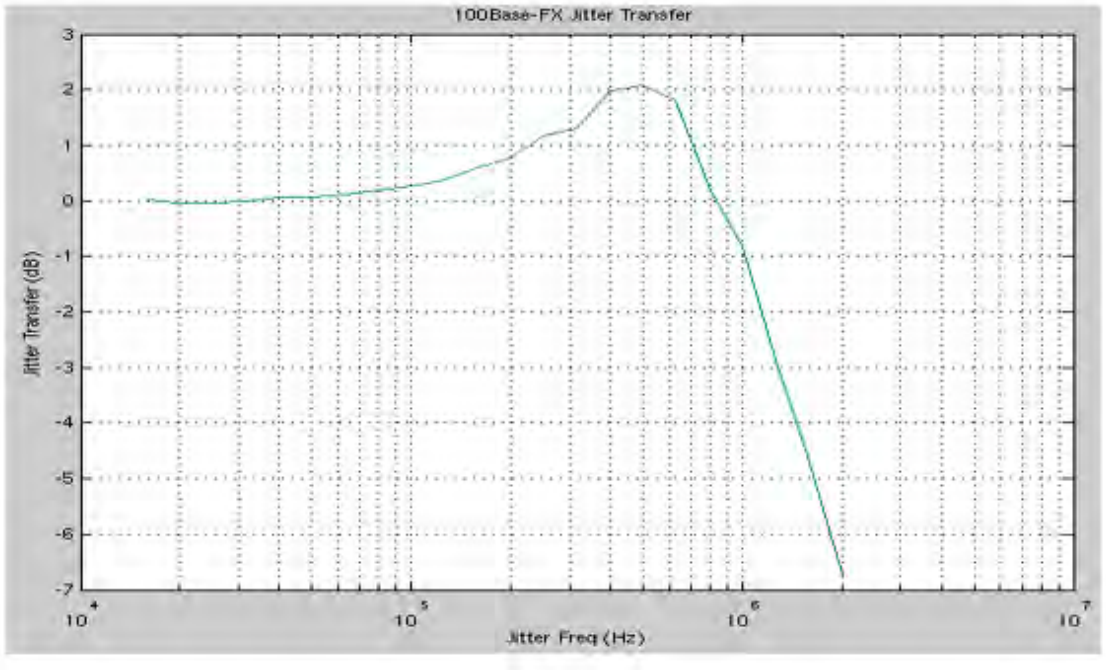


Figure 7 • 100BASE-FX Jitter Transfer



4.2.4 Clock Source Selection

4.2.4.1 Port Number Selection

The port number from which the output signal is derived is defined by bits 13:12 of registers 23G and 24G.

4.2.4.2 Recovered vs. Local Selection

Defined by bits 1:0 of registers 23G and 24G, it can be programmed to become the output clock of the following.

- Fiber SerDes media
- Copper media
- Copper transmitter TCLK (TX_TCLK) output (RCVRD_CLK1 only)
- The local REFCLK input coming into the device

According to the IEEE 802.3 standard (section “40.4.2.2 PMA Transmit function”), “the four transmitters (referred to the four copper pairs A, B, C, and D) shall be driven by the same transmit clock, TX_TCLK”. “The PMA Transmit function shall source TX_TCLK from a local clock source” or “from the recovered clock” in the 1000BASE-T Master or Slave mode, respectively.

As a part of the IEEE compliance test procedure, jitter value of this clock is measured in the Test Mode 2 (Master mode) or Test Mode 3 (Slave mode). To switch the PHY into these test modes, bits 9.15:13 are used.

4.2.4.3 If Auto-Media Sense Used

When using the Auto-Media Sense feature, changing the recovered clock output between each active media must be managed by management control via register settings.

4.2.4.4 If Copper Media Used

- As mentioned previously, a 10BASE-T's receiver does not produce a reliable continuous clock source
- In the 1000BASE-T mode, the PHY must be configured (using its Register 9) to auto- negotiate to "Slave Timing", since in the Master mode the entire PHY's clocking scheme is based on the REFCLK input pin, which is a local clock.

4.2.5 Recovered Clock Output Squelch

To prevent an undesirable local clock (based on the REFCLK input pin) from being present on the recovered clock pins, the PHY can squelch (inhibit) the clock output based on the following criteria.

- Link Status bit 1.2 = 0 (no physical link detected)
- The link is found to be unstable using the Fast Link Failure detection feature (see Section 4.3)
- The copper link is up in 10BASE-T or 1000BASE-T Master.

Different squelching options, including no squelching, are defined by bits 5:4 of the mentioned registers.

4.3 Fast Link Failure Indication

When a given port is being used as a synchronization-timing link for the system and its link goes down (fails), the system host must be immediately notified that the Clock Synthesizer input is being switched to either the secondary recovered clock or in the case of both clock links failing, a free-running clock. Such rapid notification is provided by the VSC8664 Fast Link Failure indicator, which is critical for metro Ethernet traffic and overall system synchronization.

4.3.1 Fast Link Failure Indication Timing

Since a Clock Slave PHY operating in the 1000BASE-T mode auto-negotiates to "Slave Timing" (see Section 4.2.4.4), the time required by the PHY to make decision about the link failure takes 350 ± 10 ms, as defined in section "40.4.5.2 Timers" of the IEEE 802.3 standard. Until then the "Link Status" bit 1.2 nor the appropriate LED state will not indicate the status change.

The newly introduced feature is the FAST_LINK_FAIL (GPIO[9]) pin, which indicates that in less than 1 ms, 1000BASE-T link is no longer present.

In all cases, except for the 1000BASE-T mode, this pin will be equivalent to the Link Status (Register 1, bit 2).

A 1000BASE-T link failure with this pin is based on a circuit that will analyze the integrity of the link and will assert at the indication of failure.

4.3.1.1 Port Number Selection

The pin will correspond to the port number set in bits 19G.1:0. When a link is failing, this pin will assert high and will remain this way until the link is re-established or bits 19G.1:0 are changed to an established link (on another port).

4.3.2 Enabling or Disabling Fast Link Failure Indication

To enable this feature, available for all copper and fiber media speeds, Register 19E, bit 4 must be set to 1 (0 is the default).

5 Configuring VSC8664 for Synchronous Ethernet

Presented below is a VSC8664 configuration example for a Synchronous Ethernet application. The default register values are kept unchanged since they fit the desired configuration diagrammed in Figure 2.

As a result of the following script, the PHY0 (port 0) connected to 1000 Mb/s Copper media (1000BASE-T mode) delivers a 125 MHz recovered clock on the RCVRD_CLK1 pin with Fast Link Failure indication enabled, while the PHY2 (port2) connected to Fiber (SerDes) media delivers a 125 MHz recovered clock on the RCVRD_CLK2 pin with the Fast Link Failure indication disabled. The Clock Squelch settings are enabled for both the ports (default value).

Command Format

```
PhyWrite (PortNo, reg_num(dec), 16_bit_unsigned_data(hex))
PhyRead (PortNo, reg_num(dec))

reg = PhyRead (0, 9); //Read 1000Base-T Control reg. value and assign it to variable

reg[12:11] = 10; // Modify variable value to force Port 0 into resolving as Slave
PhyWrite (0, 9, reg); // Write modified value back into 1000Base-T Control register

reg = PhyRead (0, 19E); //Read Fast Link Fail Control reg. Value, assign it to
variable

reg[4] = 1; // Modify value to enable Fast Link Failure indication for Port 0

PhyWrite (0, 19E, reg); // Write modified value back into Fast Link Fail Control
register

reg = PhyRead (0, 23G);//Read RCVRD_CLK1 register value and assign it to variable

reg[15] = 1; // Modify variable value to enable RCVRD_CLK1

reg[8] = 1; // Modify variable value to make RCVRD_CLK1 frequency 125MHz

reg[1:0] = 01; // Modify variable value to select Copper media

PhyWrite (0, 23G, reg);// Write modified value back into RCVRD_CLK1 register

reg = PhyRead (2, 24G);//Read RCVRD_CLK2 register value and assign it to variable

reg[13:12] = 10; // Modify variable value to select Port 2

reg[15] = 1; // Modify variable value to enable RCVRD_CLK2

reg[8] = 1; // Modify variable value to make RCVRD_CLK2 frequency 125MHz

PhyWrite (2, 24G, reg);// Write modified value back into RCVRD_CLK2 register


The “modify variable value” operations are presented separately for better
visibility, whereas all of them can be done using a single operation instead.
```

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