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Application Note

PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics Feature

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.1

In revision 1.1 of this document, API information was updated. For more information, see VeriPHY Calling Method.

Revision 1.0

Revision 1.0 was the first release of this document. It was published in 2016.

2 PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics

This application note provides a user with the basic knowledge of VeriPHY® – the cable diagnostics feature of Microsemi Gigabit Ethernet PHY and Integrated PHY-Switch products.

2.1 VeriPHY – Microsemi Cable Diagnostics Feature

While not required by IEEE 802.3-2012, Ethernet cable diagnostics are common features found in most PHYs. This feature is considered very important by the majority of PHY vendors. To enable maximum network management feedback to the host system and the user, VeriPHY Link Management and Cable Diagnostics Suite can be used with the device. VeriPHY integrates with NIC or switch software to greatly simplify Gigabit Ethernet network deployment and management by providing the functionality equivalent to a hand-held cable tester. The feature provides extensive network and cable operating and status information:

- Cable length of properly terminated cable
- Cable termination mismatch, including short and open states
- Identification of which cable pair (A, B, C, D) is improperly terminated
- Coupling between cable pairs.

Due to the legacy 10BASE-T hardware constraints, the cable length cannot be reliably determined when the cable is connected to a remote PHY in 10BASE-T Half-Duplex mode.

2.1.1 Fundamentals

The feature uses the Microsemi internal Digital Signal Processing (DSP) of the PHY that can investigate the input signal characteristics in order to detect the link quality. The VeriPHY software suite compares the signal received at the Microsemi PHY device to the link partner transmit signal (defined by the standard) to determine the characteristics of the specific CAT-5 cable.

2.1.2 Information Provided

The following sections provide the details of the information provided.

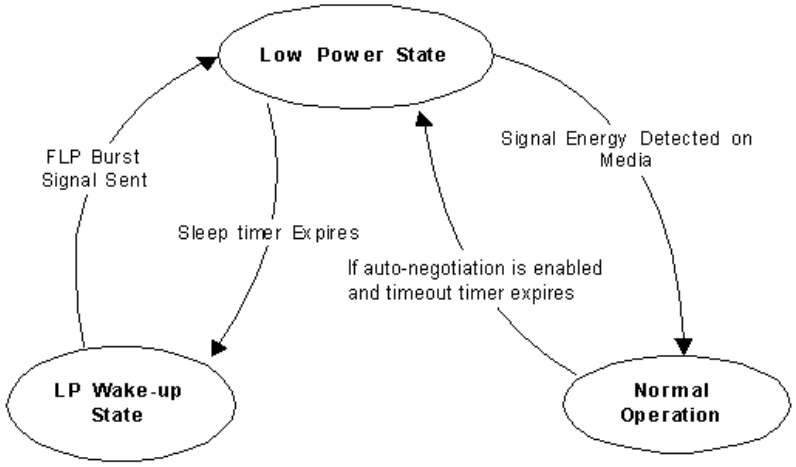
2.1.2.1 Cable Length

When properly terminated, VeriPHY reports the approximate cable length (in meters) for each of the four cable pairs A, B, C, and D, the operation range being between 7 and 120 meters with 5-meter accuracy.

2.1.2.2 Cable Pair Termination

Proper termination of the CAT-5 cable requires 100-W differential impedance between the positive and negative cable terminals. The IEEE 802.3 standard allows for a termination of as high as 115 W or as low as 85 W. If the termination falls outside of an accepted termination range, it will be reported as anomalous by the VeriPHY cable diagnostics. Open or shorted states on each of the cable pair (A, B, C, D) are also recognized and their location determined with 8-meter accuracy.

Figure 1 • Cable Pair Termination



2.1.2.3 Coupling between Cable Pairs

Shorted wires, improper termination, or high crosstalk resulting from an incorrect wire map can cause anomalous coupling between cable pairs. All these conditions can prevent the PHY from establishing a link at any speed.

The VeriPHY feature can correctly identify a cross-pair short location up to 100 meters with 10-meter accuracy.

2.2 VeriPHY Operation Details

2.2.1 Interaction with Normal PHY Operation

If a link is established on the twisted pair interface in 1000BASE-T mode, VeriPHY cable diagnostics can run without disruption of the link or of any data transfer.

However, if a link is established in 100BASE-TX or 10BASE-T, VeriPHY cable diagnostics will cause the link to drop while the diagnostics are running. Once the diagnostics are finished, the link will be reestablished.

During the time that the function is running, the PHY registers will not be available. This may affect the operation of the link status polling algorithms in some MAC chips.

2.2.2 VeriPHY Calling Method

Irrespective of the Microsemi PHY product, VeriPHY execution uses a library of routines that retrieve DSP data from the intended PHY registers and the Application Programming Interface (API) presents the diagnostics data result in the vtss_phy_veriphy_get API routine. It is recommended to take advantage of the Microsemi API library routines rather than direct register access to start the task and then collect results. See the copper PHY chip API documentation for the VeriPHY call methods included in the API package (e.g., /doc/vtss_phy).

VeriPHY API execution time depends on whether the vtss_phy_veriphy start routine runs internally by an integrated hardware mechanism, or externally by a system host. For the integrated hardware mechanism in 65 nm Microsemi PHYs, the approximate execution times (per port) are as below:

- 1000BASE-T link: 6 seconds for any cable length
- 10/100BASE-T link*: 6 to 7 seconds for any cable length
- No link: 4 seconds for any cable length

The API library routine is written such that execution time on a switch processor host will be similar.

If a link is established in 100BASE-TX or 10BASE-T, VeriPHY cable diagnostics will cause the link to drop while the diagnostics are running. Once the diagnostics are finished, the link will be reestablished. Furthermore, CAT5 or better cabling is required for valid results.

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