

PIC16(L)F15356/75/76/85/86 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F15356/75/76/85/86 family devices that you have received conform functionally to the current Device Data Sheet (DS40001866E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).

The errata described in this document will be addressed in future revisions of the PIC16(L)F15356/75/76/85/86 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (A2).

Data Sheet clarifications and corrections start on [page 5](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F15356/75/76/85/86 silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾	
		A1	A2
PIC16F15356	30B0h	2001h	2002h
PIC16LF15356	30B1h	2001h	2002h
PIC16F15375	30B2h	2001h	2002h
PIC16LF15375	30B3h	2001h	2002h
PIC16F15376	30B4h	2001h	2002h
PIC16LF15376	30B5h	2001h	2002h
PIC16F15385	30B6h	2001h	2002h
PIC16LF15385	30B7h	2001h	2002h
PIC16F15386	30B8h	2001h	2002h
PIC16LF15386	30B9h	2001h	2002h

Note 1: The Device IDs (DEVID and DEVREV) are located at addresses 8006h and 8005h, respectively. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the "PIC16(L)F153XX Memory Programming Specification" (DS40001838) for detailed information on Device and Revision IDs for your specific device.

PIC16(L)F15356/75/76/85/86

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A1	A2
Analog-to-Digital Converter (ADC)	ADC Positive Voltage Reference	1.1	Using FVR as the positive voltage reference to the ADC can cause missing codes in the conversion result	X	X
Development Support	Data breakpoints	2.1	Data breakpoints are not available on Banks 32 through 63	X	
Windowed Watchdog Timer (WWDT)	Watchdog Timer clock source	3.1	WWDT does not work with SOSC as the clock source	X	
Electrical Specifications	Minimum VDD specification for LF devices	4.1	VDDMIN specifications are changed for LF devices only	X	X
	Fixed Voltage Reference (FVR) Accuracy	4.2	FVR output tolerance may be higher than specified at temperatures below -20°C	X	X
	ADC Offset Error	4.3	ADC Offset Error specification changed	X	X
Enhanced Universal Synchronous Receiver Transmitter (EUSART)	Transmit mode	5.1	Under certain conditions, a byte written to the TXREG register can be transmitted twice	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: Analog-to-Digital Converter (ADC)

1.1 ADC Positive Voltage Reference

Using the FVR as the positive voltage reference to the ADC can cause an increase in missing codes.

Work around

1. Increase the bit conversion time, known as TAD, to 8 us.
2. Use VDD as the positive voltage reference to the ADC.

Affected Silicon Revisions

A1	A2						
X	X						

2. Module: Development Support

2.1 Data Breakpoints

Data breakpoints are not available on Banks 32 through 63. Any breakpoints that are placed in Banks 32 through 63 will fail to be recognized.

Work around

None.

Affected Silicon Revisions

A1	A2						
X							

3. Module: Windowed Watchdog Timer (WWDT)

3.1 WWDT Clock Source Selection

When the WDTCS <2:0> bits of the WDTCON1 register are set to 'b010', selecting the Secondary Oscillator SOSC 32 kHz, as the clock source, the WWDT does not operate.

Work around

Use the LFINTOSC or MFINTOSC clock sources for the WWDT.

Affected Silicon Revisions

A1	A2						
X							

4. Module: Electrical Specifications

4.1 Minimum VDD Specifications for LF Devices

VDDMIN at -40°C to +25°C = 2.3V. (See [TABLE 37-1: Supply Voltage](#) below for reference.)

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

4.2 Fixed Voltage Reference (FVR) Accuracy

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

TABLE 37-1: SUPPLY VOLTAGE

PIC16LF15356/75/76/85/86			Standard Operating Conditions (Unless Otherwise Stated)				
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
D002	VDD		1.8	—	3.6	V	FOSC ≤ 16 MHz, +25°C ≤ TA ≤ +125°C
			2.3	—	3.6	V	FOSC ≤ 16 MHz, -40°C ≤ TA ≤ +25°C
			2.5	—	3.6	V	FOSC > 16 MHz

4.3 ADC Offset Error

The table containing the Offset Error specification (AD04:EOFF) for the Analog-to-Digital Converter is modified. The updated value for Offset Error specification is +/- 3.0 LSB.

Work around

None.

Affected Silicon Revisions

A1	A2						
X	X						

5. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

5.1 Transmit Mode

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty.

This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle.

If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

1. Monitor the Transmit Interrupt Flag (TXIF) bit. Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty. If using this method, ensure that the second byte is filled in TXREG before bit 6 of the first byte is transmitted. If the delay is more than 6 bit times, there is a possibility of double byte transmission.

2. Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty. This work around can be applied if back-to-back transmissions are not necessary.

Affected Silicon Revisions

A1	A2						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001866E):

Note: Corrections are shown in bold . Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev F Document (10/2023)

Data Sheet Clarifications:

Updated data sheet revision level to revision E; removed items from previous data sheet revisions.

Rev E Document (08/2021)

Added Module 5: Enhanced Universal Synchronous Receiver Transmitter (EUSART). Updated Table 2. Other minor corrections.

Data Sheet Clarifications:

Removed Module 2: Section 4.2.3 Boot Block and Module 3: Electrical Specifications.

Rev D Document (03/2021)

Updated Tables 2 and 37-1 and Section 4.1. Other minor corrections.

Data Sheet Clarifications:

Added Module 3: Electrical Specifications.

Rev C Document (11/2020)

Added Table 37-1 and Section 4.3 ADC Offset Error; Updated Table 2 and Section 4.1.

Rev B Document (11/2018)

Added Module 4: Electrical Specifications, and Sections 4.1 and 4.2.

Data Sheet Clarifications:

Removed Modules 1 and 2. Added Module 1: Interrupt-on-Change (PORTE) and Module 2: Section 4.2.3 Boot Block.

Rev A Document (01/2017)

Initial release of this document.

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