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## DOCUMENT DESCRIPTION

**Component Placement Checklist for the LAN9117, 100-pin TQFP Package**

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# Component Placement Checklist for LAN9117

### Information Particular for the 100-pin TQFP Package

## LAN9117 TQFP Phy Interface:

1. Place the 49.9 Ω TX termination pull-up (TPO+, pin 79) as close to the magnetics as possible.

2. Place the 49.9 Ω TX termination pull-up (TPO-, pin 78) as close to the magnetics as possible.

3. Place the (2) 6.8 ηF RX Channel series AC coupling capacitors as close to the LAN9117 TQFP device as possible (pins 82 & 83).

4. Place the (2) 49.9 Ω RX termination resistors and the 0.01 μF capacitor ($C_{rxterm}$) (TPI+, pin 83 & TPI-, pin 82) as close to the LAN9117 TQFP as possible. The combination of the (2) 49.9 Ω resistors form the necessary 100-ohm termination for the RX channel.

## LAN9117 TQFP Magnetics:

1. Place the 10.0 Ω TX Channel Center Tap feed resistor as close to the magnetics as possible.

2. Place the 0.022 μF TX Channel Center Tap termination capacitor as close to the magnetics as possible.

3. Place the 75 Ω cable side center tap termination resistors and the 1000 ρF, 2KV capacitor ($C_{magterm}$) cap as close to the magnetics as possible.

## RJ45 Connector:

1. Place the RJ45 connector, the magnetics and the LAN9117 TQFP as close together as possible.

2. If No. 1 is not possible, keep the RJ45 connector and the magnetics as close as possible. This will allow remote placement of the LAN9117 TQFP.

3. Select and place the magnetics as to set up the best routing scheme from the LAN9117 TQFP to the magnetics to the RJ45 connector. There are many styles and sizes of magnetics with different pin outs to facilitate this operation. Investigate Tab-Up & Tab-Down RJ45 connectors in order to facilitate layout.

4. Place the Unused Wire Pair termination resistors and the 1000 ρF, 2KV capacitor ($C_{rjterm}$) as close to the RJ45 connector as possible.

5. Make sure to not place any other components in or near the TX Channel & RX Channel lanes of the PCB. These lanes should be clear of any other signals and components.

## Power Supply Connections:

1. Place the (8) VDD_IO decoupling capacitors for the LAN9117 TQFP as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

2. Place the (3) VDD_A decoupling capacitors for the LAN9117 TQFP as close to each separate power pin as possible. Using an SMD_0603 package will make this task easier.

3. Place the (1) VREG_3.3 decoupling capacitor for the LAN9117 TQFP as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

4. Place the (1) VDD_REF decoupling capacitor for the LAN9117 TQFP as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

## Ground Connections:

1. There are no component placement issues associated with the LAN9117 TQFP ground connections. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible.

## Voltage Reference Inputs:

1. There are no component placement issues associated with the LAN9117 TQFP Voltage Reference Input connections.

## Ground Reference Inputs:

1. There are no component placement issues associated with the LAN9117 TQFP Ground Reference Input connections.

## VDD_CORE_1.8V:

1. VDD_CORE_+1.8V (pin 3) requires a 0.01 μF decoupling capacitor and a low ESR 10 μF bulk capacitor placed as close as possible to pin 3.

2. The other VDD_CORE_+1.8V (pin 65) only requires a 0.01 μF decoupling capacitor placed as close as possible to pin 65.

## VDD_PLL_1.8V:

1. VDD_PLL_+1.8V (pin 7) requires a 0.01 μF decoupling capacitor and a low ESR 10 μF bulk capacitor placed as close as possible to pin 7.

## Crystal Connections:

1. Place the 25 MHz crystal, the zero ohm series EMI resistor and the associated 15 – 33 ρF capacitors as close together as possible and as close to the LAN9117 TQFP (XTAL1, pin 6 & XTAL2, pin 5) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.)

2. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all crystal components are referenced to the same reference plane.

## EEPROM Interface:

1. There are no component placement issues associated with the LAN9117 TQFP EEPROM Interface connections.

## RBIAS Resistor:

1. Place the RBIAS resistor as close to pin 10 of the LAN9117 TQFP as possible.

## EXRES1 Resistor:

1. Place the EXRES1 resistor as close to pin 87 of the LAN9117 TQFP as possible.

## MII Interface:

1. If the designer has elected to use impedance matching terminations in his design, these series resistors should be placed as close as possible to the source of the driving signal.

## Required External Pull-ups:

1. There are no component placement issues associated with the LAN9117 TQFP Required External Pull-up connections.

## CPU Interface:

1. The design engineer must review placement issues associated with the Host Bus CPU Interface. Specific processor design guidelines should be reviewed in determining the placement of the LAN9117 device with respect to the processor. Address, data and control signal trace lengths must be considered when placing these two devices. Critical timing issues may arise if recommended trace lengths are exceeded.

## Miscellaneous:

1. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the RJ45 in a logical place to short the two planes.

2. Bulk capacitors for each power plane can reside anywhere on the plane they serve.